COMPONENTS OF FAST ANALOG INTEGRATED MICROCIRCUITS FOR FRONT-END ELECTRONIC SYSTEMS

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Abstract

A basic set of analog integrated microcircuits (ICs) for front-end electronic systems, which have been developed and introduced into the experimental production in Russia, is presented.

In the capacity of active components the ICs employ n-p-n transistor structures including those with Schottky diodes, p-n-p lateral transistors, p-n-p vertical transistors with the collector in the substrate, field-effect p-n junction transistor structures, precision diodes with the Schottky barrier. Resistors (low- and high-Ohmic) and capacitors on the basis of MOS-structures are used as passive components of the ICs.

The design principles of the IC active components have been described, the dependencies of main parameters of the typical (library) components on bias and temperature have been considered.

1. INTRODUCTION

By the present time in Russia, the following items have been developed and introduced into the experimental production:

- ICs containing a fast comparator and a D-trigger, which are intended to be used in time-of-flight systems of plastic wall type;
- the four-channel ICs of an amplifier-shaper with differential inputs and outputs for use with wire detectors and intended for the amplitude data processing (amplification, filtration);
- the four-channel ICs of a differential low-power comparator of the nanosecond range, which is intended for analog signal discrimination;
- the four-channel ICs of a differential comparator of the nanosecond range, which contains a circuit for the hysteresis regulation.

The following developments are at their final stage:

- the eight-channel LSI circuits containing analog and discrete-analog channels for radiation detector data processing;
- the ICs of a fast sample-hold, which are intended for signal sampling before analog-digital conversion, analog-digital processing (filtration, commutation) of rapidly changing signals.

The circuit-engineering of the pointed microcircuits has been developed by the specialists of the Electronics department at Moscow Engineering-Physics Institute (University).

In the capacity of active components the ICs employ n-p-n transistor structures including those with Schottky diodes, p-n-p lateral transistors, p-n-p vertical transistors with the collector in the substrate, field-effect p-n junction transistor structures, precision diodes with the Schottky barrier. Resistors (low- and high-Ohmic) and capacitors on the basis of MOS-structures are used as passive components of the ICs.

General questions of the design of similar active components are expounded in reports [1,2]; and those of passive components, especially of high-Ohmic resistors, are in literature [3].

However, the circuit-engineering of each type of the microcircuits pre-determines specific requirements to their components. The most complicated among the IC components are: transistor structures with the Schottky barrier, p-n-p lateral transistors, field-effect p-n junction transistors. Let us consider the principles of their design and the results of investigation of each among them.

2. EXPERIMENT AND RESULTS

2.1. Transistor structures with the Schottky barrier (TS)

Simulation and calculation of microcircuits by using a PC have shown that the values of working currents Ic in TS amount to 0.3-5 mA. On taking this fact into account, in the IC lay-out development two typical (library) structures have been used, one of which has been calculated for the collector working current I_c=0.3...1 mA and the other has been calculated for I_c=3-5 mA. They are different only in geometrical dimensions especially in the perimeter of the emitter P_e. The two structures are implemented with two basic contacts and one collector contact.

Cross section of the transistor with the Schottky barrier is presented in fig.1.

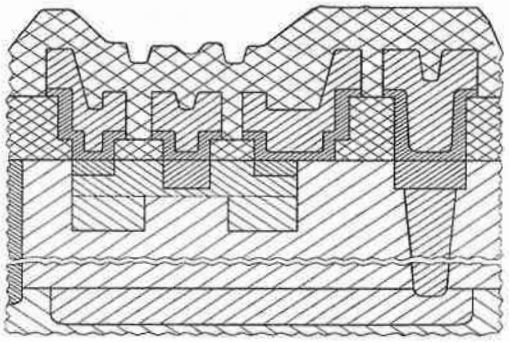

Fig.1. Cross section of the transistor with the Schottky barrier

Molybdenum which possesses a value of the work function of approximately 0.2eV less than that of aluminum (φ_c=0.5 and 0.7-0.72 correspondingly) is used as the barrier metal here. This permits approximately 0.2 V reduction of the forward voltage drop in case of molybdenum metallization (at the identical areas of diodes). Hence, employment of molybdenum as the barrier metal makes it possible to reduce the area of the Schottky diode (DS) and, correspondingly, its stray capacitance C_{DS}. Besides, molybdenum performs a role of the barrier metal in the emitter region preventing interaction between silicon and aluminum and excluding shorts in the emitter p-n junction, which could arise because of electromigration. Technological peculiarities of microcircuits for front-end electronics which have been developed in Russia are expounded in report [4].

Criterion of an optimum area of the diode in the transistor with the Schottky barrier is the difference in the forward voltage drops between the p-n junction and the diode, which is ensured at a level of U_{FOR}=0.1...0.15 V in the range of working current densities and working temperature. Besides, from the viewpoint of ensured dynamic parameters, the difference in U_{FOR} between the collector p-n junction and the diode with the Schottky barrier must be not lees than 0.1-0.15 V; and, from the condition of a minimal value of the collector-emitter voltage reached in the saturation mode Ucesat, the difference in U_{FOR} between the emitter p-n junction and the diode with the Schottky barrier must be not larger than 0.1-0.15 V.

One of the main characteristics of TS, that considerably determines the IC parameters especially the speed, is the current amplification cut-off frequency f_C. Typical dependencies of f_C on the emitter current Ie for the two types of the library transistor structures are given in fig.2 and 3.

Measurements of f_C were carried out by using the results of checking the phase angle of the current transmission factor in the common-base circuit arg(h_{21b}). The phase angle arg(h_{21b}) between vectors of the collector and emitter currents is linearlly increasing with the increase in the measurement frequency f and can be described by the expression

$$\arg(h_{21b})=(f/fc)[rad]=57.3(f/f_C)[grad]$$

The cut-off frequency represents itself as the transconductance of the phase-frequency characteristic.

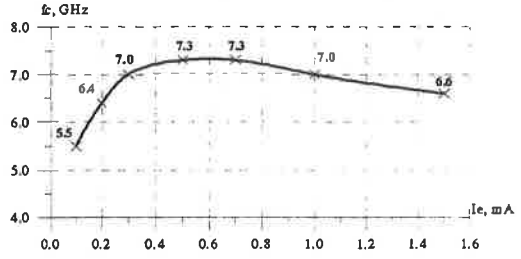

Fig.2. Dependence of the current amplification cut-off frequency f_C on the emitter current Ie for the I type structure

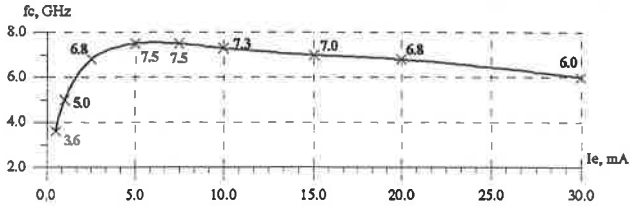

Fig.3. Dependence of the current amplification cut-off frequency f_C on the emitter current Ie for the II type structure.

From fig.2 and 3 it can be seen that the two structures possess a maximal value of fc which amounts to the order of 7 GHz directly in the range of the working currents.

From the dependence $f_C=f(I_e)$, by means of constructing a graphical dependence of $1/2\pi f_C$) on $1/I_e$, the information about the emitter junction capacitance of the transistor structures biased in the forward direction and about the parameter "cut-off frequency of the transistor theoretical model" f_{CTM} has been obtained. The delay of the signal transmission from the emitter to the collector can be represented by the following expression:

$$T_{ec}=1/2\ f_C=r_eC_e+\ 1/f_{CTM},$$

where: r_e=26mV/I_e - is the resistance of the emitter;

C_e - is the capacitance of the emitter junction biased in the forward;

$1/f_{CTM}$ - is the delay which is determined by transmission of a signal through the base, the collector junction and the collector bulk and which is not dependent on the emitter current in the considered range of currents.

Calculated values of C_e have made up 0.07 and 0.2 pF correspondingly.

The calculation of the microcircuits by using PC have shown at the same time that, apart from a high value of f_c, the transistor structures must be characterized by a value of the current transmission factor h_{21e} of not less than 50 (at t_{amb}=25±10°C) in the range of working currents Ic.

Dependencies of the h_{21e} value on the collector current Ic for the two types of structures are represented in fig.4 and 5 from which it is seen that the h_{21e} value amounts to 70 in the range of working currents I_c at t_{amb}=25±10°C.

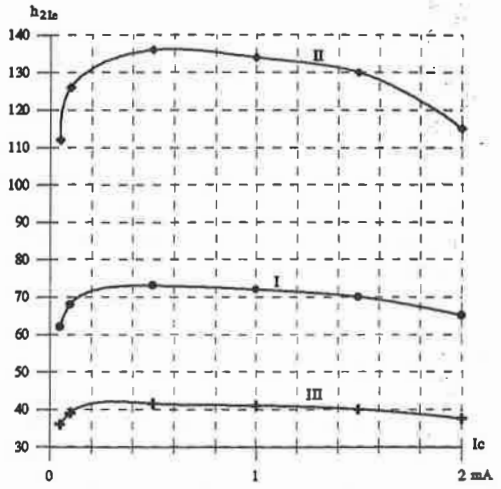

Fig.4. Dependence of the current transmission factor h_{21e} on the collector current I_c and the ambient temperature for structures of the first type

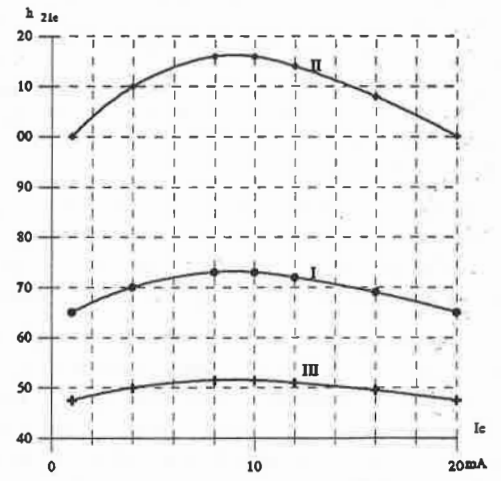

Fig.5. Dependence of the current transmission factor h_{21e} on the collector current I_c and the ambient temperature for structures of the second type

The character of the presented dependencies corresponds to theoretical models - lower values of h_{21e} are caused by the influence of recombination components of the base current Ib at low currents; and by the less effectiveness of the emitter at higher currents. At the same time fig.4 and 5 show dependencies of h_{21e} on the ambient temperature t_{amb}: (I) is for t_{amb}=25±10°C, (II) is for t_{amb}=125±3°C , (III) is for t_{amb}=-60±3°C . They have a shape which is usual for silicon planar transistors: at t_{amb}=125±3°C an approximately two-fold increase of the h_{21e} value is observed in comparison with the h_{21e} value at t_{amb}=25±10° C; and at t_{amb}=-60°C the decrease is also approximately of two fold. Therefore the microcircuit calculation must be carried out by taking the minimal value h_{21e}=30 i.e. the worst exploitation conditions.

Thus, the performed investigations have shown that the typical (library) transistor structures are characterized by: low stray capacitances of the isolation, collector and emitter junctions (in particular, they make up 0.3; 0.2; 0.07 pF correspondingly in the structures of the I type); a high value of the current amplification cut-off frequency f_C (7GHz); the current transmission factor h_{21e}=70.

2.2. P-n-p lateral transistor structures

In fast sampling-hold microcircuits, the p-n-p lateral transistor structures are used as the current-setting components. The lay-out fragment of the IC containing such structures is shown in fig.6. As a rule, the regions of the collector and emitter are created at the same time with the base doping diffusion into n-p-n structures, i.e. the both types of the transistors are compatible in the manufacturing technology.

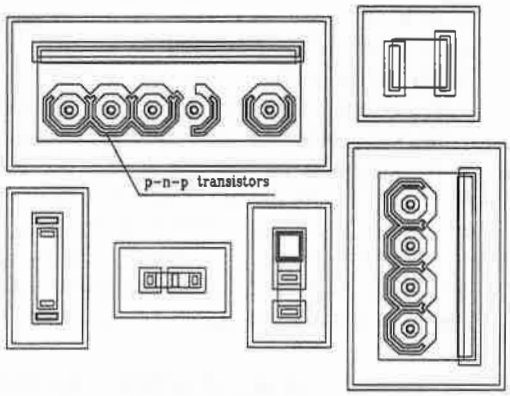

Fig.6. The IC lay-out fragment

Dependencies of the current amplification factor β on the collector current Ic are given in fig.7 for three types of the p-n-p lateral transistors which are identical in the lay-out but different in the technological regimes.

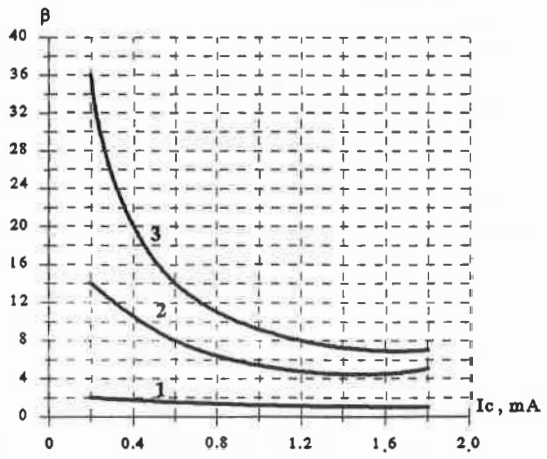

Fig.7. Dependences of the current amplification factor β on the collector current Ic for three types of the p-n-p lateral transistors.

In the first two of them (curves 1,2) the manufacturing processes for n-p-n and p-n-p structures were unified, i.e. $h_e=h_c$ (h_e, h_c* - are the depths of the emitter, collector junctions in the p-n-p transistor; h_c is the depth of the collector junction in the n-p-n transistor); in the third transistor (curve3) the fabrication of p-n-p structures is previous to the creation of n-p-n structures. In the first case h_e=1μm, in the second case h_e=1.5 μm , in the third case h_e=1.7 μm.

Analysis of the presented data has shown that the main parameter which influences the current amplification factor β is the emitter junction depth he (at N_S=1.5...3.3 10^{19} at/cm^3). When the collector junction depths are less (h_c<1.5μm), the processes of the complementary transistor structures creation must be separated. This requirement becomes especially actual in cases when the current amplification cut-off frequency fc in the n-p-n structures is the factor which determines increase of the IC speed.

The structure marked in fig.6 by a dotted line has been chosen as a basic structure and has been calculated for the working current Ic=1mA. Designing of structures working at high currents (of the order of 2..4 mA) was carried out by means of parallel connection of a few basic structures. Employment of such a principle has permitted the required current setting in the microcircuit to be reliably reproduced (even when the absolute value of β has some fluctuations).

2.3. Field-effect p-n junction transistors (FETs)

The circuit-engineering basis of the fast sampling-hold IC is the set-up structure of the double-correlated sampling [5] where the amplification module has been constructed on the basis of the circuit of the three-stage voltage follower with an input stage fabricated on a field-effect transistor with p-n junction and p-channel.

Simulation and computing of the microcircuit functional modules have permitted us to define the requirements to parameters of their components. In particular, it has been proved that the FETs must simultaneously possess: the pinch-off voltage Up of not larger than 2V; the initial saturation current Isat of not less than 2 mA; the source-drain breakdown voltage Usd of not less than 25 V.

The design of structures which possess such a combination of parameters is connected with compromising solutions. Besides, the parameters of FETs are largely determined by the regimes of the channel and gate ion doping.

In the calculation and experimental investigations it has been found out that in order to reach the pinch-off voltage Up of 2 V the channel and gate ion doping must be carried out in the following regimes: Q=0.5μCoul/cm^2, E=100keV and Q=10μCoul/cm^2, E=100keV correspondingly and with the subsequent annealing at T=1100°C, t=60 min to form the channels (boron) and at T=1050°C, t=15 min to form the gates (arsenic).

The value of the initial saturation current Isat is determined by the geometrical dimensions of the channel region and by the number of gates. In particular, in order to increase Isat it is necessary to reduce the channel length L, to extend its width Z and to increase the number of gates.

3. CONCLUSIONS

1.Criterion of an optimum area of the diode in the transistor with the Schottky barrier is the difference of the forward voltage drops between the p-n junction and the diode, which is ensured at a level of U_{FOR}=0.1...0.15 V in the range of working current densities and working temperature. Besides, from the viewpoint of ensured dynamic parameters, the difference in U_{FOR} between the collector p-n junction and the diode with the Schottky barrier must be not lees than 0.1-0.15 V; and, from the condition of a minimal value of the collector-emitter voltage reached in the saturation mode U_{cesat}, the difference in U_{FOR} between the emitter p-n junction and the diode with the Schottky barrier must be not larger than 0.1-0.15 V.

2. In the experimental investigations it has been found out that the main parameter which influences the current amplification factor β is the emitter junction depth h_e (at Ns=1.5...3.3 10^{19} at/cm^3). When the collector junction depths are less (hc<1.5μm), the processes of the complementary transistor structures creation must be separated. This requirement becomes especially actual in cases when the current amplification cut-off frequency fc in the n-p-n structures is the factor which determines increase of the IC speed.

3. The design principles for p-n-p lateral transistors have been proposed. They are based on the parallel connection of a few basic structures (I_c=1mA), that has permitted the required current setting in the microcircuit to be ensured (even when the absolute value of β has some fluctuations).

4. In order to reach the pinch-off voltage U_p of 2V in the field-effect transistor with p-n junction and p-channel, the channel and gate ion doping must be carried out in the following regimes: Q=0.5 μCoul/cm^2, E=100keV and Q=10μCoul/cm^2, E=100keV correspondingly and with the subsequent annealing at T=1100°C, t=60 min to form the channels (boron) and at T=1050°C, t=15 min to form the gates (arsenic). Besides, a good concurrence of the calculated and experimental results has been achieved.

Employment of circuit-engineering solutions which take into account peculiarities of specific physical experiments, in particular, 'Hades' (GSI, Darmstadt), the development of the original lay-outs defended by protection documents, optimization of the technological processes of the microcircuits manufacturing have permitted the creation of the set of

ICs which are not inferior in their main electrical parameters to the best foreign functional analogs.

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