

LHC-B Collaboration

LHC-B Data Flow Requirements

User Requirements Document

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Abstract

This document summarises the basic requirements for the buffering, processing, monitoring and control of the data flowing from the detector front ends through all stages of the trigger . It covers the requirements in the following areas:

- *The buffering and bandwidth required in sub-detector front-end electronics to meet the demands of the Level-0 and Level-1 triggers.*
- *The pre-processing and multiplexing of detector data to provide digital, zero-suppressed data to the data acquisition system(DAQ).*
- *The bandwidth and buffering required for reading zero suppressed sub-detector data into DAQ.*
- *Event building with error detection and recovery.*
- *The execution of the Level-2 and Level-3 trigger algorithms.*
- *The calibration, monitoring and storage of event data.*
- *Parallel and asynchronous running of different sub-detector configurations using separate trigger sources.*

The working point of the data acquisition system will be a 40 kHz Level-1 trigger rate and an average event size of ~100 kByte, including an allowance for electronic noise, this giving an event building requirement of ~4 GB/s. The processing requirement for the Level-2 and Level-3 triggers corresponds to ~1400 1000 Mips processors.

The principle criteria for the design and implementation of the system, which must develop with running conditions evolving over a long period of time, are also summarised.

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1 Introduction

1.1 Purpose of the document

This document specifies the requirements for the dataflow from the detector front-end electronics through all stages of the LHCb Trigger/Data Acquisition system (DAQ). It considers all the requirements involved in the buffering, communications, processing and control of the dataflow.

The following sub-systems impose requirements:

- a. The detector front-end electronics readout
- b. The LHCb hardware trigger systems(level-0 and level-1)
- c. The LHCb high level trigger algorithms
- d. The Trigger and Timing Control system (TTC)
- e. The LHC machine control system
- f. The LHCb operator control system
- g. The LHCb run configuration description
- h. The LHCb event store
- i. The LHCb Detector Control System (DCS)

In addition to these requirements we consider overall requirements such as performance, cost, maintainability, and also those coming from general system, software and hardware considerations.

1.2 Scope of document

The following functions can be identified, in the context of the dataflow :

1.2.1 The Sub-detector front-end electronics readout

A general front-end model has been developed based on which each sub-detector which have pipelines, buffers, and control and processing functions to enable them to conform to the trigger strategy. The general front-end model has FE-links leading from the sub-detector front-end electronics to the data acquisition system. The data acquisition readout scheme must take account of the physical constraints imposed by each sub-detector and also provide multiplexing, buffering and data processing facilities to prepare the data in a form appropriate for all levels of trigger processing..

The DAQ system should be capable of providing initialisation, monitoring and error recovery procedures for sub-detector front-end systems.

1.2.2 The LHCb hardware trigger sub-systems(level-0 and level-1)

The design parameters for these triggers impose the requirements on the sub-detector electronics for readout and buffering.

Within the data acquisition system functions must be provided to read out the trigger sub-systems results as for sub-detectors.. In addition the data acquisition must be responsible for initialisation, control and error recovery for the trigger sub-systems.

1.2.3 The LHCb high level trigger algorithms

The algorithms will require processing, buffering and data access capabilities in the data acquisition system in order to satisfy the data access, execution time and input rate requirements. These DAQ functions of buffering, data switching and processing will be highly dependent on the algorithms and the patterns of data in the detectors providing the triggers.

1.2.4 The Trigger and Timing Control system (TTC)

Within the front-end design interfaces are provided allowing TTC to be used to distribute timing and control signals to all detectors, in a suitably partitioned manner, these including the Level-0 and Level-1 Accept signals.

Functions must be provided by the data acquisition system for initialisation, monitoring and error recovery of the TTC sub-systems. In addition configuration and partitioning of the sub-detectors and their segments (stations) must be possible to allow independent running according to the needs of the sub-detectors.

1.2.5 The LHC machine control system

Functions will be provided for monitoring the machine state, and making this information available to LHCb sub-systems.

The state of the LHCb detector will be communicated to the LHC machine.

1.2.6 The LHCb operators

A unified control interface will be provided for control and monitoring of the sub-systems used for triggering and data-taking. This will provide status displays, and control facilities for all aspects of data taking.

1.2.7 The LHCb run configuration description

DAQ will update the description of the run configurations to reflect the detector sub-systems participating, and also to reflect all trigger parameters.

1.2.8 The LHCb event store

The DAQ system will write events according to physics classifications into the central event store together with full information about data-taking conditions.

1.3 Definitions, acronyms and abbreviations

1.3.1 [Definitions]

Detector This term is used to refer to the entire LHCb detector.

Sub-detector This term is used for individual major detector elements i.e the vertex, calorimeter, muon, RICH, tracking 'sub-detectors.'

Level-0 The high pT triggers combining information from the calorimeters and the muon spectrometer.

Level-1 Combination of vertex trigger and track trigger.

Level-2 Software trigger combining momentum information from the trackers with the vertex detector information on primary and secondary vertices.

Level-3 Software trigger involving partial or full event reconstruction, and applying cuts relevant to the physics channels of interest.

Front-end Electronics All of the sub-detector electronics including the front-end multiplexers.

Front-end Multiplexers Following a Level-1 accept all data flows to this stage which processes and multiplexes sub-detector data in a sub-detector dependent manner prior to placing it, in a standard protocol, onto the front-end links.

Front-end Links These carry the zero-suppressed sub-detector data from the front-end multiplexers into the Readout Units of the data acquisition system. These will be standardised for the experiment.

Readout Units These units perform mini event building of the sub-detector fragments coming on the front-end links. They also buffer the data as necessary according to the overall event building needs.

Readout Network This network routes the sub-detector data from the Readout Units to the processors which perform the Level-2 and Level-3 trigger algorithms.

Sub-Farm Contollers These units accept the sub-detector data coming from the Readout Units via the Readout Network, build complete events and pass them to selected processors.

1.3.2 [Acronyms]

CERN	European Laboratory for Particle Physics
DAQ	Data AcQuisition
DCS	Detector Control System
FEM	Front-End Multiplexer
RU	Readout Unit
SFC	Sub-Farm Contoller

1.4 References

- [1] K. Krisebom et al. (The LHC-B collaboration), *LHC-B Letter of Intent*, CERN/LHCC 95-5, LHCC/I8, 1995.
- [2] The LHC-B Collaboration, *Trigger and Data Acquisition System for LHC-B Experiment: Current status and work programme*, LHC-B 97-0008, CERN/LHCC 97-14, 1997.

1.5 Overview of the document

The requirements placed upon the dataflow system come from various sources. These may be broken down as follows (Acronyms in bold are used to label the requirements in this document):

READ : detector readout (covers flow from the very front-end electronics through to the data acquisition Readout Unit)

TRG0 : Level-0 trigger

TRG1 : Level-1 trigger

TRG2 : Level-2 trigger

TRG3 : Level-3 trigger

TTC : Timing control system

EB : Event building (distributed throughout dataflow) protocols

DTPAR: Detector parameter description

EVSTORE : Event Storage

LHC : communication with LHC machine supervisory systems

OP : operators of the DAQ system

DCS : the Detector Control System

The following are classes of requirements which apply to the overall system rather than coming from a specific 'user'. As such one could regard them as internal requirements for the design of a viable system.

GEN : General Design Criteria

MON : monitoring

MODE : running modes

CAL : calibration

TEST : testing

PART : system partitioning

UINT : user interfacing

FAULT : faults

CON : control functions

SAF : safety

HARD : hardware

SOFT : software

COMM : commissioning of the system

The **Requirements** are broken down into **sub-chapters** with the following themes

- **Data Traffic Patterns** - the sizes , distributions and rates of data coming from detector and trigger systems. Requirements for different modes of running are considered.
- **Data Flow Protocols** - the necessary protocols involved in trigger and timing control signal distribution, and the control of dataflows according to running states. The protocols involved in event building (including error recovery).
- **Data Processing** - the requirements for processing coming from the high level triggers
- **System Aspects** - this will cover configuring, partitioning, running modes and overall system considerations such as error detection and recovery
- **Calibration and Monitoring**- requirements in addition to those given by 'data traffic patterns'
- **General Design Criteria**- the overall requirements for hardware and software design-standards, reliability, maintainability,scalability

In each of these chapters, before listing the specific requirements, there is some overview discussion.

2 General Description

2.1 Overview of Trigger/DAQ

At the nominal LHCb running luminosity single interaction beam collisions will occur at about 10 MHz. By using a pile-up veto it is proposed to accept only these at the initial level of triggering, Level-0, which applies high p_T cuts using muon chambers, and hadron and electron calorimeters. It is proposed to tune the cuts to allow 1 MHz average output rate at Level-0.

At Level-1 will be applied a vertex topology algorithm to find primary and secondary vertices using data from the 17 silicon stations close to the beam interaction. In addition at Level-1 it is proposed to have a track trigger using seeds from Level-0. It is proposed to apply cuts giving a 40 kHz output rate, of which will be around 2kHz of Bs, several kHz of charm, and the remainder minimum bias events such as strange decays.

Detector data is read at a nominal rate of 40 kHz into the data acquisition system, which will transfer data into processors where high level trigger algorithms reduce the event rate to storage to some 200 Hz.

It is proposed to break down the high level algorithms into 2 broad classes. Firstly the so called Level-2 algorithms, which using the track and vertex guidance from the trigger, look to reduce the rate to some 5 kHz using only partial event data. The strategies will include refining the vertex detector decision with full precision data and enhanced algorithms, and then combining VD and track spectrometer data. The Level-3 algorithms will involve partial or full event reconstruction to apply physics cuts appropriate to the CP violation channels.

The overall trigger architecture is illustrated in Figure 1

2.2 User characteristics

These requirements are written with in mind the total dataflow for the LHCb experiment. Thus the users, from whom we obtain the requirements, are the total community of physicists, engineers and programmers contributing to the design and implementation of the detectors and data handling systems according to the requirements imposed by the physics aims of the experiment. Each specific requirement has the a named source.

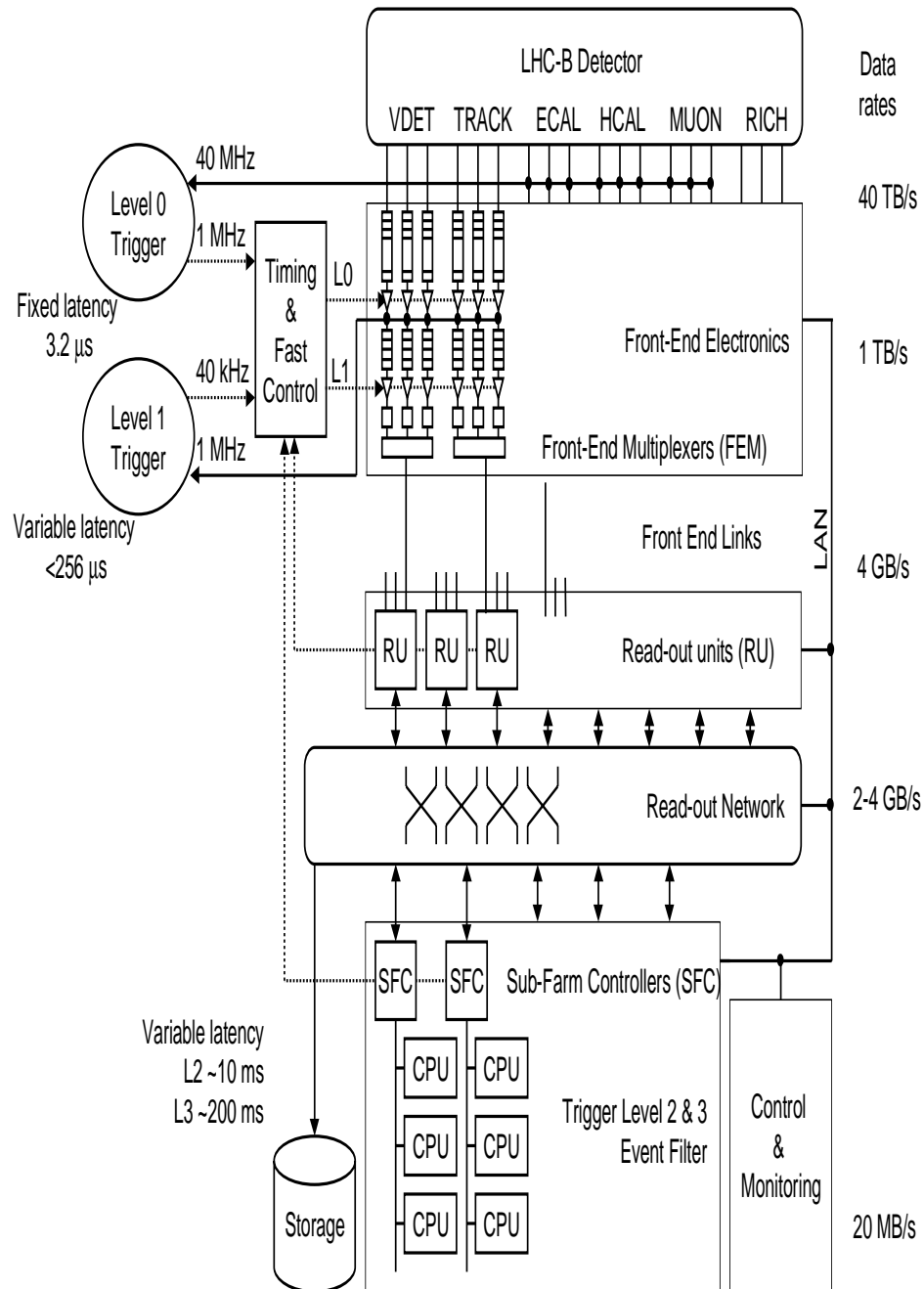


Figure 1 Trigger/Data Acquisition Architecture

2.3 Operational environment

The operation of the Trigger/DAQ system will be according to the phases of the experiment and the LHC machine

- a. Machine shutdown periods
- b. Machine stop periods
- c. Machine cold start
- d. Preparing for physics data taking
- e. Physics data taking

When the machine is running the detector, and the electronics the detector side of the protecting wall, will be inaccessible. It is foreseen that the DAQ and the Trigger sub-systems will be in a counting room which is accessible during machine running. Also sub-detector groups may choose to put the last stage of their front-end electronics in an accessible counting room.

In general the system must be runnable by non-experts, whether the experiment is in or out of physics run mode. Outside physics one foresees parallel running of different sub-detector configurations using triggers appropriate for tests or calibrations. This will be the major mode of running in the years preceding LHC start-up.

During physics running the data taking will be fill and run oriented, with one or more runs in a fill, a run being data taken with the same detector and environment conditions.

3 Requirements (Capabilities and Constraints)

3.1 Data Traffic Patterns

There are 3 modes of running to be considered, each of which impose different requirements for dataflow.

- **Physics data taking** with zero suppressed and formatted data at the nominal design rates.
- **Calibration running** where typically one needs to accept full raw data at rates determined by the detector dependent calibration procedures
- **Test Pattern running** where the dataflow test patterns generated by detector dependent procedures

The physics data will include, in addition to the zero-suppressed sub-detector data on physics triggers, data arising from special triggers, for example for embedded calibrations or storing scalars for monitoring. Since zero-suppression and the attachment of special data is performed after a Level-1 accept, the type of Level-1 trigger will need to be passed to the front-end electronics. The readout system must cope with the normal physics events and the special 'events' which may be substantially larger. Also random triggers must be permitted which will pass all levels of the trigger system. These can be used to monitor sub-detector noise, and also as a means to transport special data not connected to the current beam crossing.

The nature of calibration data, acquired during dedicated runs, is quite different to that of physics data. Usually the data will not be zero-suppressed and all channels will be read out, giving rise to very large event sizes. Consequently the trigger rate used will be adapted to meet the system bandwidth.

For detector testing it will be necessary to artificially generate signals at the detector front ends. Also for testing DAQ we need to generate patterns simulating closely physics data. The DAQ system should support the readout of both types of test pattern.

The DAQ system must provide readout facilities for the following detectors (ACRONYMS in brackets after the detector names)

- Silicon detector (**VERTEX**)
- Upstream RICH detector (**RICH1**)
- Downstream RICH detector (**RICH2**)
- Inner Trackers (**ITRACK**)
- Outer Tracker (**OTRACK**)
- Electromagnetic Calorimeter (**ECAL**)
- Hadron Calorimeter (**HCAL**)
- Muon tracking (**MUON**)

Fig. 2 shows the generic scheme for detector readout necessary for compatibility with the proposed trigger scheme. The placement of the digitisation and multiplexing functions will be detector dependent.

The essential buffering components of the generic front-end model as shown in Fig.2 are:

- **Level-0 Latency Buffer** - to provide storage of detector data during the fixed 3.2 microsec latency of the Level-0 trigger.
- **Level-0 Derandomiser Buffer** - to smooth out the statistical fluctuations in the Level-0 trigger prior to downstream electronics for multiplexing, digitisation and Level-1 processing.
- **Level-1 Latency Buffer** - to provide storage of detector data during the variable latency of the Level-1 trigger.
- **Level-1 Derandomiser Buffer** - to smooth out the data flow following Level-1 decisions, into downstream electronics for multiplexing.

The scheme has well defined requirements for these components which are summarised prior to specifying those requirements which are sub-detector dependent.

In the sections on requirements for individual sub-detectors we have included information which is relevant to the structure of the digital, zero suppressed data that comes into DAQ. As such we include information on channel occupancies, and also indicate where we need to read more one bucket of data on a trigger accept.. We need to this when front-end delays (drift + electronics+cable) can be longer than 25 ns.

3.1.1 Detector Front-End Electronics

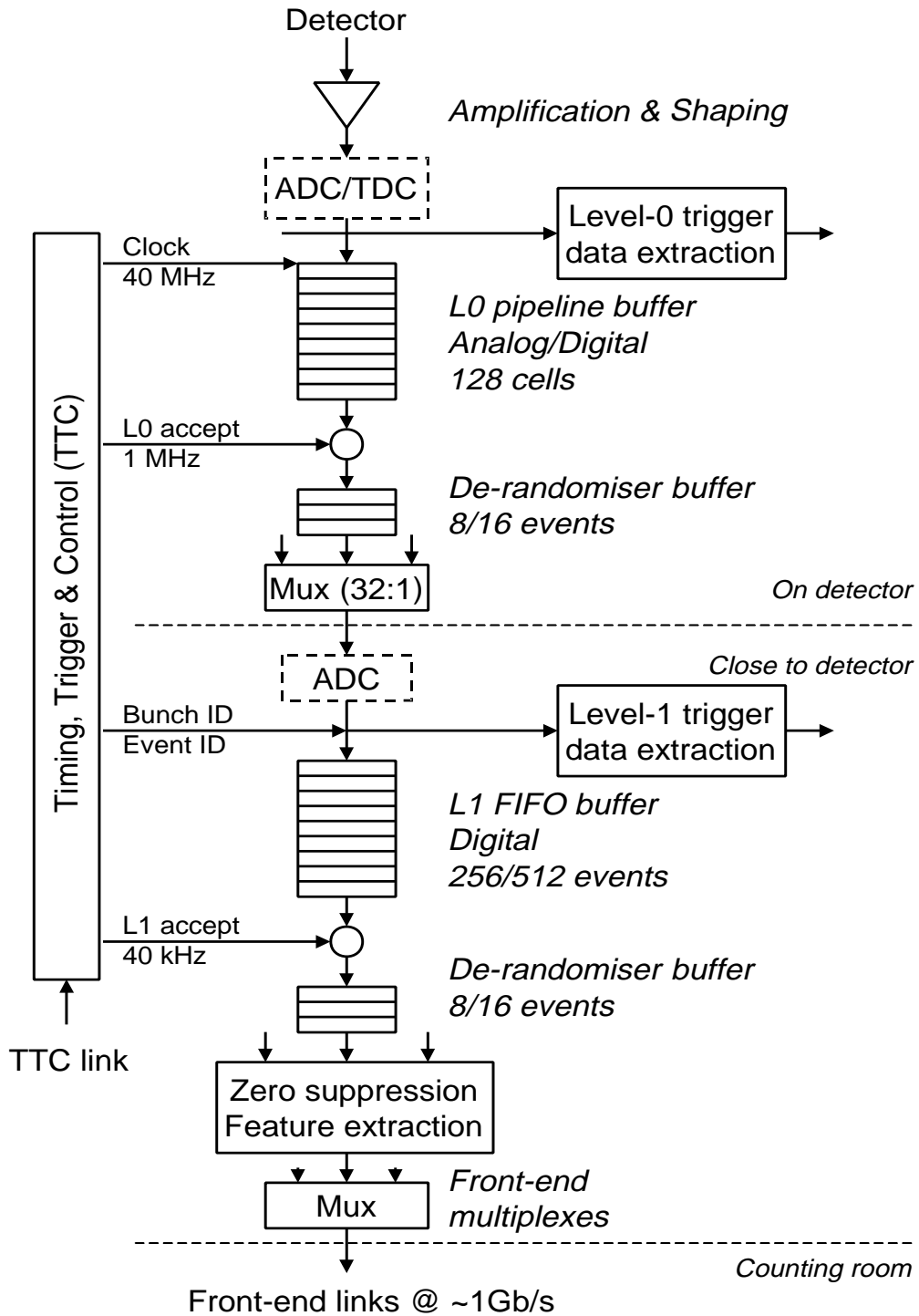


Figure 2 Front-End Electronics Model

UR READ01 All sub-detectors must follow the agreed definitions for the specifications of the Level-0 pipeline buffer, Level-0 derandomiser buffer, Level-1 FIFO buffer and the Level-1 derandomiser buffer.

Need Essential

Priority High

Stability The depths of the buffers have to defined according to performance/cost trade-offs

Source LHCB TDAQ group

UR READ02 All sub-detector Level-0 data, on a Level-0 accept, must be read out into the Level-1 digital FIFO buffers within 1 microsec.

Need Essential

Priority High

Stability The multiplexing, link and digitisation details are sub-detector dependent and will evolve with the design

Source LHCB TDAQ group

UR READ03 All sub-detector data, on a Level-1 accept, must be pre-processed and multiplexed in order to put zero-suppressed data, in an agreed protocol, onto high bandwidth links leading to DAQ.

Need Essential

Priority High

Stability Pre-processing required is sub-detector dependent, and will evolve with design.

Source LHCB TDAQ group

UR READ04 The trigger number and beam crossing number must be added into each event fragment. In order to allow proper synchronisation of event building null fragments should be generated when the sub-detector element has no data.

Need Essential

Priority High

Stability Stable

Source LHCB TDAQ group

3.1.2 Vertex Detector

UR READ_VERTEX VERTEX Readout - There are 17 stations of 13K channels each. On average there are ~600 clusters to be read out spread over the 17 stations. A cluster is coded in 6 bytes. The average event size, without noise, is ~4kByte.

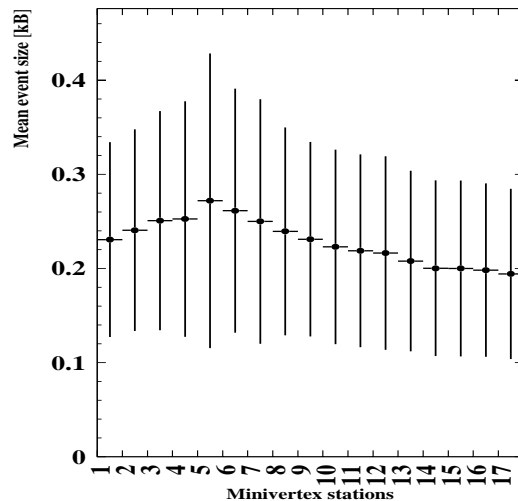
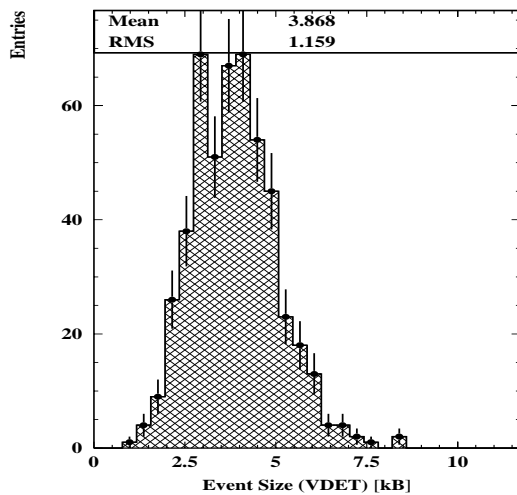
- **Number of Channels** - 220 K
- **Channel Partitioning**- 17 stations of 12966 ch., 6 r-sectors(1265 ch.)and 6 phi-sectors(896 ch.) per station
- **min occupancy** - 0.1%
- **av occupancy** - 0.3%
- **max occupancy**-2 %
- **Multiplexing before DAQ** - . (17 or 12 outputs according to multiplexing on station(18) or sector (12) basis)

Need Essential

Priority High

Stability Estimates under review as a function of simulation results

Source LHCb VD group



The above plot shows the variation in event size over a large sample events. Also shown is the event size per station. The average number of strips hit/track is ~1.3. These are readout in addition to the 2 adjacent strips. Each cluster is coded as 6 bytes (16 bit address, 2 bit strip count, 4*6 bit signals, 6 bits common mode)

3.1.3 RICH Readout

UR READ_RICH RICH Readout . Event data is read from RICH1(140K channels) and RICH2(200). On average there are ~2700 hits in RICH1 and ~1000 in RICH2. Hits are coded in 4 bytes. Average event sizes are ~11 kByte and ~4 kByte for RICH1, RICH2 respectively.

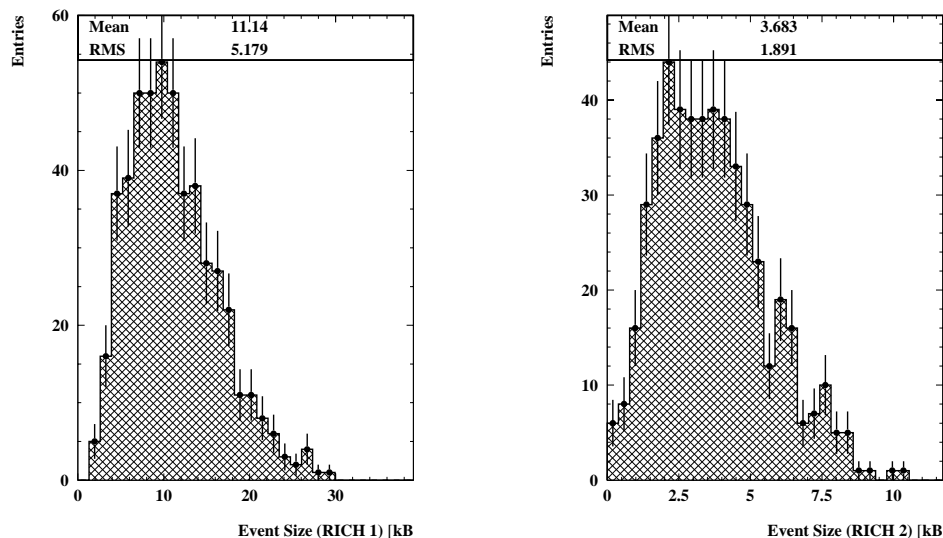
- **Partitioning** 2 detectors,RICH1 and RICH2
- **Number of Channels** - ~ 340K, RICH1 having about 140K channels and RICH2 200K channels.
- **Min Occupancy** - 0.1%
- **AV Occupancy** - 2% RICH1 , 1% RICH2
- **Max Occupancy** - 5%
- **Multiplexing before DAQ** - to be determined

Need Essential

Priority High

Stability Estimates under review as a function of simulation results

Source LHC-B RICH group(R Forty, Andre T.)



The plots above show the variation, event by event, of the data in RICH1 and RICH2. Each hit is coded in 4 bytes (2 byte address, 2 byte data)

3.1.4 Outer Tracker Readout

UR READ_OTRK OTRACK Readout. Event data is read from 109K channels, spread over 10 stations. An event gives ~4750 hits, on average, spread over the 10 stations. A hit is coded in 4 bytes. Since electronic delays are greater than 25 ns. we must read data for 2 beam crossings. This increases the average event size to ~24 kByte.

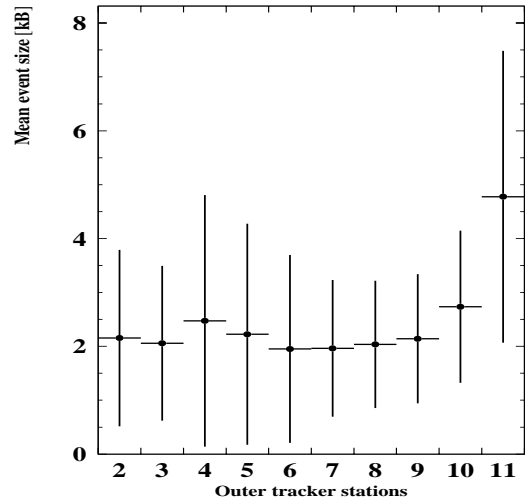
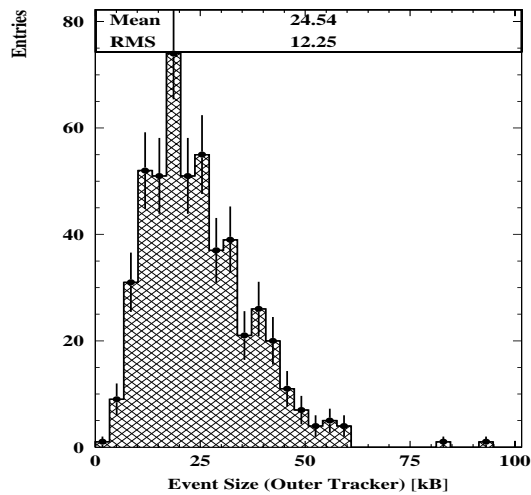
- **Number of channels** -- 108.8K
- **Channel Partitioning** -10 stations
There are 4 planes/station (vert.,+5,-5,vert). In addition stations 2 and 10 have 2 additional planes with horizontal wires. Station 11 is special, and has 2 planes with horizontal wires and 2 with vertical wires. Planes are divided into modules, each with 256 readout channels.
 - Station 2 (behind RICH)- 6.0K channels
 - Station 3 - 10.2K channels
 - Station 4 - 10.2K channels
 - Station 5 -10.2K channels
 - Station6(just behind coil) -11.6K channels
 - Station 7 - 9.9K channels
 - Station 8 - 10.4K channels
 - Station 9 - 11.0K channels
 - Station 10 (before RICH2) - 16.4K channels
 - Station 11(behind RICH2) - 12.9K channels
- **Min Occupancy** - < 1%
- **AV Occupancy** - 4.5% overall. This rises to 7% for busy modules in stations 2,3,4 close to beam pipe
- **Max Occupancy** - 9%. In hottest area of hottest station
- **Data sampling** - 6 bit TDC, 2 samples per Level-0 accept
- **Multiplexing onto detector links** - do at level of module of 256 channels. These links lead off detector to higher order multiplexing prior to going onto DAQ. With 110K channels need around 450 such links. Worst case capacity for link 8 Mbit/s.
- **Off Detector Multiplexing** - takes data from 450 detector links, and puts onto higher performance links leading into DAQ the zero suppressed, multiplexed data-

Need Essential-

Priority High

Stability Estimates under review as a function of new design and simulation results

Source LHCb OuterTracker group(B Koene,Andre T.)



Plots above show the variation, event by event, of the number of hits for a single event. However OTRACK must be read out in 2 buckets to allow for delays of more than 25 ns. Since we have 25% probability of an event in the next bucket (as well as allowing for the probability there was an event in the previous) we must scale this estimate by ~ 1.3 .

- Assume 16 bit address + 2×8 bit data sample per hit

3.1.5 Inner Tracker Readout

UR READ_ITRK ITRACK Readout - We read from 11 stations. The preferred technology for stations 1-4 is silicon, and MSGC for stations 5-11. For the MSGC we must read 2 bunch crossings. The average number of hits for an event is ~2000. A hit is coded in 4 bytes. The average event size is ~10kByte

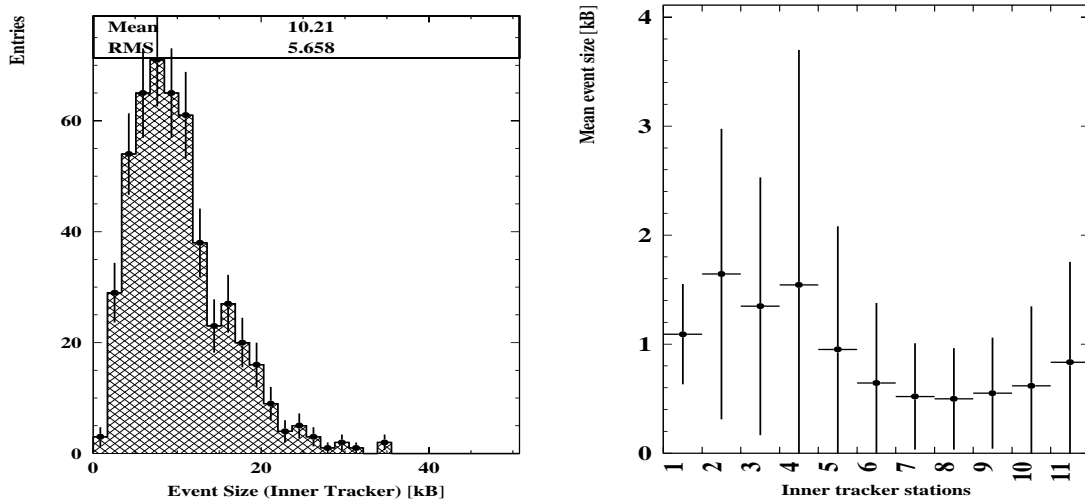
- **Number of channels** -220 K
- **Partitioning** - 11 stations (each with ~20K channels)
- **Min Occupancy** - to be confirmed%
- **Av Occupancy** - 1%
- **Max Occupancy** - to be confirmed%

Need Essential

Priority High

Stability Estimates under review as a function of simulation results

Source LHCb InnerTracker group(A Buijs,Andre T.)



The plots above show the variation, event by event, of hits in the Inner Tracker. We assume 4 byte hit coding (2 byte address, 2 byte data). In the case of the MSGC we must allow, as for the outer tracker, for reading out 2 buckets.

3.1.6 HCAL Readout

UR READ_HCAL HCAL is segmented into (Inner,Outer) parts. Event data is read from 2740 channels. The average number of hits is ~250. A hit is coded in 4 bytes. Average event size is ~1 kByte.

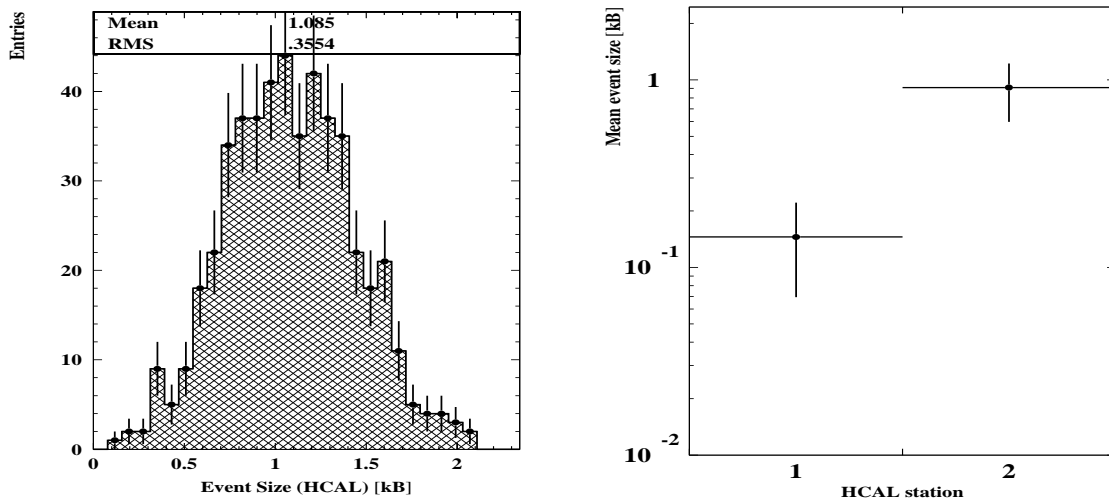
- **DETECTOR**
 - **Number of Channels** - 2740
 - **Partitioning** - 2 modules of 1370 channels
 - **Min Occupancy** - 1%
 - **Av Occupancy** - 10%
 - **Max occupancy** - 20%

Need Essential

Priority High

Stability Estimates under review as a function of simulation results

Source LHC-B HCAL group(A Konopliannikov)



We assume 4 bytes/hit (2 byte address, 2byte data).

3.1.7 ECAL Readout

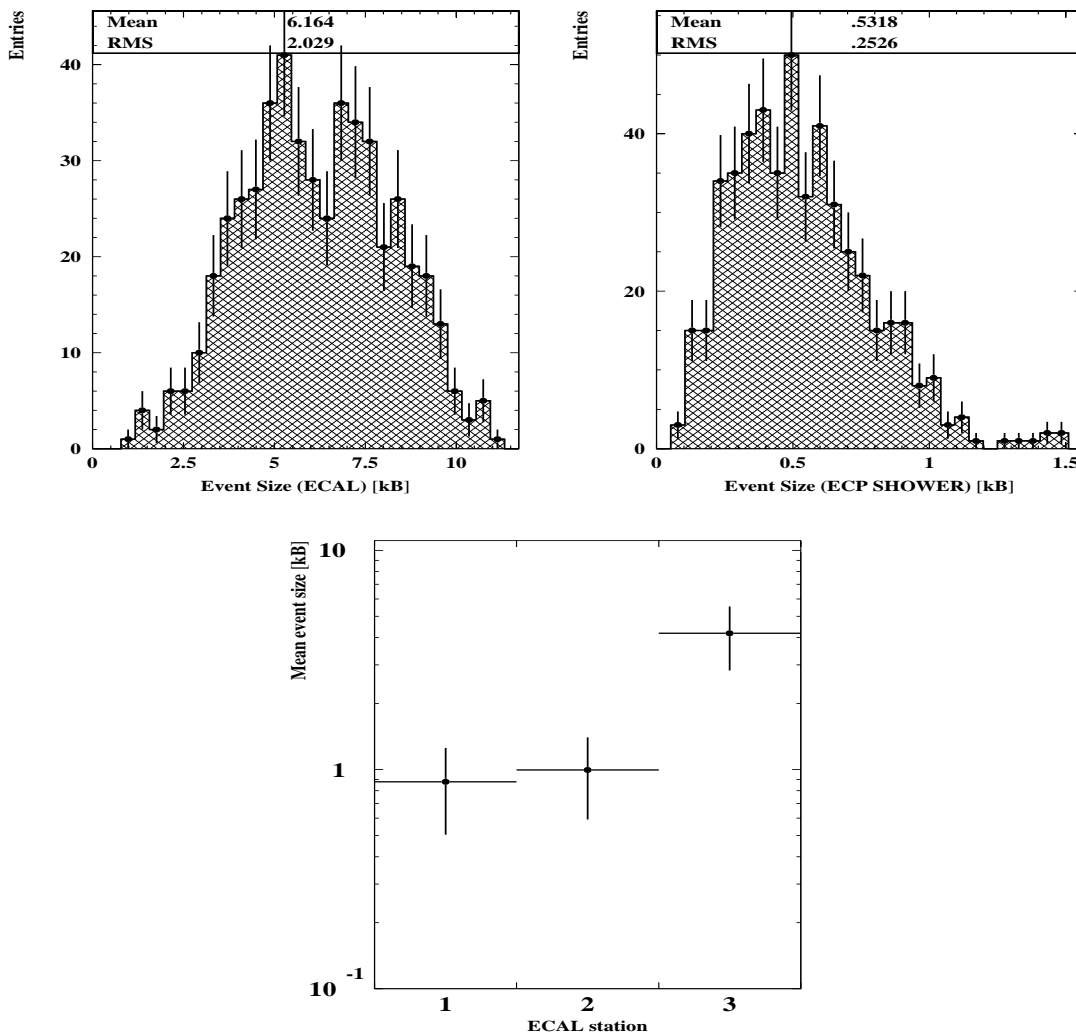
UR READ_ECAL ECAL and Pre-Shower Readout. Each has 6 K channels and is segmented into (Inner,Middle,Outer) parts. Both have hits coded in 4 bytes. ECAL has on average 1500 hits, giving an event size of 6 kByte. The pre-shower has, on average 130 hits, giving an event size of .5 kByte.

Need Essential

Priority High

Stability Estimates under review as a function of simulation results

Source LHCb ECAL group



We assume 4 byte coding/hit (2 byte address, 2byte data)

3.1.8 MUON Readout

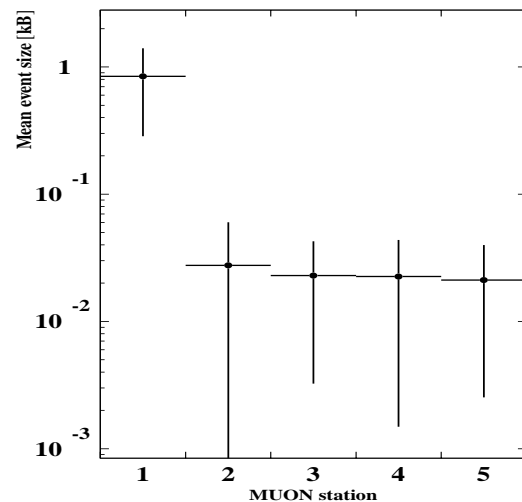
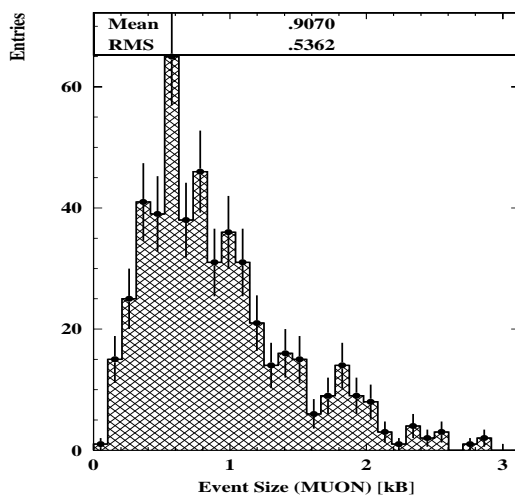
UR READ_MUON MUON Readout. Event data is read from 5 planes, the first being the special pad chamber, and the other 4 chambers in the muon detector itself. There are a total of 45K channels. A hit is coded in 4 bytes. On average there are ~250 hits, with over 200 in the special pad chamber. Average event size is 1 kByte.

Need Essential

Priority High

Stability Estimates under review as a function of detector design and simulation results

Source LHC-B Muon group(Andre+Brad)



We assume a 4 byte coding (2 byte address, 2 byte data) gives an average event size of 1 kByte

The substantial majority of the data is in the first pad chamber.

3.1.9 TRIGGER Readout

UR READ_TRIG

The results of the trigger, coming from Level-0, Level-1 and the overall trigger decision, must be read out by DAQ. A preliminary estimate is 5 kByte for the average event size. The content and format remains to be defined.

Need Essential

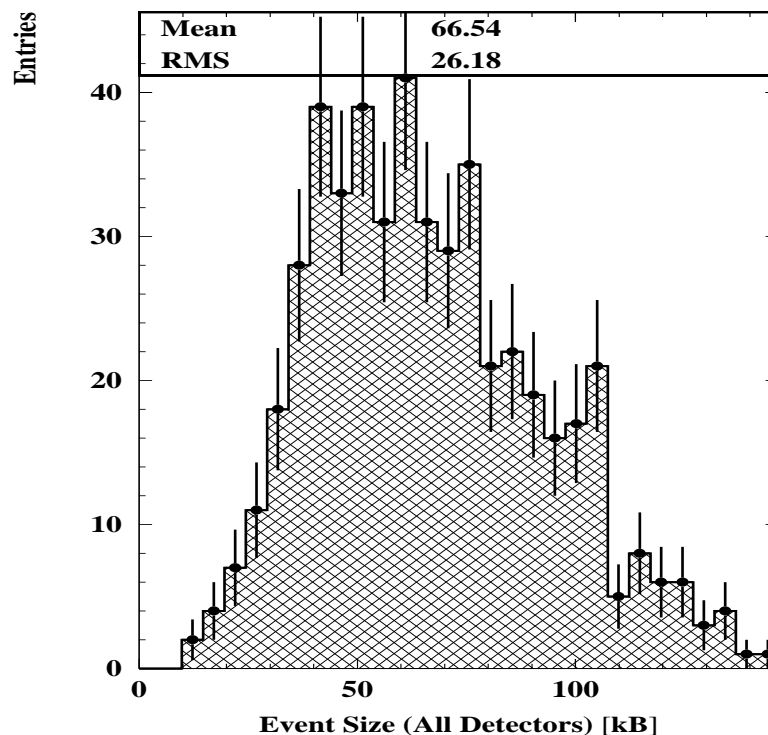
Priority High

Stability Estimates under review as a function of detector design and simulation results

Source LHCb Muon group(Andre+Brad)

3.1.10 Overall Readout Requirements

The following figure shows the variation of event size from a large sample of simulation data.



UR READ_SUM The following tables summarise the overall requirements for readout taking into account average event sizes and the physical organisation of sub-detectors. The table on 'Detector Channel Readout' shows an average event size of 67 kByte spread over 56 sub-detector segments where a segment is either a station or a (inner,middle,outer) section of a calorimeter as described in the sub-detector specific sections. The table on 'Sub-Detector segmentation and Link Allocation' has a notional allocation of 1 GBit links to read a sub-detector into DAQ. This folds the constraints of a sub-detector's physical segmentation into the allocation of link bandwidth requirements

Table 1: Sub-Detector Channel Readout^a

Sub-detector	Total Channels (K)	Average ^b Channel Occupancy %	Event Size (kByte)	Segments ^c
Vertex	220	0.4	4	17
Inner Tracker	220	1.0	10 ^d	11
Outer Tracker	110	4.5	24 ^e	10
RICH 1	140	2.0	11	2
RICH 2	200	0.5	4	2
Pre-Shower	6	2.5	1	3
ECAL	6	25.0	6	3
HCAL	3	10.0	1	2
Muon	45	0.5	1	5
Trigger			5	1
TOTALS	~950		67	56

- a. This table is based on event hit data given by the SICB simulation
- b. The average channel occupancy % is given as the percentage of readout channels to be readout following detector dependent thresholding and clustering
- c. For all sub-detectors a segment corresponds to a station, except for the calorimeters where the segmentation is into (inner,middle,outer). From the point of view of readout the trigger is treated as one segment combining the results of level-0 and level-1
- d. Includes the effect of having to read out 2 buckets
- e. As for d

Table 1: Sub-Detector segmentation and link^a assignments

Sub-detector	Event Size (kByte)	Segments (Stations)	Event Size per Segment (kByte)	1Gbit/s Links per Segment	Data ^b per Link (kByte)	Num of 1Gbit/s Links
Vertex	4	17	0.2	1	0.2	17
Inner Tracker	10	11	0.9	4 ^c	0.2	44
Outer Tracker	24	10	2.5	4	0.6	40
RICH 1	11	2	5.5	8 ^d	0.7	16
RICH 2	4	2	2.5	8	0.3	16
Pre-Shower	1	3	0.3	1	0.3	3
ECAL	6	3	2.0	4	0.5	12
HCAL	1	2	0.5	1	0.5	2
Muon	1	5	0.2	1	0.2	5
Trigger	5	1	5.0	10	0.5	10
TOTALS	67	56				165

a. The allocation of 'links' to sub-detector segments is done on the basis of physical organisation of detector, and of the bandwidth needed. Thus '1 Gbit links' could be made up of several physical links of lower bandwidth, or combined into links of higher bandwidth.

b. A 1 Gbit link at 50% average occupancy can handle fragments of 1.56 kByte at an average input rate of 40kHz. The allocations made here are conservative, with link average occupancies of 10-30%

c. In the case of tracking stations we have allocated one link to each station quadrant

d. In the case of RICH1 and RICH2 we have allocated 8 links to each silicon detector plane (2 planes each for RICH1 and RICH2)

3.2 Data Flow Protocols

We list below the major requirements the necessary protocols involved in trigger and timing control(TTC) signal distribution, and the control of dataflows according to running states. The requirements for the protocols involved in event building (including error recovery) are also listed.

3.2.1 Trigger and Timing Control distribution

UR TTC01 A TTC system will be used to distribute the clock, which is synchronised to the LHC machine, and also the Level-0 and Level-1 decisions to the frontend electronics.

Need Essential
Priority High
Stability Stable
Source LHCB TDAQ group

UR TTC02 The TTC needs to be configured by the DAQ system. The configuration will depend on the partition information.

Need Essential
Priority High
Stability Stable
Source LHCB TDAQ group

UR TTC03 The TTC will require to make its monitoring information available to other systems in the DAQ (trigger rates,dead-time, counters, etc.)

Need Essential
Priority High
Stability Stable
Source LHCB TDAQ group

UR TTC04 The TTC will require an interface to report errors detected within the TTC system

Need Essential
Priority High
Stability Stable
Source LHCB TDAQ group

3.2.2 Event Building (within DAQ)

UR EB01 Events should be built from fragments with the same trigger number and bam crossing number, which are checked at each stage in event building with timeouts for missing fragments.

Need Essential
Priority High
Stability Stable
Source LHCb TDAQ group

UR EB02 The input trigger rate must be controlled when the event building is getting overloaded. A backpressure should be applied in advance of data loss due to buffer overflows.

Need Essential
Priority High
Stability Stable
Source LHCb TDAQ group

UR EB03 The event building must support an average event size of 100 kByte read out at an average Level-1 rate of 40 kHz.

Need Essential
Priority High
Stability Stable
Source LHCb TDAQ group

3.2.3 Level-0 and Level-1 Triggers

The Level-0 and Level-1 information must be read out just like a sub-detector. In addition control and monitoring functions must be provided.

UR TRG001 Initialisation of the Level-0 system must be provided, including the definition of all trigger parameters.

Need Essential
Priority High
Stability Stable.
Source LHCB TDAQ group

UR TRG002 The DAQ system will be capable of reading the status of the Level-0 trigger system, and executing error recovery procedures as appropriate.

Need Essential
Priority High
Stability Stable.
Source LHCB TDAQ group

UR TRG003 The DAQ system will read the output of the Level-0 trigger for an event into the buffers provided for the Level-0 sub-system.

Need Essential
Priority High
Stability Stable.
Source LHCB TDAQ group

UR TRG101 Initialisation of the level-1 sub-system must be provided, including the definition of all trigger parameters.

Need Essential
Priority High
Stability Stable.
Source LHCB TDAQ group

UR TRG102 The DAQ system will be capable of reading the status of the Level-1 trigger sub-system, and executing error recovery procedures as appropriate.

Need Essential
Priority High
Stability Stable.
Source LHCB TDAQ group

UR TRG103 The DAQ system will read the output of the Level-1 sub-system for an event into the buffers provided..

Need Essential
Priority High
Stability Stable.
Source LHCb TDAQ group
Source

3.2.4 Interfaces to Level-2 and Level-3

UR TRG201 The DAQ system will provide buffers to allow for the latency of the Level-2 algorithms running at 40 kHz .

Need Essential
Priority High
Stability Stable
Source LHCb TDAQ group

UR TRG202 The DAQ system will provide access to the detector data according to requests from the level-2 algorithms.

Need Essential
Priority High
Stability Stable
Source LHCb TDAQ group
Clarity

UR TRG301 The DAQ system will provide buffers to allow for the latency of the level-3 algorithms running at 5 kHz average.

Need Essential
Priority High
Stability Stable
Source LHCb TDAQ group

UR TRG302 The DAQ system will provide access to the detector data according to requests from the level-3 algorithms.

Need Essential
Priority High
Stability Stable
Source LHCb TDAQ group

3.3 Data Processing

UR TRG203 The Level-2 algorithms require a total processing power equivalent to 1000 *1000 Mips processors..

Need Essential
Priority High
Stability Stable
Source LHC B TDAQ group

UR TRG303 The Level-3 algorithms require a total processing power equivalent to 400*1000 Mips processors.

Need Essential
Priority High
Stability Stable
Source LHC B TDAQ group

Table 2 HIGH LEVEL TRIGGER REQUIREMENTS - PROCESSING and EVENT BUILDING BANDWIDTH(using a 'phased readout' event building scenario)

Trigger level	Input Rate	Av Proc per Trigger	Number of (1000 MIPS) units	Percent of 100 kByte event needed	Event Building Power needed (GB/sec)
LEVEL-2	40 kHz	10 MI	400	40	1.6
LEVEL-3	5 kHz	200 MI	1000	60	.33
TOTALS			1400* 1000 MIPS		1.90 GB/sec

3.4 System Aspects

3.4.1 Partitioning

There is a general requirement to allow parallel and asynchronous running of different DAQ configurations each running with independent triggers. The requirements in their simplest form may be stated as follows.

UR PART01 It must be possible to run the “global” system with any configuration of sub-detector elements running from the same trigger (physics/cosmic/random test..).

Need Essential
Priority High
Stability Stable
Source LHC-B DAQ/Trigger group

UR PART02 It must be possible for an individual sub-detector configuration to run “local” tests from their own trigger source .

Need Essential
Priority High
Stability Stable
Source LHC-B DAQ/Trigger group

UR PART03 It must be possible to run in parallel a “global” partition with one or more “local “ partitions.

Need Essential
Priority High
Stability Stable
Source LHC-B DAQ/Trigger group

3.4.2 Modes of running

UR MODE01 It must be possible to support several modes of running for a partition, each involving different triggers. For example:

- Physics data taking
- Test triggers generated by the DAQ or detector groups(including calibration running)
- Cosmic triggers

Need Essential

Priority High

Stability Stable

Source LHC-B DAQ/Trigger group

3.5 Error handling

The DAQ system must satisfy the following minimum requirements

UR ERROR01 Data transmission and protocol errors must be detected both on front-end links and inside DAQ communications. As far as possible recovery procedures should be local.

Need Essential

Priority High

Stability Stable

Source LHC-B DAQ/Trigger group

UR ERROR02 Recovery procedures must be implemented if necessary to meet the overall event acceptance criteria. The loss of events due to transmission errors should be no more than 0.5 %.

Need Essential

Priority High

Stability Stable

Source LHC-B DAQ/Trigger group

UR ERROR03 Acceptable events are full events which have been built without any irrecoverable errors. There should be no bias as a function of event size.

Need Essential

Priority High

Stability Stable

Source LHC-B DAQ/Trigger group

UR ERROR4 A fast reset should be available for all internal buffers of the system to enable easy error recovery.

Need Essential

Priority High

Stability Stable

Source LHC-B DAQ/Trigger group

3.6 Calibration and Monitoring

Each detector has its own calibration procedures some of which put special demands upon DAQ. We give below these detector dependent requirements.

UR CAL_VERTEX The Vertex Detector needs to record calibration information for each channel at a frequency of about 1 sample/minute. Necessary information/channel is

- Pedestal (1 byte)
- Noise (6 bits)
- Status (4 bits)

Need Essential

Priority High

Stability Stable

Source LHC-B DAQ/Trigger group

3.7 Design Criteria

The principle criteria for the design and implementation are simplicity, ease of maintenance, scalability to meet new requirements, and the ability to follow developments in technology. These may be expressed in the following requirements :

UR GEN001 We will seek to use commercial components, with homogeneity in both software and hardware components.

Need Essential
Priority High
Stability Stable
Source LHC-B DAQ/Trigger group

UR GEN002 We must have scalability to follow changing experimental conditions. This will affect especially the choice of communications and processing components..

Need Essential
Priority High
Stability Stable
Source LHC-B DAQ/Trigger group

UR GEN003 Interfaces between sub-systems must be defined so as hide details of sub-system implementation. Thus we will avoid to lock ourselves into particular technologies for the lifetime of the experiment.

Need Essential
Priority High
Stability Stable
Source LHC-B DAQ/Trigger group

UR GEN004 One must be able to test and validate each component individually, and hence greatly simplify the integration and commissioning of the DAQ system.

Need Essential
Priority High
Stability Stable
Source LHC-B DAQ/Trigger group

3.8 Other Issues

MON : monitoring

UINT : user interfacing

SAF : safety

HARD : hardware commissioning

DTDB : Detector description

EVDB : Event store

LHC: Communication with LHC machine supervisory systems

TEST : testing

4 List of User Requirements

- UR READ01** All sub-detectors must follow the agreed definitions for the specifications of the Level-0 pipeline buffer, Level-0 derandomiser buffer, Level-1 FIFO buffer and the Level-1 derandomiser buffer. 14
- UR READ02** All sub-detector Level-0 data, on a Level-0 accept, must be read out into the Level-1 digital FIFO buffers within 1 microsec. 14
- UR READ03** All sub-detector data, on a Level-1 accept, must be pre-processed and multiplexed in order to put zero-suppressed data, in an agreed protocol, onto high bandwidth links leading to DAQ. 14
- UR READ04** The trigger number and beam crossing number must be added into each event fragment. In order to allow proper synchronisation of event building null fragments should be generated when the sub-detector element has no data..... 14
- UR READ_VERTEX** VERTEX Readout - There are 17 stations of 13K channels each. On average there are ~600 clusters to be read out spread over the 17 stations. A cluster is coded in 6 bytes. The average event size, without noise, is ~4kByte. 15
- UR READ_RICH** RICH Readout . Event data is read from RICH1(140K channels) and RICH2(200). On average there are ~2700 hits in RICH1 and ~1000 in RICH2. Hits are coded in 4 bytes. Average event sizes are ~11 kByte and ~4 kByte for RICH1, RICH2 respectively..... 16
- UR READ_OTRK** OTRACK Readout. Event data is read from 109K channels, spread over 10 stations. An event gives ~4750 hits, on average, spread over the 10 stations. A hit is coded in 4 bytes. Since electronic delays are greater than 25 ns. we must read data for 2 beam crossings. This increases the average event size to ~24 kByte..... 17
- UR READ_ITRK** ITRACK Readout - We read from 11 stations. The preferred technology for stations 1-4 is silicon, and MSGC for stations 5-11. For the MSGC we must read 2 bunch crossings. The average number of hits for an event is ~2000. A hit is coded in 4 bytes. The average event size is ~10kByte 19
- UR READ_HCAL** HCAL is segmented into (Inner,Outer) parts. Event data is read from 2740 channels. The average number of hits is ~250. A hit is coded in 4 bytes. Average event size is ~1 kByte. 20
- UR READ_ECAL** ECAL and Pre-Shower Readout. Each has 6 K channels and is segmented into (Inner,Middle,Outer) parts. Both have hits coded in 4 bytes. ECAL has on average 1500 hits, giving an event size of 6 kByte. The pre-shower has, on average 130 hits, giving an event size of .5 kByte. 21

UR READ_MUON	MUON Readout. Event data is read from 5 planes, the first being the special pad chamber, and the other 4 chambers in the muon detector itself. There are a total of 45K channels. A hit is coded in 4 bytes. On average there are ~250 hits, with over 200 in the special pad chamber. Average event size is 1 kByte.....	22
UR READ_TRIG	23
	The results of the trigger, coming from Level-0, Level-1 and the overall trigger decision, must be read out by DAQ. A preliminary estimate is 5 kByte for the average event size. The content and format remains to be defined.	23
UR READ_SUM	The following tables summarise the overall requirements for readout taking into account average event sizes and the physical organisation of sub-detectors. The table on ‘Detector Channel Readout’ shows an average event size of 67 kByte spread over 56 sub-detector segments where a segment is either a station or a (inner,middle,outer) section of a calorimeter as described in the sub-detector specific sections. The table on ‘Sub-Detector segmentation and Link Allocation’ has a notional allocation of 1 GBit links to read a sub-detector into DAQ. This folds the constraints of a sub-detector’s physical segmentation into the allocation of link bandwidth requirements.....	24
UR TTC01	A TTC system will be used to distribute the clock, which is synchronised to the LHC machine, and also the Level-0 and Level-1 decisions to the frontend electronics.....	26
UR TTC02	The TTC needs to be configured by the DAQ system. The configuration will depend on the partition information.....	26
UR TTC03	The TTC will require to make its monitoring information available to other systems in the DAQ (trigger rates,dead-time, counters, etc.)	26
UR TTC04	The TTC will require an interface to report errors detected within the TTC system ...	26
UR EB01	Events should be built from fragments with the same trigger number and bam crossing number, which are checked at each stage in event building with timeouts for missing fragments.	27
UR EB02	The input trigger rate must be controlled when the event building is getting overloaded. A backpressure should be applied in advance of data loss due to buffer overflows.....	27
UR EB03	The event building must support an average event size of 100 kByte read out at an average Level-1 rate of 40 kHz.....	27
UR TRG001	Initialisation of the Level-0 system must be provided, including the definition of all trigger parameters.....	28
UR TRG002	The DAQ system will be capable of reading the status of the Level-0 trigger system, and executing error recovery procedures as appropriate.....	28
UR TRG003	The DAQ system will read the output of the Level-0 trigger for an event into the buffers provided for the Level-0 sub-system.....	28

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- UR TRG101** Initialisation of the level-1 sub-system must be provided, including the definition of all trigger parameters. 28
- UR TRG102** The DAQ system will be capable of reading the status of the Level-1 trigger sub-system, and executing error recovery procedures as appropriate. 28
- UR TRG103** The DAQ system will read the output of the Level-1 sub-system for an event into the buffers provided. 29
- UR TRG201** The DAQ system will provide buffers to allow for the latency of the Level-2 algorithms running at 40 kHz 29
- UR TRG202** The DAQ system will provide access to the detector data according to requests from the level-2 algorithms. 29
- UR TRG301** The DAQ system will provide buffers to allow for the latency of the level-3 algorithms running at 5 kHz average. 29
- UR TRG302** The DAQ system will provide access to the detector data according to requests from the level-3 algorithms. 29
- UR TRG203** The Level-2 algorithms require a total processing power equivalent to 1000 *1000 Mips processors. 30
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- UR ERROR4** A fast reset should be available for all internal buffers of the system to enable easy error recovery. 33

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- UR GEN004** One must be able to test and validate each component individually, and hence greatly simplify the integration and commissioning of the DAQ system. 34

A Trigger and Timing Control (TTC).

The TTC system will be used to distribute the clock, which is synchronised to the LHC machine, and Level-0 and Level-1 decisions to the frontend electronics. Assuming the RD12 TTC is used Level-0 will use Channel A for its decision, and Level-1 Channel B. The specific requirements on the TTC from LHCB are

- Assuming a lifetime of an event in DAQ of 1 sec an EV-ID of 20 bits is required
- LHCB requires to run any subset of detectors asynchronously and concurrently
- If Level-1 decisions in sequence then, depending on the tails of the Level-1 processing time distribution, then the instantaneous Level-1 rate can significantly exceed 1 MHz. In this case we may require a faster version of the channel bandwidth(e.g. double the bandwidth of 40 MB/sec.)
- If Level-1 decisions are out of sequence then 6-10 bits have to be transferred to allTTC receiver chips, the number of bits depending upon the average Level-1 processing latency. Channel B is unsuitable(only 8 bits), and so individually addressed frames have to be used. Again a higher speed version of the current 950 kHz rate may be required.

The TTC receiver chip should have 2 separate data paths, one for receiving trigger and timing information, and one for setup and diagnostic purposes. This latter path should be readable as well as writeable. (the protocol for the control path requires definition)

