

Cryogenic III-V and Nb electronics integrated on silicon for large-scale quantum computing platforms

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Quantum computers now encounter the significant challenge of scalability, similar to the issue that classical computing faced previously. Recent results in high-fidelity spin qubits manufactured with a Si CMOS technology, along with demonstrations that cryogenic CMOS-based control/readout electronics can be integrated into the same chip or die, opens up an opportunity to break out the challenges of qubit size, I/O, and integrability. However, the power consumption of cryogenic CMOS-based control/readout electronics cannot support thousands or millions of qubits. Here, we show that III-V two-dimensional electron gas and Nb superconductor-based cryogenic electronics can be integrated with Si and operate at extremely low power levels, enabling the control and readout for millions of qubits. Our devices offer a unity gain cutoff frequency of 601 GHz, a unity power gain cutoff frequency of 593 GHz, and a low noise indication factor ($\sqrt{I_D} g_m^{-1}$) of $0.21\sqrt{\text{Vmm}}\sqrt{\text{s}^{-1}}$ at 4 K using more than 10 times less power consumption than CMOS.

Quantum computers have demonstrated a superior computational capability compared to classical computers for certain tasks^{1–4}. To realize their full potential and solve real-world problems, quantum computers need to be large-scale systems, featuring millions to billions of qubits^{4,5}. In this context, among various physical qubit platforms, silicon-based qubits have emerged as a key platform due to their inherent scalability with techniques of the complementary metal-oxide-semiconductor (CMOS) industry⁶. Today, quantum computer based on silicon spin qubits is composed of qubits positioned at a very low-temperature stage and classical microwave electronics at room temperature for control and readout, and they are connected by very long coaxial cables (Fig. 1a (left)). This approach is feasible for a small number of qubits and is useful for demonstrating the concept of a quantum computing system. However, considering that qubit platforms require one or more control and

readout lines for each qubit, unlike conventional computers, it is practically impossible to implement thousands or millions of qubits using this approach due to the input-output difficulties and high loss caused by long coaxial cables.

To overcome this bottleneck, the idea of placing the control and readout electronics closer to the qubits was proposed as an intermediate solution (Fig. 1a (center))^{6–8}. Ultimately, similar to the evolution of conventional computers, it has been suggested to leverage advanced semiconductor processes to co-integrate qubits and control/readout electronics on the same chip (Fig. 1a (right)). In fact, recent research has focused on utilizing CMOS processes to integrate qubits and control/readout electronics onto a single chip^{9,10}.

However, one critical challenge is the power consumption of control and readout electronics. Qubits can only function within

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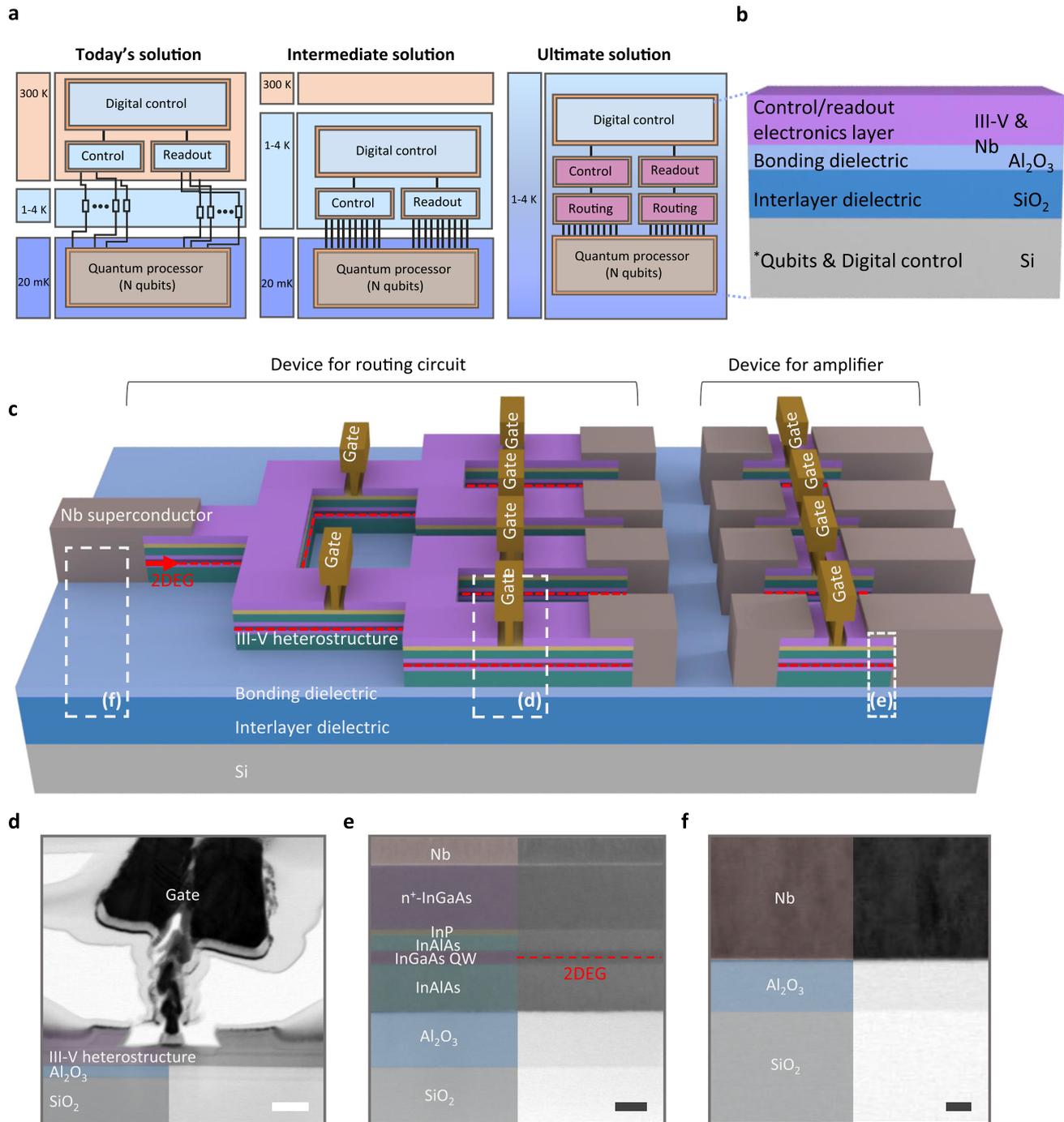


Fig. 1 | Concept of heterogeneous and monolithic 3D integration of III-V-based electronics on Si towards large-scale quantum computing solutions. **a** Present-day quantum computing systems are characterized by a qubit chip operating below 1 K, accompanied by classical microwave electronics functioning at 300 K. These classical microwave electronics, pivotal for control and readout functions, are connected to the qubits via lengthy coaxial cables. Placing control/readout electronics nearer to the qubit chip helps minimize the number of coaxial cables originating from room temperature. The ultimate solution for future large-scale quantum computing systems involves the integration of qubits and cryogenic control/readout electronics onto a single die. Given the constraints in cooling power, the imperative for extremely low-power cryogenic electronics, encompassing routing circuits and amplifiers, becomes evident. **b** Conceptual image of III-V/CMOS heterogeneous 3D integrated circuits to co-integrate qubits and control/readout electronics on the same chip. Although this work explored 3D integration in Si instead of CMOS, we anticipate that future studies will enable additional

functionalities, including integration with foundry-available CMOS-based qubits and digital blocks. **c** 3D schematic of the proposed cryogenic devices for amplifier and switch, utilizing III-V-based high-mobility two-dimensional gas (2DEG) channels and Nb-based superconductors integrated on Si. The devices for RF signal amplifiers consist of III-V high-electron mobility transistors combined with Nb superconducting material to achieve high-frequency, low-noise, and low-power operation. **d** Cross-sectional STEM image of III-V heterostructure with T-shaped gate, demonstrating a gate length of 70 nm. Scale bar, 100 nm. **e** Cross-sectional STEM image of III-V heterostructure with Nb on Si with Al_2O_3 (bonding dielectric), SiO_2 (interlayer dielectric). The InAlAs/InGaAs heterojunction with Si delta doping induces a two-dimensional electron gas (2DEG) in the quantum well (QW) InGaAs layer, providing remarkably high electron mobility at cryogenic temperature. Scale bar, 20 nm. **f** Cross-sectional STEM image of Nb global interconnect on Si with Al_2O_3 (bonding dielectric), SiO_2 (interlayer dielectric). Scale bar, 20 nm.

certain temperature limits, and the permissible power consumption at these temperatures is highly restricted, creating a significant power consumption constraint in quantum computing systems. Due to this issue, there has been active research into qubits that can operate at higher temperatures^{11–13}. Recently, spin qubits capable of operating at 4 K have been developed, slightly alleviating the power consumption limitation¹³. Nonetheless, to implement thousands or millions of qubits, extremely low-power control/readout electronics are essential. In more detail, to control and readout qubits, we must use an RF signal, typically in the GHz range. As a result, RF transistors should be used in control/reading electronics, configured as a single system in conjunction with a digital block that converts and processes RF signals into digital signals (Fig. 1a (right)). However, the power consumed for the RF signal amplification accounts for as much as 40% of the total system power when we use the CMOS technology¹⁴, posing significant challenges to the exclusive use of CMOS technology and it is the main challenge in reducing the power consumption of the total system.

Several technologies have been explored for ultralow-power cryogenic RF transistors, including SiGe-based heterojunction bipolar transistors (HBTs)^{15–17} and InP-based high-electron-mobility transistors (HEMTs)^{18–21}. SiGe HBT possesses a significant advantage in its integration capability with CMOS; however, it suffers from several issues such as high noise level and operating power characteristics compared with InP HEMT devices¹⁹. In contrast, InP HEMT demonstrates outstanding low-noise and low-power characteristics at cryogenic temperatures, making it the primary choice in contemporary quantum computers. Nevertheless, the lack of cryogenic III-V technology integrated with Si limits its utilization of CMOS-driven large-scale quantum computing applications.

In this Article, we report high-frequency, low-noise, and low-power cryogenic RF transistors and routing circuits by utilizing III-V-based high-mobility two-dimensional gas (2DEG) channels and Nb-based superconductors integrated on Si, which we conceptually presented in our previous work²². Here, we provide an extension in terms of results, analysis and implications over the previous work. The device is especially efficient at cryogenic temperatures as low as 4 K, where the resistance of 2DEG significantly decreases and the resistance of the Nb superconductor approaches zero. We show that the device can offer state-of-the-art cryogenic performances with respect to the unity current gain cutoff frequency (f_T) of 601 GHz, unity power gain cutoff frequency (f_{MAX}) of 593 GHz, and noise indicator ($\sqrt{I_D g_m^{-1}}$) of $0.21\sqrt{\text{Vmm}}\sqrt{\text{s}^{-1}}$ at 4 K. Notably, these performances are realized with power consumption an order of magnitude lower than conventional CMOS technologies, while being seamlessly integrated on Si. Furthermore, employing a groundbreaking routing circuit with 2DEG and Nb, we demonstrate the feasibility of extremely low-power electronics, which empower the utilization of several thousand qubits at 4 K. Our work establishes the foundation for scalable cryogenic control/readout platforms essential for large-scale quantum computing systems.

Results and discussion

Concept and device structure

Because of the cooling budget, only a small number of control/readout electronics are available in cryostats. Therefore, not only for devices that amplify RF signals, routing devices are necessary as well to control/readout a large number of qubits with a small number of cryogenic electronics. Figure 1b, c outlines the concept and structure of the devices. An III-V heterostructure and Nb superconductor are monolithically integrated on Si, and we used these materials to fabricate devices for amplifier and routing circuit. The techniques for the monolithic integration of different materials into Si are thoroughly explained in Supplementary Fig. 1, 2 and Methods. By employing III-V on Si technology through wafer bonding, even RF circuits can be implemented^{23,24}. The device for RF signal amplifier is composed of a HEMT with scaled T-gate (Fig. 1d) and an Nb-based superconductor (Fig. 1e). Among the wide variety of superconductors, Nb was selected

due to its superconducting properties at 4 K and its excellent compatibility with III-V materials, especially InGaAs, in terms of contact resistance (Supplementary Fig. 3). Furthermore, the Nb and InGaAs contact is expected to exhibit excellent device reliability due to its non-alloyed nature^{25,26}. Recently, research has progressed towards epitaxially growing Nb on III-V materials²⁷, further expanding its potential across quantum computing applications. The routing circuit also consists of III-V HEMT and Nb superconductor, but the key design approach using III-V 2DEG local interconnect and Nb global interconnect is applied. The III-V 2DEG is used for transistor-to-transistor connections (referred to as local interconnect) to eliminate the vertical transport resistance, which is the main bottleneck at cryogenic temperatures, leading to extremely low resistance and high scalability. Moreover, for the global interconnect, the Nb superconducting material is used to effectively remove the parasitic resistance, resulting in low-noise and low-power operation (Fig. 1f).

The subsequent discussion details how the careful design of III-V heterostructure and the introduction of Nb superconductors compatible for III-V materials enabled the development of high-performance cryogenic devices. These devices operate at 4 K with high-frequency, low-noise, and low-power consumption, achieving a figure of merit that significantly surpasses the current state of the art. This concept offers a promising route for future large-scale quantum computing systems.

Design and characterization of III-V heterostructure

III-V heterostructure should be carefully designed for low-power and low-noise operation at cryogenic temperatures. HEMTs are constructed based on heterojunctions of several III-V materials. Due to the InAlAs/InGaAs heterojunction with Si delta doping, 2DEG is formed in the quantum well channel with very high electron mobility ($40,000\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 4 K) (Fig. 2a). However, a vertical transport resistance component is inevitably created in the barrier layer, which is called barrier resistance (R_{barrier}). This component accounts for a large portion (about 60% or more) of the total resistance in the InGaAs HEMTs at room temperature^{28,29}. As the environment transitions to cryogenic conditions, this component becomes more dominant because of the change in major mechanism from thermionic emission to field emission (Fig. 2b). Notably, the extent of field emission is modulated by layer thickness. Consequently, optimizing barrier thickness is imperative for the minimization of the R_{barrier} .

To explore the practical impact of barrier thickness on the characteristics of III-V heterostructure at cryogenic temperatures, we designed epitaxial structures with barrier thicknesses of 18, 11, and 9 nm, while maintaining the other layers identical, as shown in Fig. 2c. The cross-sectional scanning transmission electron microscopy image of the three different III-V heterostructures can be found in Supplementary Fig. 4. The results of the characterization are summarized in Fig. 2d–f. The sheet resistances of 2DEG ($R_{2\text{DEG}}$) in our 3D integrated InGaAs HEMTs range from 91 to $132\ \Omega\text{sq}^{-1}$ at 4 K, which is slightly higher than the $R_{2\text{DEG}}$ for state-of-the-art conventional InGaAs HEMTs (20 to $90\ \Omega\text{sq}^{-1}$)^{20,25,30,31}, mainly due to backside interface, which requires further study to mitigate its impact in the future. Nevertheless, the $R_{2\text{DEG}}$ of $91\ \Omega\text{sq}^{-1}$ at 4 K is more than 10 times smaller than a typical high-doped Si semiconductor and a similar sheet resistance to Al metal of the same thickness. This is due to the fact that the electron mobility of 2DEG becomes higher at 4 K, which enables a higher frequency, and lower power and noise operation. However, the comparison of the R_{barrier} as shown in Fig. 2f reveals that the outstanding conductivity achieved by the InAlAs/InGaAs heterostructure with Si delta doping will be of little value unless the R_{barrier} can be suppressed. For non-optimized barrier thickness such as EPI-A as shown in Fig. 2c, the R_{barrier} at 4 K increases to over $1000\ \Omega\ \mu\text{m}$, which is equivalent to the resistance of a $10\ \mu\text{m}$ long channel on a 2DEG with a sheet resistance of $100\ \Omega\text{sq}^{-1}$. This demonstrates that the thickness of the InAlAs barrier has a dominant effect on R_{barrier} and, consequently, plays a

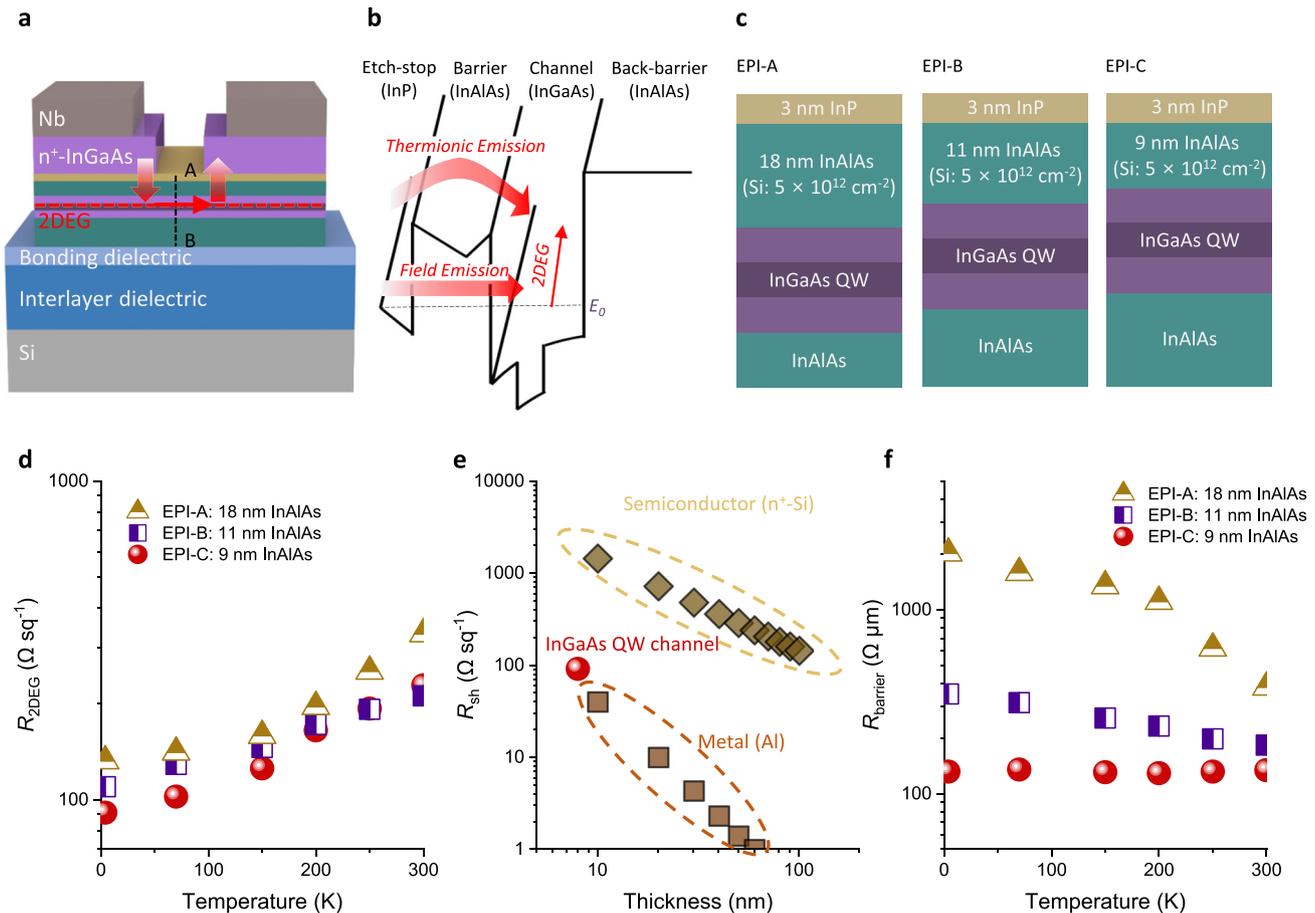


Fig. 2 | Design of III-V heterostructure for cryogenic devices. **a** Schematic of the III-V heterostructure on Si with Al_2O_3 bonding dielectric and SiO_2 interlayer dielectric. **b** Illustration of the conduction band of III-V heterostructure along the line AB in (a). Two different emission mechanisms (thermionic emission and field emission) are shown. At cryogenic temperatures, field emission is a dominant mechanism. **c** Three different III-V heterostructures with different barrier thicknesses. The InAlAs barrier thicknesses are 18, 11, and 9 nm, respectively, and all other layers are the same. **d** $R_{2\text{DEG}}$ versus temperature for three different III-V

heterostructures. **e** R_{sh} versus thickness at 4 K for III-V 2DEG and conventional metal (Al) and semiconductor ($n^+\text{-Si}$). R_{sh} of III-V 2DEG is more than 10 times lower than typical high-doped Si and comparable to Al metal of the same thickness. **f** Dependence of R_{barrier} on temperature in different III-V heterostructure. As the temperature decreases, the difference in the R_{barrier} attributable to variations in barrier thickness increases. This phenomenon is caused by a change in the mechanism at cryogenic temperatures and underscores the crucial role of barrier scaling at cryogenic temperatures.

crucial role in determining the overall device resistance at cryogenic temperature. Therefore, to ensure the effective operation of a scaling device with a sub-micron level, the R_{barrier} must be reduced to approximately $100 \Omega \mu\text{m}$. The III-V heterostructure with the scaled InAlAs barrier of 9 nm shows very low R_{barrier} values of $132 \Omega \mu\text{m}$. Such a low R_{barrier} can play a key role in enabling high-frequency, low-noise, and low-power operation at cryogenic temperature. In this context, the barrier thickness plays a critical role. A scaling barrier thickness allows a more effective field emission, allowing the low parasitic resistance at cryogenic temperature. However, over-scaling the barrier thickness can cause high gate leakage and generate additional noise, so designing an appropriate barrier thickness is very important, and the 9 nm barrier was used in this study. The detailed device characteristics depending on the III-V heterostructure can be found in Supplementary Fig. 5.

Cryogenic device for low power and low noise amplifier

The characterization of the III-V HEMT with Nb superconductor integrated on Si was conducted at 300 K and 4 K in a cryogenic probe station. The detailed measurement setup is described in Methods. All the results reported in the following refer to two-finger devices with gate length $L_G = 70 \text{ nm}$. For a fair comparison, currents were

normalized by the total width of the device. The transfer characteristics at low drain voltage (V_{DS}) of 50 and 100 mV are shown in Fig. 3a. When the temperature drops to cryogenic levels, the subthreshold swing (SS) of the device is improved and the off-current of the device decreases along with the decreasing gate leakage current (Supplementary Fig. 6). At 4 K, the minimum SS is 35 mV dec^{-1} at $V_{\text{DS}} = 50 \text{ mV}$, and the gate leakage current is in the order of $10^{-8} \text{ A } \mu\text{m}^{-1}$ during typical optimal low-noise operation of gate voltage (V_{GS}), which is small enough not to dominate the noise performance. The SS value of 35 mV dec^{-1} is not exceptionally low compared to previously reported cryogenic devices^{20,21,32,33}. This is attributed to fluctuations in the channel potential^{34,35}, which influence the level of disorder within the device, thereby impacting the SS of the device. This effect largely depends on the channel structure^{34,35}, making the design of an appropriate channel structure important for quantum computing applications. Figure 3b presents the transconductance (g_m) characteristics measured at V_{DS} of 50 and 100 mV. A greatly improved g_m of 0.8 S mm^{-1} is obtained at 4 K with a low V_{DS} of 100 mV compared to 300 K thanks to the increased mobility and the reduced parasitic resistance obtained by the optimized III-V heterostructure and Nb-based contact (Supplementary Figs. 3, 7). The small parasitic resistance and excellent mobility characteristics at 4 K can also be found in the

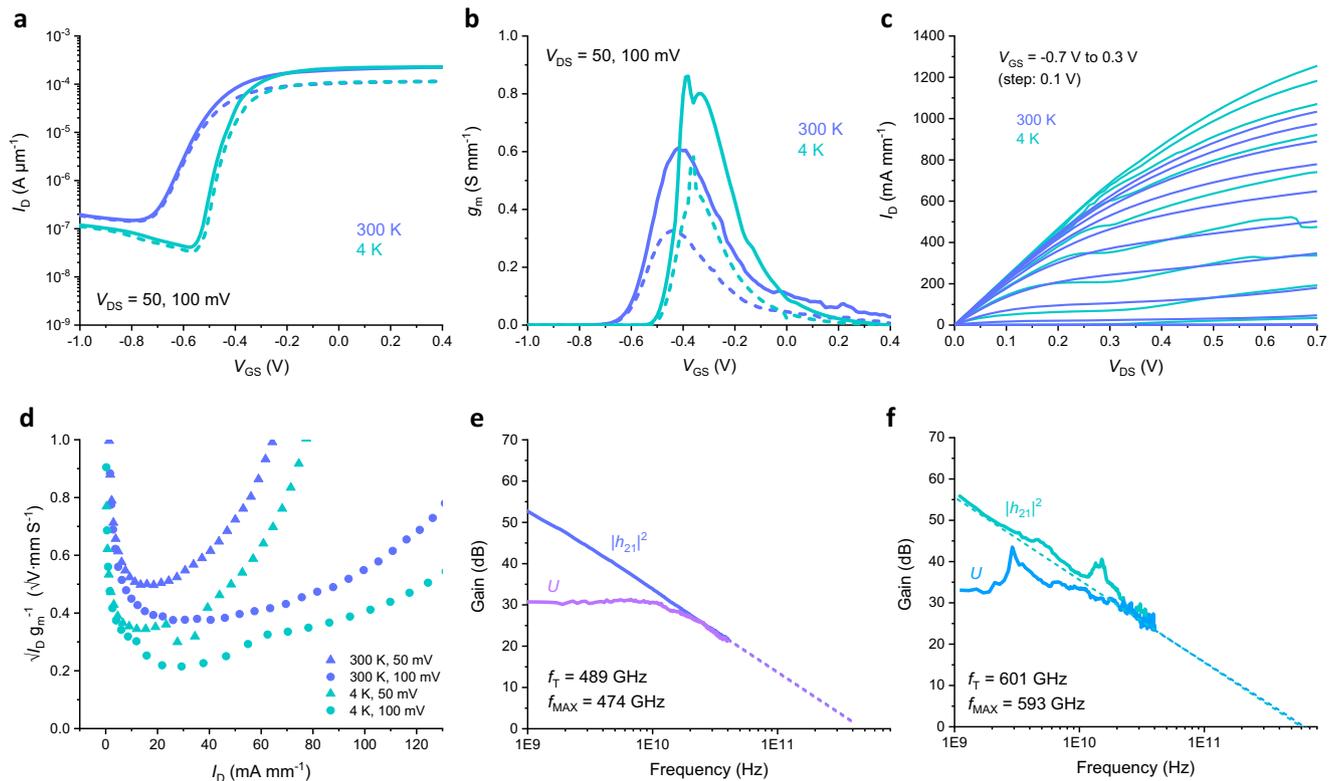


Fig. 3 | Electrical performance of cryogenic III-V HEMT on Si for low noise amplifier. Transfer (a) and transconductance (b) characteristics of III-V HEMTs on Si with L_G of 70 nm and W_G of $2 \times 20 \mu\text{m}$ measured at V_{DS} of 50 (dashed) and 100 mV (solid). The measurements were conducted at 300 K and 4 K. When cooled to 4 K, the device exhibits transfer characteristics with improved SS of 35 mV dec^{-1} at $V_{DS} = 50 \text{ mV}$. The positive threshold voltage (V_{TH}) shift is also observed. The device offers sharper g_m characteristics and a high peak g_m of 0.8 S mm^{-1} at 4 K for a low V_{DS} of 100 mV, compared to those observed at 300 K. This improvement at 4 K is attributed to enhanced 2DEG mobility and a reduction in parasitic resistance.

c Output characteristics of the same device, showing improved on-resistance and increased maximum current at 4 K. d Noise indication factor versus I_D of the device at a low V_{DS} of 50 and 100 mV. The measurements were conducted at 300 K and 4 K. The device shows a very low noise indication factor of $0.21 \text{ } 0.21 \sqrt{\text{Vmm}} \sqrt{\text{s}^{-1}}$ and the P_{DC} at minimum noise indication factor is only 0.8 and 2 mW mm^{-1} at $V_{DS} = 50$ and 100 mV. Gain plots of III-V HEMTs on Si with L_G of 70 nm and W_G of $2 \times 20 \mu\text{m}$ measured at 300 K (e) and 4 K (f). The measurements were conducted at V_{DS} of 500 mV and the optimal V_{GS} for each temperature. The f_T and f_{MAX} are extracted by extrapolating the h_{21} and U curves with -20 dB dec^{-1} lines.

output characteristics of the device measured over V_{GS} range of -0.7 to 0.3 V with 0.1 V steps (Fig. 3c), showing improved on-resistance (R_{on}) of $0.4 \Omega \text{ mm}$ and maximum drain current of 1225 mA mm^{-1} at V_{GS} of 0.3 V at 4 K. The low noise potential of the device can be clearly seen in a figure of merit called the noise indication factor ($\sqrt{I_D} g_m^{-1}$), which is particularly important for low-noise and low-power RF applications³⁶. The noise indication factor as a function of I_D is reported in Fig. 3d. At 4 K, the device exhibits a low noise indication factor of $0.21 \text{ } 0.21 \sqrt{\text{Vmm}} \sqrt{\text{s}^{-1}}$ at I_D of 20 mA mm^{-1} . The I_D is a range of $15\text{--}20 \text{ mA mm}^{-1}$ for optimal low-noise operation, which is a very low current level and therefore suitable for low-power operation.

High-frequency characterization was also conducted at both 300 K and 4 K using vector network analysis (VNA). Prior to device characterization, on-wafer calibrations were performed to remove extrinsic effects from cables and probe station, ensuring precise results. The parasitic components related to the contact pad were also removed through a pad de-embedding process using open and short test patterns fabricated on the same substrate. Following this, the scattering (S)-parameters of III-V HEMTs on Si were measured. The current gain (h_{21}) and unilateral power gain (U) derived from the S-parameter are shown in Fig. 3e, f. The device exhibits f_T of 489 GHz and f_{MAX} of 474 GHz at 300 K. When the temperature drops to 4 K, the f_T and f_{MAX} are greatly enhanced to 601 and 593 GHz at a low V_{DS} of 0.5 V due to improved electron mobility and reduced parasitic resistance, as analyzed in the DC characteristics. These results demonstrate that III-V HEMT on Si-based cryogenic RF transistors not only outperform CMOS-based cryogenic RF transistors but also provide competitive performance when compared to conventional III-V-

based cryogenic RF transistors. Recently, researchers have been exploring optimal barrier, spacer, and channel structures to further enhance the 40 dB gain and 1.4 K average noise temperature of state-of-the-art InGaAs HEMT LNAs for quantum computing applications^{37,38}. Incorporating such optimized designs into this study could bring us a significant step closer to achieving large-scale quantum computing platforms. Moreover, because our device is integrated on Si, it can break the trade-off relationship between cryogenic performance and integration capability observed in conventional devices. In fact, our device can be integrated into cryogenic CMOS chip including digital blocks or qubit processors, and the potential of this approach has been demonstrated in previous studies through the implementation of heterogeneous and monolithic 3D integration of III-V and CMOS technologies^{39,40}.

Routing strategy with low power consumption

To implement large-scale quantum computing systems within the limited power budget of a cryostat, the development of cryogenic RF transistors that operate at very low power is crucial. However, simply reducing the power consumption of cryogenic RF devices may have limitations. Therefore, there has been active development of routing circuits designed to control and readout a large number of qubits with a small number of cryogenic devices. A routing circuit for large-scale quantum computing systems must meet multiple criteria: low power consumption, low noise, low insertion loss, and high isolation capability. Cryogenic routing circuits have already been demonstrated using various technologies such as CMOS and III-V^{41–46}. However, one of the limitations for conventional routing circuits is their large vertical

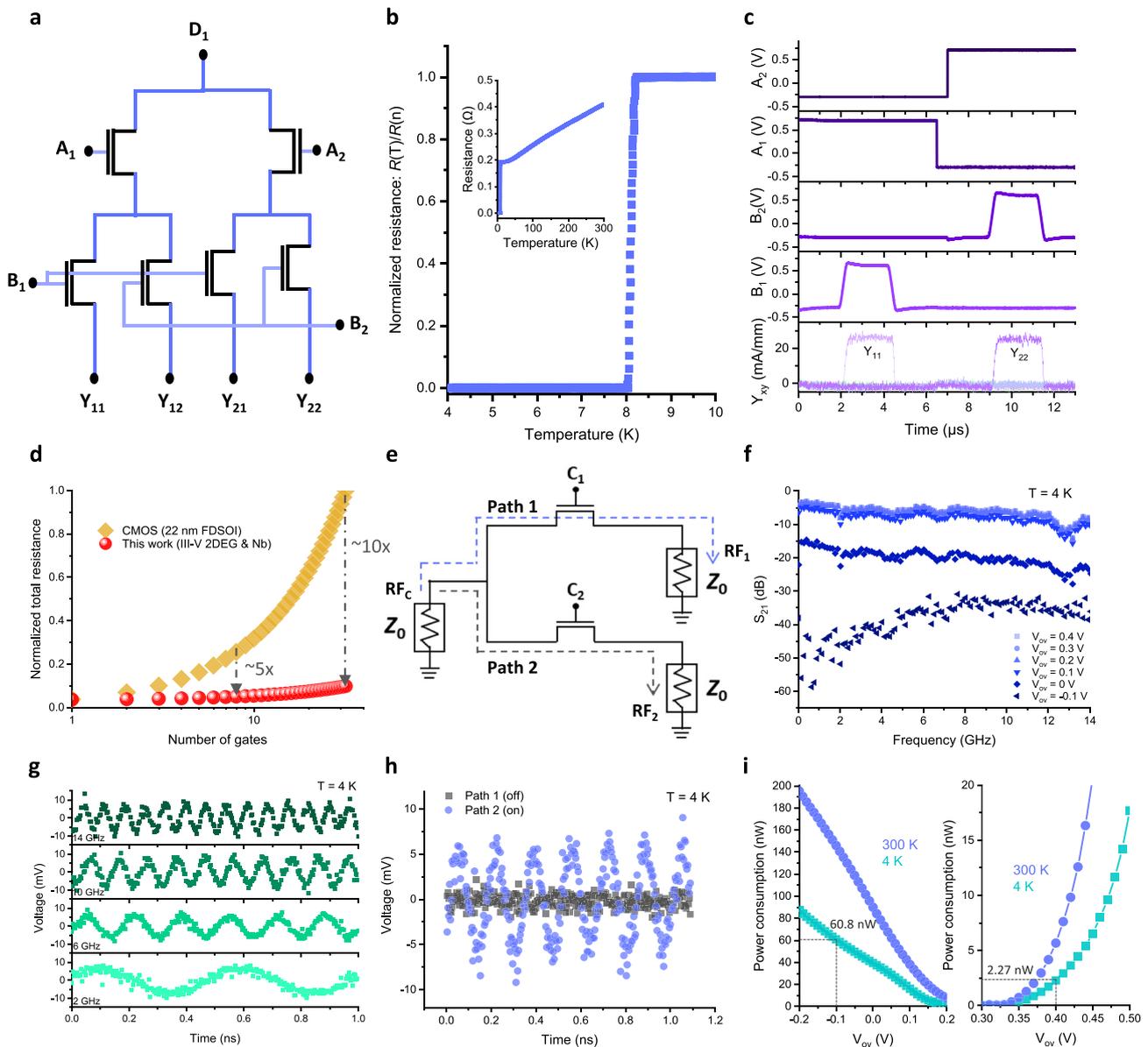


Fig. 4 | Cryogenic characteristics of III-V-based DC and RF routing circuits monolithically integrated on Si. **a** Schematic of 1-to-4 DC routing circuit diagram. There are one input and four outputs with four control gates (A_1 , A_2 , B_1 , B_2). **b** Resistance of Nb versus temperature (normalized to the resistance at 10 K), showing the transition temperature of 8 K. Inset includes resistance values measured up to 300 K. **c** Input-output waveforms under different input voltages, showing the functionality of the cryogenic routing. **d** Resistance benchmark for the presented routing circuits compared with conventional CMOS-based approach (22 nm FDSOI) in the case of scaled structure. The layout of the routing circuit is

found in Supplementary Fig. 8. The resistance is normalized to the resistance of a CMOS-based routing circuit with 32 gates. **e** Schematic of 1-to-2 RF routing circuit diagram. There are two RF output ports (RF_1 and RF_2) with one common port (RF_c). The C_1 and C_2 are control gates. **f** S_{21} versus frequency under different V_{ov} of the control gate. **g** Output waveform under different input signal frequencies. **h** Output waveform for a 6 GHz input signal with path 1 off and path 2 on. **i** Static power consumption as a function of V_{ov} measured at 4 and 300 K. The line represents the typical operation region with a V_{ov} range of -0.1 to 0.4 V.

transport resistance. The portion of the vertical transport resistance of the 1-to-8 routing circuit utilizing state-of-the-art cryogenic CMOS (22 nm FDSOI) is about 80% (Supplementary Fig. 8). It means that the vertical transport resistance is a main bottleneck in the routing circuits at cryogenic temperature. Therefore, reducing the vertical transport resistance or ideally removing the vertical transport resistance is the main key to developing highly scalable routing circuits.

To break this bottleneck, we designed the routing circuit using III-V 2DEG local interconnect and Nb superconducting global interconnect (Fig. 4a). More detailed cross-sectional structures of routing

circuits can be found in Supplementary Fig. 8. By replacing the local interconnect between transistors from metal to 2DEG, the vertical transport resistance can be effectively eliminated (Supplementary Fig. 8). On the global interconnect side, superconducting Nb is used to minimize the power consumed of electrodes and suppress the self-heating generated as a result. The superconductive transition of the Nb is depicted in Fig. 4b, occurring within the temperature range of 8 K. The operating temperature for the routing circuits is 4 K, at which the Nb global interconnect remains superconductive. The time-domain measurements are shown in Fig. 4c. Applying a constant voltage to the

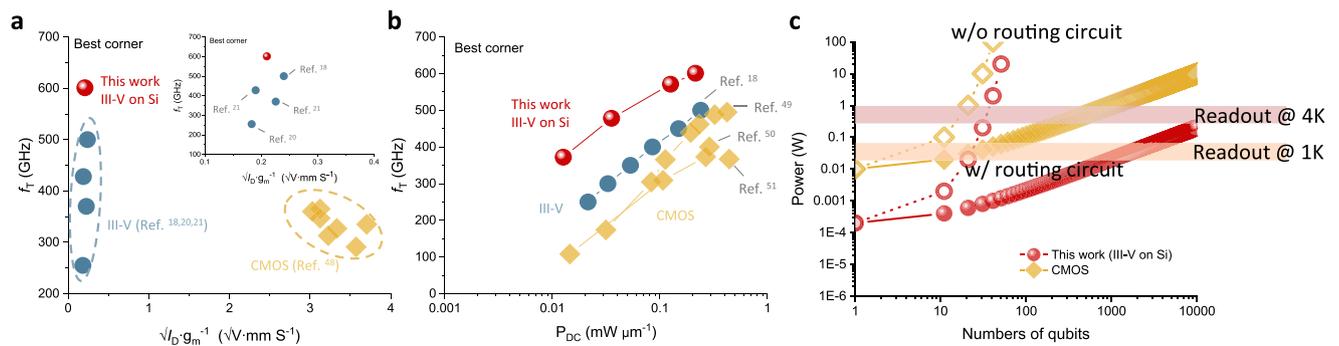


Fig. 5 | Achieving high-gain and low-noise cryogenic electronics using III-V on Si devices. f_T versus $\sqrt{I_D} g_m^{-1}$ (a) and f_T versus P_{DC} (b) benchmarks for state-of-the-art cryogenic RF transistors. The f_T and $\sqrt{I_D} g_m^{-1}$ are extracted at each optimum bias point, not at the same bias. Among the presented devices, our device is closest to the optimum corner region (highest f_T and lowest noise indication factor & highest f_T and lowest P_{DC}). Inset includes f_T versus $\sqrt{I_D} g_m^{-1}$ benchmark only for III-V. Data

from refs. 18,20,21,47–50. c Projected power consumption profiles for our device and CMOS depending on the number of gates and considering the presence or absence of routing circuits. The routing ratio is 1-to-10. Colored lines indicate the cooling power achievable with state-of-the-art dilution refrigerators, assuming 50% power consumption at the readout.

common port, on-state voltage to A_1 , off-state voltage to A_2 , and on-state voltage pulse to B_1 causes current to flow through the corresponding Y_{11} output. Conversely, applying the off-state voltage to A_1 , on-state voltage to A_2 , and on-state voltage pulse to B_2 results in current flow through the corresponding Y_{22} output. These show the proper routing operation in 1-to-4 DC routing. The projected total resistance of our approach and conventional CMOS approach for the same layout is reported in Fig. 4d. The layout used for the prediction can be found in Supplementary Fig. 8. The routing circuits with 2DEG local interconnect and Nb global interconnect demonstrate approximately a 5-fold reduction in resistance compared to the conventional structure in routing with 8 gates, and up to approximately 10-fold reductions for 32 gates (Fig. 4d). The larger the number of gates, the greater the effectiveness of our structure, suitable for large-scale quantum computing systems. This improvement is attributed to the zero resistance of superconductive global interconnect and significantly reduced local resistance achieved by introducing 2DEG without metal contact between the channels. As the scale of the quantum computer increases, the impact of this structure becomes more pronounced. Therefore, this architecture could provide a promising solution for a highly scalable routing system.

We developed not only DC but also 1-to-2 RF signal routing circuits. As presented in Fig. 4e, the RF signal is applied to a common port and divided into two paths. The path is selectively connected or isolated by using III-V 2DEG on Si. By applying bias on the control gate, the density of 2DEG is regulated, thereby changing the transmission of the RF signal (Fig. 4f). The insertion loss and isolation are 5.1 dB and 32.8 dB at 8 GHz. The switching ratio ($S_{21,\text{off}} - S_{21,\text{on}}$) is about 25 dB up to 14 GHz, representing the appropriateness for control of spin qubits⁴⁶. As shown in Fig. 4g, h, the time-domain response of the routing circuit is demonstrated by signal generator and oscilloscope. The routing circuit is not significantly affected by frequency changes in the frequency range of 2–14 GHz (Fig. 4g) and demonstrates excellent routing capabilities (Fig. 4h). The static power consumption, which accounts for most of the power consumption of the RF routing circuit, is measured (Fig. 4i). Due to reduced gate leakage at cryogenic temperatures, the switch can operate with less static power consumption. In the operating range of the switch (V_{ov} : -0.1 to 0.4 V), it has a low power consumption of up to 60.8 nW per switch.

Performance benchmark

For cryogenic devices used in large-scale quantum computing applications, high-frequency, low-noise, and low-power characteristics are of major importance. The trade-off between high performance (high

frequency, low noise, and low power) and scalability (integration capability and CMOS compatibility) is one of the main limitations of conventional cryogenic electronics. The state-of-the-art III-V HEMT-based cryogenic electronics, which are widely used in today's quantum computing system, exhibit high cutoff frequency, low noise, and low power consumption. However, they are not considered promising candidates for future large-scale quantum computing due to poor scalability and low compatibility with CMOS. On the other hand, CMOS-based cryogenic devices are very effective from a scalability perspective due to the active development of CMOS-based spin qubits and the potential for CMOS to enable the co-integration of qubit-control/readout electronics. However, they have the drawback of being difficult to achieve high performance. Figure 5a, b show the performance benchmarking of the III-V-on-Si-based cryogenic RF electronics compared with other approaches including III-V and CMOS that are available in the literatures. The f_T and $\sqrt{I_D} g_m^{-1}$ are extracted at their respective optimum bias point. For our device, f_T is extracted at V_{DS} of 500 mV and $\sqrt{I_D} g_m^{-1}$ is extracted at V_{DS} of 100 mV. This benchmark highlights two major aspects of our devices. First, our III-V-based devices integrated on Si significantly outperform CMOS-based cryogenic devices. The cutoff frequency is about twice as large, and the noise indication factor is approximately 15 to 20 times smaller (Fig. 5a). It is particularly important that these excellent characteristics are achievable at power consumption more than 10 times lower. Second, our device not only surpasses CMOS performance but also demonstrates enhanced performance compared to previously reported III-V devices^{18,20,21,47–50}. This significant improvement could arise from two main factors: (1) optimized III-V heterostructure with QW channel and barrier thickness, which can more effectively enhance the electron mobility and reduce the parasitic resistance at cryogenic temperature; (2) the Nb-based ohmic contact effectively reduces the contact resistance, which is more importance in scaling RF devices, improving high-frequency, low-noise, low-power characteristics. Of course, f_T and noise indicator do not directly represent the gain and minimum noise levels in an LNA circuit, but it is clear that our device has sufficient potential as a qubit signal readout device. In future studies, a comprehensive evaluation of the minimum noise after LNA fabrication will be necessary^{19,37,38}.

Based on the performance of cryogenic RF devices and routing circuits, we estimated the power consumption of readout electronics. Figure 5c shows the projected power consumption profiles for our proposed platform compared to a CMOS-only platform depending on the number of gates and considering the presence or absence of routing circuits. Assumptions include a routing ratio of 1-to-10 and 50%

power dissipation at the readout. Colored lines represent the cooling power provided by state-of-the-art dilution refrigerators. Our projections strongly demonstrate that: while using only CMOS technology to control and readout thousands of qubits is a practical approach, reaching tens of thousands of qubits or more likely necessitates the implementation of III-V-on-Si technology presented by this work.

We have demonstrated cryogenic electronics using III-V heterostructure and Nb superconductor, integrated on Si, for amplifying GHz range signal and signal routing. The capabilities and advantages of our devices result from the distinctive combination of a carefully designed III-V heterostructure and the introduction of the Nb superconductor, providing state-of-the-art cryogenic performance. Crucially, because our devices were demonstrated on a Si wafer using a heterogeneous and monolithic 3D integration method, it challenges the fundamental problem of conventional III-V technology, which is difficulty in integration with Si, thereby offering a path to highly scalable quantum computing systems. Given the effectiveness of our heterogeneous and monolithic 3D integration solution in accommodating multiple functionalities without performance degradation³⁹, more functionalities such as CMOS-based qubits (e.g., spin qubits) and control/readout electronics (e.g., analog-to-digital converters, digital-to-analog converters, and mixer) can be added to our approach.

Methods

Fabrication of heterogeneous and monolithic 3D integrated InGaAs HEMTs on Si

The process began with the fabrication of III-V on Si wafer. A schematic of the process flow is shown in Supplementary Fig. 1. The III-V heterostructure was grown on a semi-insulating InP wafer by molecular beam epitaxy. The III-V heterostructure contains both active layers grown in an inverted sequence and etch stop layers. The etch stop layers comprise InGaAs and InP layers. The active layers consist of a 40 nm n⁺-InGaAs contact layer, 3 nm InP etch stop layer, 9 nm InAlAs barrier with Si delta doping, InGaAs-based QW channel (In_{0.53}Ga_{0.47}As/In_{0.8}Ga_{0.2}As/In_{0.53}Ga_{0.47}As, 1/4/3 nm), and 30 nm InAlAs back barrier. We prepared the III-V wafer and Si wafer with cleaning steps. After cleaning steps, the 2- μ m-thick SiO₂ was deposited on Si wafer as an interlayer dielectric. Subsequently, both samples were loaded into atomic layer deposition (ALD) chamber at 250 °C for deposition of 20-nm-thick Al₂O₃ as a bonding dielectric. After the surface activation with O₂ plasma, the III-V wafer was bonded to the Si wafer by direct wafer bonding (DWB) process at 200 °C. Finally, the III-V on Si wafer was achieved by selectively removing the III-V substrate and etch stop layers by HCl and H₃PO₄:H₂O₂:H₂O solution.

Both the HEMT-based low noise-oriented RF devices and HEMT-based routing circuits were fabricated with same fabrication process. A schematic of the processing step is provided in Supplementary Fig. 2. The device area definition was conducted by H₃PO₄:H₂O₂:H₂O and H₃PO₄:HCl solutions. Following the removal of the native oxide by HCl: DI solution, Nb-based contact metal was deposited. Subsequently, we re-deposited the Nb as a global interconnect. The T-shape pattern was defined by double-exposure electron-beam lithography with the bilayer electron-beam resist stack composed of poly(methyl methacrylate) (PMMA) and poly(methyl methacrylate)-poly(methacrylate acid) (PMMA-PMAA). Prior to depositing the gate metal, the n⁺-InGaAs layer was etched using citric acid-based solution for gate recess. Then, the gate metal of Pt/Ti/Au was deposited. Finally, annealing was performed at 250 °C for 5 min. The devices for the RF amplifier, DC switch, and RF switch have gate width (W_G) of 40, 5, and 30 μ m, respectively, while the gate length (L_G) and source-to-drain spacing (L_{SD}) are all same as 70 nm and 2 μ m. Using the same integration process, we have demonstrated the heterogeneous and monolithic 3D integration of III-V HEMTs on Si CMOS without any degradation in the performance of the top and bottom devices and circuits³⁹.

Electrical characterization

Cryogenic temperature measurements were conducted using Lakeshore cryogenic probe station equipped with a cooled radiation shield to prevent the device from thermal radiation heating. The DC characteristics were measured using an on-wafer probe station with a Keithley 4200 and RF characteristics were measured using an on-wafer probe station with VNA, signal generator, and spectrum analyzer. The GSG probe and coaxial cables were calibrated using an off-wafer two-port open-short-load-thru method. Additionally, a standard de-embedding technique with on-wafer open and short patterns was utilized to remove the parasitic capacitance and inductance related to the contact pad.

Data availability

The datasets generated during and analyzed during this study are available from the corresponding author upon request.

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Author contributions

J.J. and S.K. conceived and developed the idea of the cryogenic III-V and Nb electronics integrated on Si. S.K. supervised the project. J.J. and J. K. designed the III-V heterostructure. J.J., S.K.K., Y.-J.S., N.R., and C.J.L. fabricated the devices. J.C. and Y.J. developed the Nb superconductor deposition and characterization. J.J., J.L., J.P., and S.-Y.P. built the cryogenic experimental setup and conducted cryogenic measurements. J.J., J.P.K., B.K., J.S., D.-M.G., and S.K. discussed and analyzed the measurement data. J.J. and S. K. wrote the manuscript with input from all authors.

Competing interests

The authors declare no competing interests.

Additional information

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