Monolithic Pixel Detectors in a Deep Submicron SOI Process

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Abstract

A compact charge-signal processing chain, composed of a two-stage semi-gaussian preamplifier-signal shaping filter, a discriminator and a binary counter, implemented in a prototype pixel detector using 0.20 μm CMOS Silicon on Insulator process, is presented. The gain of the analog chain was measured 0.76 V/fC at the signal peaking time about 300 ns and the equivalent noise charge referred to the input of 80 e^-.

Keywords: SoI; Monolithic Active Pixel Sensors;Charge Sensitive Amplifier; X-ray; Radiation Detection

1. Introduction

Semiconductor radiation detectors offer best functioning when charge collection is assisted by electric field present in a depleted volume. The detector wafers and readout chips are typically processed separately and connection is finally made using bump-bonding or similar process in order to provide advanced processing functionalities in each pixel. Extra material, increase of costs, limitations of achievable pixel pitches, etc. are the drawbacks of the hybrid choice. Monolithic Active Pixel Sensors (MAPS), realized in standard bulk CMOS processes, are an alternative to bump-bonding, but offer extremely limited signal processing capabilities and they cannot be embedded without tradeoffs.

The unprecedented opportunity for monolithical combination of the detector operation in depletion with advanced signal processing in each pixel is offered by Silicon-on-Insulator (SOI) processes. The adequate SOI process, featuring through Buried Oxide (BOX) layer contacts accompanied by donor and acceptor implants for formation of ohmic contacts and junctions in a high resistivity, equal to about 1 kΩcm, n-type handle wafer, was developed in collaboration with OKI Semiconductor Co. Ltd. within the SOIPIX collaboration led by KEK [1, 2]. A fully depleted (FD) CMOS SOI 0.2 μm process is the base for this development. The BOX is 200 nm thick and the through BOX contact is less than 0.5 μm in diameter.

A compact charge-signal processing chain was designed for the MAMBO (**M**onolithic **A**ctive **M**atrix with **B**inary C**o**unters) II prototype. The chip contains a matrix of 94×94 pixels and a few test structures with a fully functional single pixel as one

of them. The conceptual sketch of the imaging array is shown in Fig. 1. Each pixel features an analog block and a counter registering consecutive events. The counters from each pixel are transformable to a shift register allowing serially outputting data from the whole chip. The paper present, the design of the pixel and its evaluation that was achieved in tests, including stimulation with radioactive sources, viz. ^{55}Fe and ^{109}Cd emitting γ's of 5.9 keV and 22 keV, respectively.

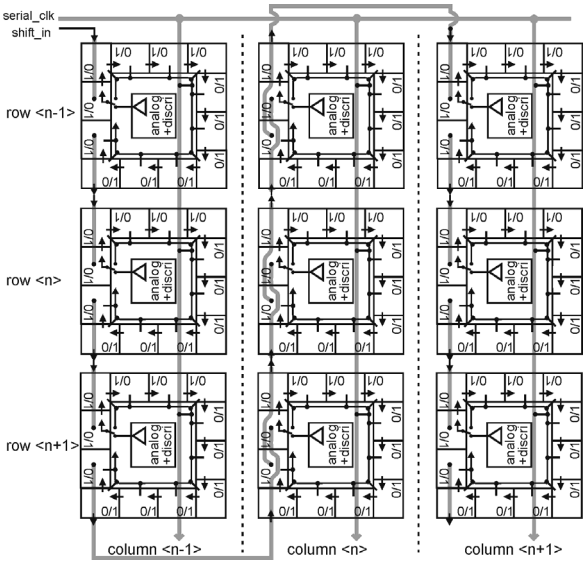

Fig. 2. Schematic diagram of the second stage of the preamplifier-shaper filtering circuit.

2. Pixel design

The pixel circuitry is a two-stage semi-gaussian CR-RC^2 amplifier-signal shaping filter with a discriminator and a 12-bit binary ripple counter. The first stage provides the charge gain of 10. It is capacitively coupled to the second stage. The design is optimized for the collection of holes. The first stage includes a trans-linear pole-zero cancellation (p-z) block [3], allowing elimination of output signal overshooting. The p-z block provides a DC path to the gate of the input transistor and is also an automatic compensation of the detector leakage current. The second stage is equipped with a simple baseline restorer. The purpose of its use is to reduce DC-level dispersions at the input of the discriminator. The overall gain of the chain is maximized to bring the expected dozen or so millivolt [4] offset dispersions of the discriminator below the electronic noise floor of the amplifier. The first stage is shown in Fig.2. The circuit is based on a simple common source (CS) structure with the input transistor, M_{a7}, biased at a single-μA current. Bandwidth limitation of the CS stage by a capacitance, realized with the transistor M_{a6}, places one pole of the transfer function in the first stage. The initial bias point of the preamplifier is set by a small, pA-level, current sourced by the transistor M_{a5} into the p-z circuitry.

The second stage, also based on a CS structure is shown in Fig. 3. The dimensions and the bias currents of the transistors M_{a7} and M_{s1} are scaled to result in

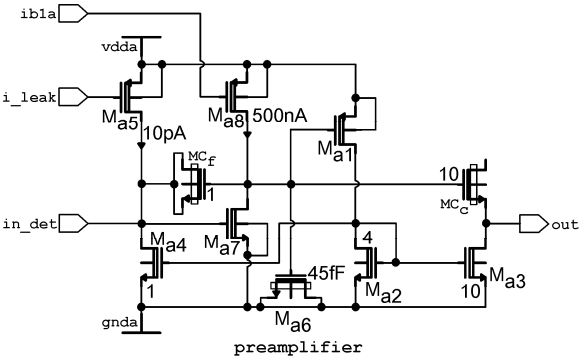

Fig. 2. Schematic diagram of the first stage of the preamplifier-shaper filtering circuit.

equal DC voltages at the inputs of both stages. The feedback capacitance and resistance are obtained with the transistors, MC_{fs} and MR_{fs}, respectively. A small current imposed by the transistor M_{s5} summed with

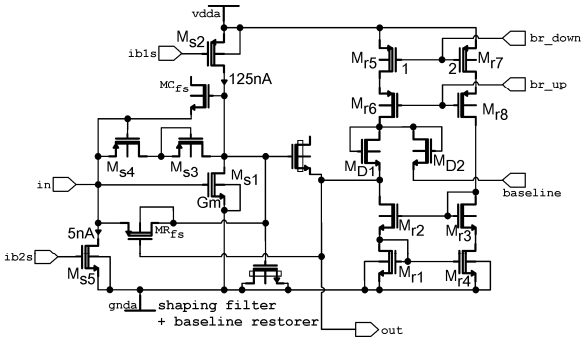

Fig. 3. Schematic diagram of the second stage of the preamplifier-shaper filtering circuit.

the amplified in the first stage leakage current (that is nevertheless very small), sets the channel conductance, $g_{ds}|MR_{fs}$. The required very high feedback resistance results from constant gate-to-source V_{GS} and bulk-to-source V_{BS} voltages of the transistor MR_{fs}. The pulse response, characterized by the shaping time τ_p=250 ns and the peak gain g=1.12 V/fC, is attained by selecting MC_c=28 fF, MC_{fs}=3.3 fF, MR_{fs}=50 MΩ, G_m=5.8 μS, M_{s6}=30 fF, leading to the match with the analytical CR-RC^2 filter formula. The two diode connected transistors, M_{s3} and M_{s4}, clip highest pulses for fast recovery to the baseline to avoid saturation. The transistor MC_{cs} provides capacitive coupling to the baseline restorer and assures constant non-zero V_{GS} voltage of the transistor MR_{fs}. All capacitors are realized with depletion NMOS transistors, except the feedback capacitor in the second stage. The depletion transistors are marked with extra empty rectangles in Fig. 2 and 3. The feedback transistor in the second stage uses a low threshold voltage (VT) NMOS transistor kept in inversion by enough voltage bias. High, marked by symbols with empty polygons, and low, marked by solid symbols, VT transistors were used to adjust operating points. Transistors with omitted body contacts are floating body. The discriminator is a differential amplifier with positive feedback. Additional source followers isolate the discriminator from the shaping filter. The counter is reconfigurable in a shift register for readout. The size of the pixel is 47×47 μm^2. The counter and 13 diodes occupy most of the pixel area. The diodes are connected in parallel, and they are distributed evenly in the pixel for equalization of the bias in the handle wafer underneath the BOX.

3. Pixel tests

No parasitic capacitance extraction existed at the design time, thus some adjustments were required during the tests. The analog gain was measured 0.76 V/fC at the signal peaking time of about 300 ns and the equivalent noise charge referred to the input of σ=80 e-. The transient responses to γ rays are shown in Fig.4. Sets of curves averaged over 25 event show the CR-RC^2 form of the response and suppression of gain for low and large signal, respectively. The power supply voltage was 1.8 V and bias currents were set at 1.1 μA, 0.26 μA and

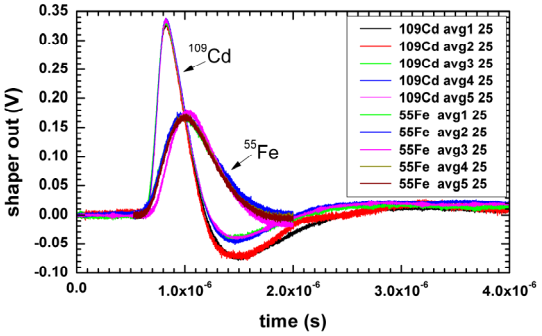

Fig. 4. Responses of amplifier to γ rays of 5.9 and 22 keV.

0.5 μA in the first, second, and discriminator stage, respectively. Examples of transient signals for different threshold voltages of the discriminator for a ^{55}Fe source are shown in Fig. 5. The reference voltage level was set to 0.4 V. The measurement curves correspond to threshold voltages varied from 0.425 V to 0.600 V, resulting in durations of discriminator pulses, Δt, ranging from 841 ns to

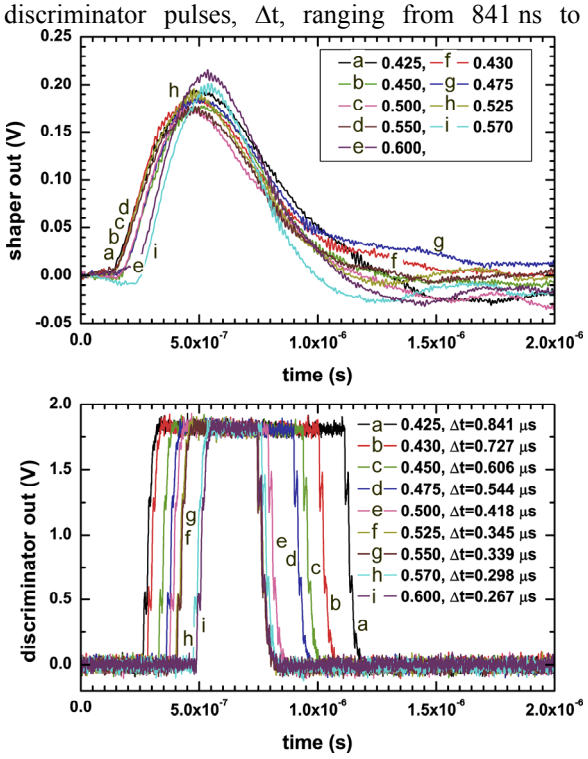

Fig. 5. Responses of the shaping filter and the discriminator.

267 ns, respectively.

The tests targeted also quantitative evaluation of

the mutual coupling of the electronics to the detector and properties of the handle wafer. The power supply of counters of about 1.3 V or more was causing instability of the amplifier due to the self triggering by charge injection following changes of the counter

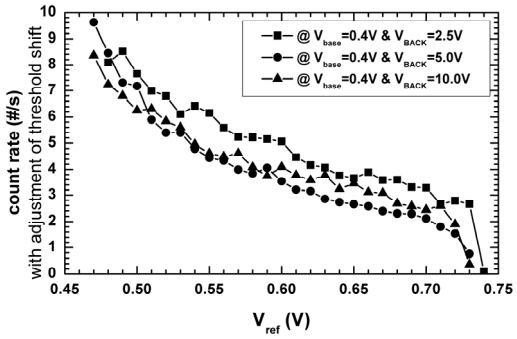

Fig. 5. Counting of 22 keV γ rays for different detector biases.

states. It was also discovered that the counting rate of 22 keV γs stayed almost unchanged despite of increasing reverse biasing of the detector. As it is illustrated in Fig. 5, the counting rate was only depending on the threshold voltage of the discriminator. The last reflects charge losses due to charge sharing between adjacent pixels. The voltages, V_{base}, V_{BACK} and V_{ref} are the voltages applied to the baseline restorer, bias voltage of the handle wafer and voltage applied to the reference input of the discriminator, respectively.

4. Conclusions

A processing chain for photon counting was successfully implemented in the 0.20 μm CMOS SOI process from OKI. The OKI process is a step toward a new generation of monolithic detectors. Tests indicate that further studies of mutual coupling between the electronics and detector are warranted along with research on alternate isolation techniques.

References

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