Technical Design Report for the Upgrade of the ALICE Readout and Trigger System | CERN-LHCC-2013-019 (ALICE-TDR-015)

ALICE
Technical Design Report

CERN-LHCC-2013-019

ALICE-TDR-015

Juliy 3rd, 2014

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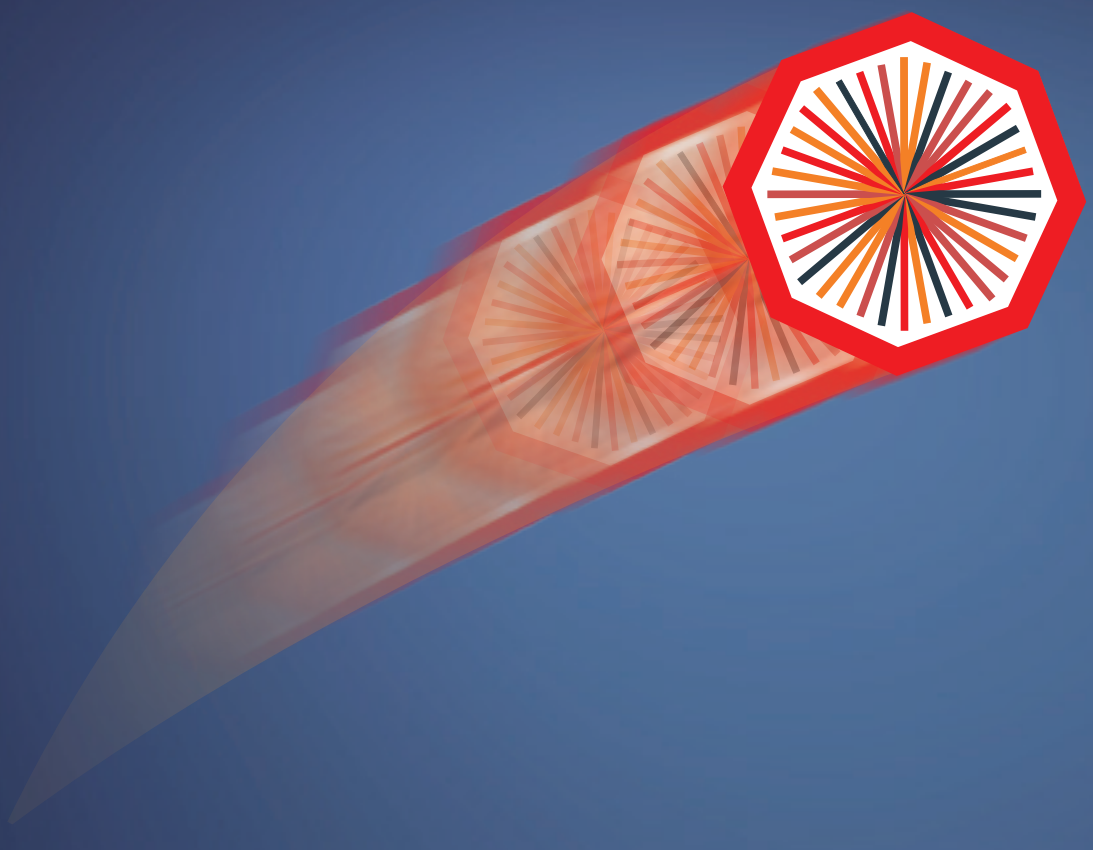
Upgrade of the **R**eadout & **T**rigger **S**ystem

Technical Design Report



ALICE-UG-TDR3

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Technical Design Report

for the

Upgrade of the ALICE Read-out & Trigger System

The ALICE Collaboration*

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Contents

1 Introduction and executive summary

1.1 Upgrade strategy

ALICE (A Large Ion Collider Experiment) is the detector at the CERN LHC dedicated to the study of strongly interacting matter, in particular the properties of the Quark-Gluon Plasma (QGP). The ALICE collaboration plans a major upgrade of the detector during Long Shutdown 2 (LS2), which is at present foreseen to start in July 2018. The scientific goals of this upgrade together with a basic description of the detector upgrade plans can be found in a Letter of Intent (LoI) [1], that was endorsed by the LHCC in September 2012.

The present ALICE detector is shown in Fig. 1.1, a detailed description of the detector can be found in [2] and the performance is summarised in [3]. ALICE will collect $1\,\mathrm{nb}^{-1}$ Pb-Pb collisions before LS2, at peak luminosities of $\mathrm{L}{=}10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, corresponding to a collision rate of 8 kHz. Hardware triggers based on event multiplicity, calorimeter energy and track p_T provide event selectivity that allows sampling of the full luminosity. The maximum read-out rate of the present ALICE detector is limited to 500 Hz of Pb-Pb events.

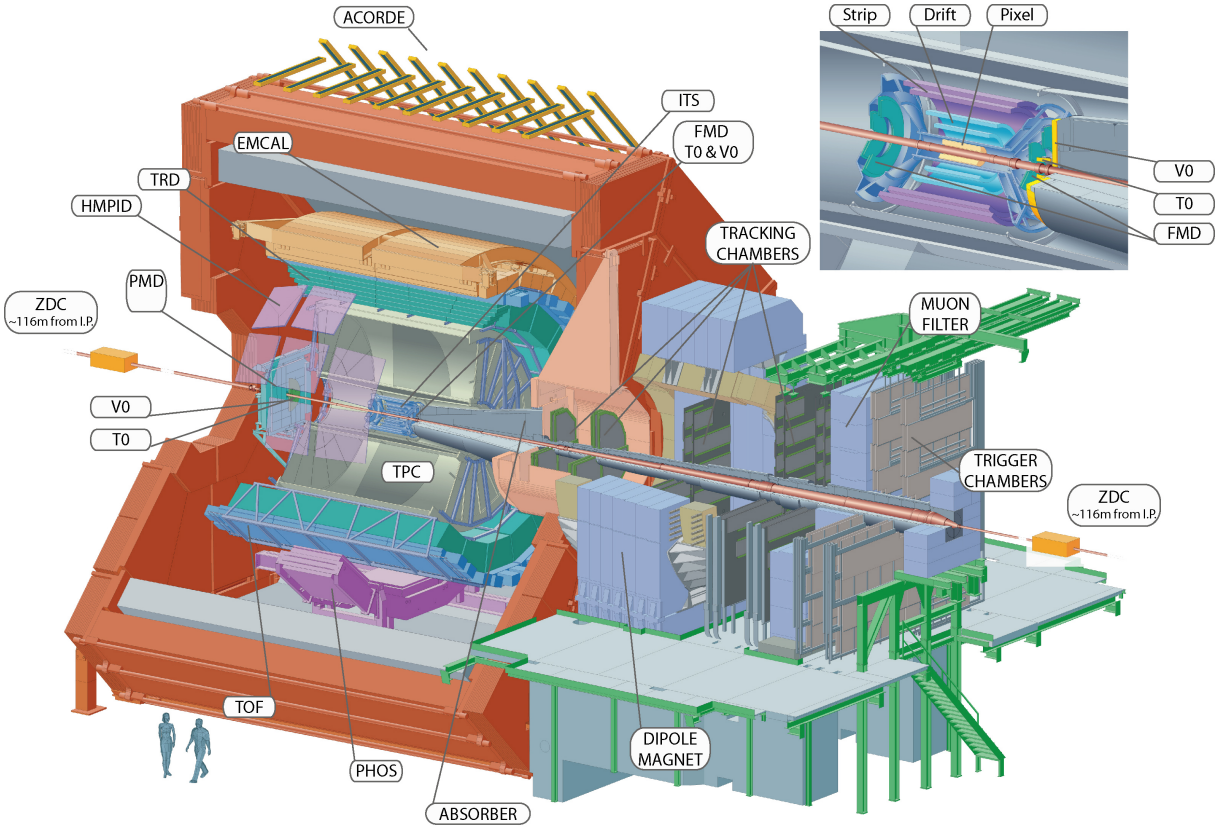


Figure 1.1: The present ALICE detector.

The physics objective of the upgrade is aimed at precision measurements of the QGP, which will be accessible through measurement of heavy-flavour transport parameters, quarkonia down

to zero p_T and low mass di-leptons. Since these processes do not exhibit signatures that can be selected by hardware triggers, they can only be collected by a zero bias (Minimum Bias) trigger. Additional physics topics include studies of jet quenching and fragmentations as well as the study of exotic heavy nuclear states.

The ALICE upgrade strategy is therefore based on collecting $>10\,\mathrm{nb}^{-1}$ of Pb-Pb collisions at luminosities up to $\mathrm{L} = 6 \times 10^{27}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ corresponding to collision rates of 50 kHz, where *each collision is shipped to the online systems*, either upon a Minimum Bias trigger or in a self-triggered, continuous fashion. The LoI considers in addition the collection of $6\,\mathrm{pb}^{-1}$ of pp collisions at the equivalent Pb-Pb nucleon energy as well as $50\,\mathrm{nb}^{-1}$ of p-Pb collisions, both at a levelled collision rate of 200 kHz. With this program, the statistics for the above mentioned physics topics will be increased by a factor of 100 over the numbers achievable with the present ALICE detector up to LS2.

The ALICE upgrade consists of replacing the present silicon tracker, upgrading the ALICE sub-detectors to read out 50 kHz Pb-Pb collisions and 200 kHz pp and p-Pb collisions at nominal performance, as well as implementing a new online system that is capable of receiving and processing the full detector information. Since the TPC drift time of $100\,\mu\mathrm{s}$ is 5 times longer than the average time between interactions, the presently employed gating of the TPC wire chambers must be abandoned and continuously sensitive read-out detectors using GEMs will be implemented.

In order to further enhance the sensitivity to charmed mesons and to make even the measurement of charmed baryons possible, an upgrade of the silicon tracker with significantly increased secondary vertex resolution and high standalone tracking efficiency will be implemented. Highly efficient triggering will be ensured by a new interaction trigger detector.

The idea of reading the full detector information, either upon a Minimum Bias trigger or in a continuous fashion, requires one single trigger signal based on an interaction trigger detector only. However, in order to keep flexibility and to allow trigger contributions for the elimination of possible background signals as well as triggers for calibration and commissioning, a Central Trigger Processor (CTP) delivering several trigger signals will be employed.

1.2 System upgrade overview

The specification for the ALICE detector upgrade is set by the collision rate of 50 kHz for Pb-Pb and a collision rate of 200 kHz for pp and p-Pb. The upgrade architecture is presented in Chap. 2, in particular the Common Read-out Unit (CRU) which will provide the interface between the on-detector electronics and the online computing system. As a baseline, the CRU units will sit in a counting room outside the radiation area and will receive data from the detectors through optical fibers.

The radiation load for the upgrade program is discussed in Chap. 3. For the sensors closest to the beampipe, one expects an ionising dose up to 1 Mrad and a fluence of 10^{13} hadrons/cm^2 in units of 1 MeV neutron equivalent.

The central trigger processor (CTP) will be upgraded to accommodate the higher interaction rate, providing trigger and timing distribution (TTS) to the upgraded detectors and backwards compatibility to detectors not upgrading their TTS interface. This upgrade is described in Chap. 4.

The present Inner Tracking System (ITS) is based on two layers of Silicon Pixel Detectors (SPD), two layers of Silicon Drift Detectors (SDD) and two Layers of Silicon Strip Detectors (SSD). This detector will be replaced by 7 layers of monolithic silicon pixel detectors, as described in the ITS conceptual design report [4] and the ITS technical design report [5]. The ITS will be able to provide read-out at rates of 100 kHz for Pb-Pb and 1 MHz for pp collisions.

The Muon Forward Tracker (MFT) consists of several discs of monolithic silicon pixel sensors, located in the forward region between the ITS and the frontabsorber. The LoI of the project [6] was endorsed by the LHCC in September 2013 and a TDR will follow at a later stage. The sensors and read-out will exploit a maximum synergy with the ITS detector.

The Time Projection Chamber (TPC) is presently based on a gated read-out with wire chambers. The electron drift time of 100 μs from the central electrode to the read-out chambers, together with the ion drift time of 180 μs from the sense wires to the gating grid, limits the read-out rate to less than 3.5 kHz. The TPC upgrade therefore foresees the replacement of the wire chambers with GEM detectors, that allow continuous operation to read out 50 kHz Pb-Pb collisions. The TPC electronics will push the digitised and time-stamped TPC data to the online systems in a triggerless mode. For calibration and commissioning purposes, a triggered mode of operation will be implemented as well. The TPC upgrade is described in a specific Technical Design Report [7].

The read-out of the TPC detector as well as the muon chambers (MCH) will be performed by a dedicated ASIC (SAMPA) that is presently being developed. The SAMPA chip will contain 32 channels and is based on the ALTRO [8] and S-ALTRO [9] developments. It will perform analog signal shaping, 10-bit digitisation at up to 20 MHz and digital signal processing. The output data are presented on 320 Mbit/s serial ports. This ASIC is discussed in detail in Chap. 5.

The Muon Chamber System (MCH) consists of a sequence of 5 wire chambers stations in the forward region of the experiment. It is presently limited to 1 kHz read-out rate and will change the entire read-out electronics using the SAMPA chip to digitise the detector signals. It will ship the data to the online system, either upon an interaction trigger or in continuous mode. This upgrade is discussed in Chap. 6.

The Muon Trigger detector (MTR) is at present providing the selection of high p_T single muon and di-muon events with a maximum trigger rate of 1 kHz. As the upgrade trigger strategy does not foresee a muon trigger, all events will be read upon the interaction trigger and the data are used offline for hadron rejection. Consequently, the detector will be called Muon Identifer (MID). This upgrade is presented in Chap. 7.

The Transition Radiation Detector (TRD) is presently limited to a few kHz read-out rate. Reducing the data volume from the detector by using tracklets and increasing the data throughput of the off-detector electronics, a trigger rate of 100 kHz for Pb-Pb and pp can be achieved. Since the front-end electronics does not support the use of multi-event buffers, a 100 kHz trigger rate corresponds to $\approx$ 60 % of events being read out. At 50 kHz Pb-Pb collisions $\approx$ 75 % of the events will be read out. Going beyond this number is not conceivable, because a change of the on-detector electronics would be needed, which requires a removal and disassembly of all TRD modules. The TRD upgrade is described in Chap. 8.

The read-out rate of the Time Of Flight detector (TOF) is at present limited to 40 kHz by the throughput of the VME system located in the crates at the end of the detector modules. An upgrade of this element will allow TOF to read out $>$ 200 kHz Pb-Pb events, which easily satisfies the requirements. The TOF upgrade is described in Chap. 9.

The V0/T0/FMD (Forward Multiplicity Detector) detector system will be replaced by a Fast

Interaction Trigger (FIT) detector, which will provide the Minimum Bias interaction trigger for the experiment. The FIT detector system will be located in the forward region of the ALICE detector at positions close to the present V0/T0 location. The FIT will consist of a new assembly of Cherenkov and scintillator detectors with > 99 % efficiency and < 30 ps time resolution for Pb-Pb events. The excellent time resolution is used for vertex selection with 1 cm resolution as well as start time for the TOF detector. Due to its proposed granularity, the detector will be also able to provide event plane determination. The trigger and read-out electronics of this detector system resembles closely the one of the present T0 system. The detector is described in Chap. 10.

The Zero Degree Calorimeter (ZDC) is located at a distance of 115 m from the interaction point and will change the read-out electronics to accept the increased trigger rate. It will also provide trigger information that can be used to clean the interaction trigger, as described in Chap. 11.

The Electro-Magnetic (EMC) and Photon Spectrometer (PHO) calorimeters use the same read-out electronics, which is being upgraded to 50 kHz operation already during LS1. This read-out will be also kept beyond LS2 and the implementation of this system into the upgraded read-out architecture is discussed in Chap. 12 and Chap. 13.

The High Momentum Particle Identifier (HMP) will not be modified and will therefore be capable of reading 2.5 kHz Pb-Pb and pp events. The implementation of this detector into the upgrade read-out architecture is discussed in Chap. 14.

The ALICE Cosmic Ray Detector (ACO) will not be modified, but is already capable of a read-out rate of 100 kHz. The implementation of this detector into the upgrade read-out architecture is discussed in Chap. 15.

The online system will receive the full detector information. Online calibration, event reconstruction and event data reduction will allow the writing of all the events to tape. The online systems are briefly discussed in Chap. 2 and will be described in detail in a future Technical Design Report.

2 Upgrade architecture

2.1 Introduction

The general approach for the ALICE upgrade is to read out all Pp-Pb events at the anticipated interaction rate of 50 kHz and read out pp and p-Pb events at an interaction rate of 200 kHz. The detector electronics, the trigger and the online computing system are designed to keep the nominal performance, even if noise or background is larger than anticipated.

The high interaction rate and the large event size result in a data flow of $\approx$ 1 TB/s from the detectors to the on-line system. Partial event reconstruction and data reduction in the online systems results peak data rate to storage of 80 GB/s. The continuous read-out of some detectors, the online calibration and the reconstruction will impose a paradigm shift in the online and offline computing [1, 10].

In the present system implementation, ALICE provides a framework of common read-out and trigger interfaces. The detector data link (DDL) [11, 12] provides a standard on-detector source interface unit (SIU) that connects the detector read-out electronics optically to the Read-out Receiver Cards (RORC) located in the DAQ computers. The trigger and timing distribution system is based on the TTC [13] architecture.

ALICE will expand the approach using standard system interfaces for the upgrade. The DDL will be upgraded to a higher bandwidth link and complemented with a common read-out unit (CRU). The CRU forms the interface between the detector front-end links and the DDL connecting to the online computing system (O^2). The CRU also receives the trigger and timing distribution (TTS) network. Depending on sub-detector specifications, detector data sent to the CRU are multiplexed, processed and formatted. The CRU on-detector interface is based on the GBT and optical versatile link [14] protocol and components. For detectors upgrading their TTS interface, the central trigger processor (CTP) will provide trigger information via a fast serial trigger protocol (FTL). For detectors not upgrading their interfaces, backwards compatibility to Run1 and Run2 systems is provided.

2.2 System architecture

Figure 2.1 shows the general ALICE read-out scheme. The CTP located in the cavern connects to the TTS via the Local Trigger Units (LTU), which, depending on detector system, are based on either fast serial trigger links (FTL) or TTC [13] links. The on-detector electronics systems connect via front-end links to either the ALICE common read-out unit (CRU) or when the read-out electronics is not upgraded to detector-specific read-out systems.

The read-out systems are connected to the online and offline computing system (O^2) and the detector control system (DCS) via the ALICE standard optical detector data link, which exists in three transmission speeds (DDL1, 2, 3). Three general read-out configurations exist:

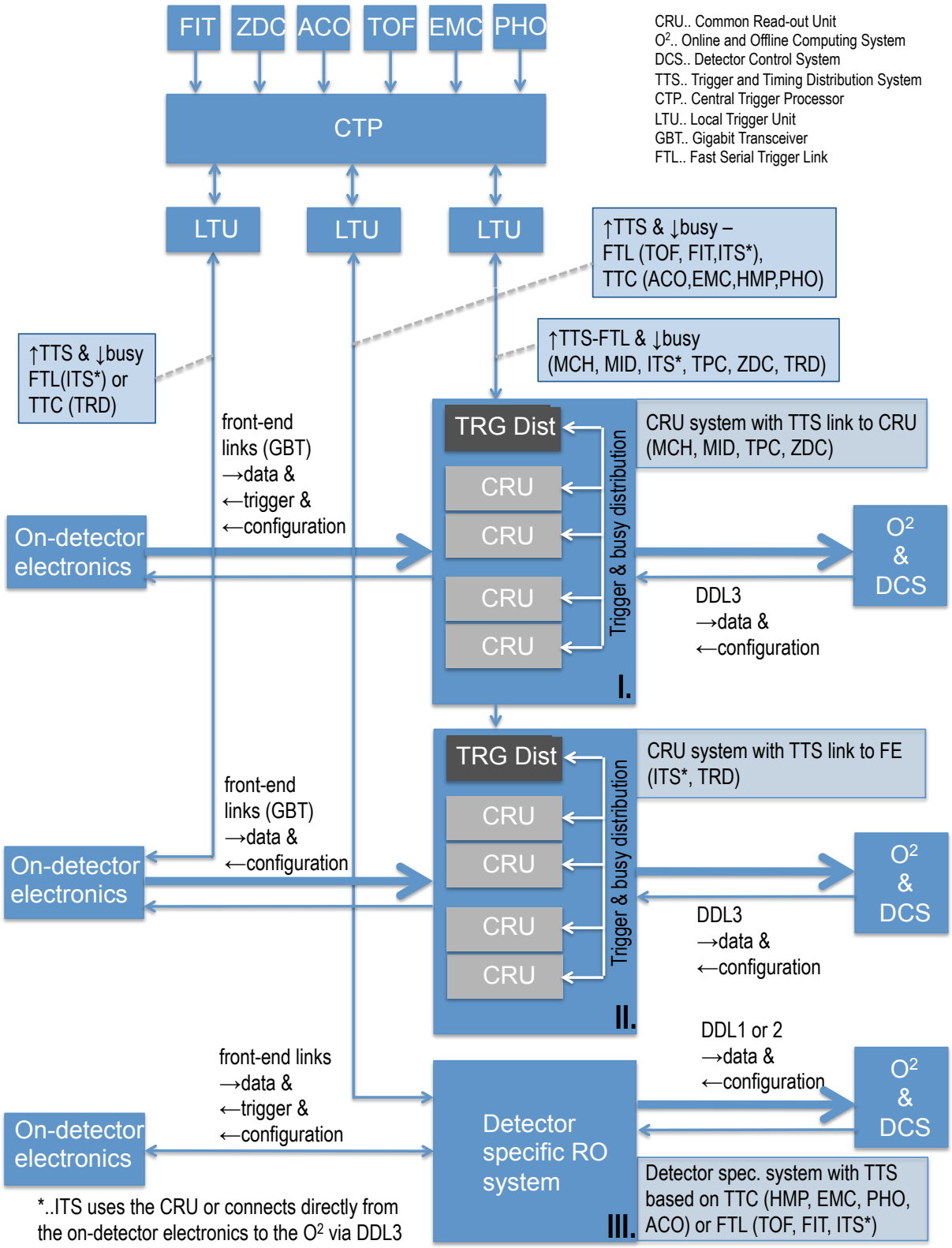


Figure 2.1: General ALICE system block diagram. Configuration I.: CRU is used as read-out processor and trigger distribution system. Configuration II.: CRU is used as read-out processor. The trigger distribution is done from the CTP/LTU directly to the on-detector electronics. Configuration III.: CRU is not used as the detectors do not upgrade their electronics and use detector-specific read-out systems.

Det	# channels	Run1&2 RO rate [kHz]	upgrade RO rate [kHz]	FE ASIC	FEC	ROC
TPC	5×10^5	3.5	50	17000 SAMPA	3400	CRU
MCH	10^6	1	100	33000 SAMPA	500	CRU
ITS	25×10^9	0.5	100	25000 ASICs	184	CRU
MID	21×10^3	1	100	FEERIC	234	CRU
ZDC	22	8	100		commercial&1 ZRC	CRU
TOF	1.6×10^5	40	100			72 DRM
FIT	160 + 64	80	100		upgrade	DRM(TOF)
ACO	120	100	100			
TRD	1.2×10^6	1	39			CRU
EMC	18×10^3	3.7	42			
PHO	17×10^3	3.7	42			
HMP	1.6×10^5	2.5	2.5			

Table 2.1: Run1 and Run2 read-out rates and hardware upgrade effort. (FEC..front-end controller, first data concentration stage, ROC..read-out card, data multiplexer, second data concentration stage and interface to O^2, ZRC..ZDC read-out card, DRM..TOF Data read-out module, SAMPA..TPC/MCH front-end ASIC, FERIC..MID front-end ASIC.)

- In one configuration, the LTU uses the fast serial trigger link protocol to transmit the timing and trigger information directly to the counting room-located CRUs via a trigger distribution module and the back plane of the CRU crate. The CRU modules forward the data to the detector front-end electronics via the GBT front-end links (see fig. 2.1, configuration I.).

- The second configuration is used for detectors which need a minimum latency trigger path and also uses the CRU for the read-out. The LTUs connect the TTS links based on fast serial trigger protocol or TTC to the detector front-ends, bypassing the CRU (see fig. 2.1, configuration II.).

- The third configuration does not use the CRU to read out the detector. The detector-specific read-out systems use TTS links based on fast serial trigger protocol or TTC from the LTU and connect via DDLs to the O^2 (see fig. 2.1, configuration III.).

Table 2.1 shows an overview of the detector upgrade effort. The read-out rate before and after the upgrade is compared as well as the number of channels in the system and the components to be replaced for the upgrade is shown. Details are discussed in the corresponding sub-detector sections.

2.3 Trigger system

The upgraded ALICE trigger system supports the read-out of triggered and continuously read out detectors. Some sub-systems not upgrading their read-out electronics will not be capable of reading the full event rate. These detectors will therefore be read out whenever they are not busy. The information is merged with the data from the other sub-detectors in the online system.

Level	Trigger Input to CTP [ns]	Trigger output at CTP [ns]	Trigger decision at detector * [ns]	contributing detectors
LM	425	525	775	FIT
L0	1200	1300	1500	ACO, EMC, PHO, TOF, ZDC
L1	#6100	#6200	#6400	EMC, ZDC

Table 2.2: Latency and contributors of the different trigger signals. * = signal arrival time at detector not including internal distribution to front-end electronics (the values reported here are indicative: differences among detectors exist due to their actual location and more details are provided in the detector chapters when relevant). #= EMC L1 latency is based on Run1 implementation, which will be shortened for the upgrade.

Det	triggered by () = optional	Pb-Pb RO rate [kHz]	TTS FTL/TTC	CRU used
TPC	(L0 or L1)	50	FTL	y
MCH	(L0 or L1)	100	FTL	y
ITS	L0	100	FTL	*y
MID	L0 or L1	>100	FTL	y
ZDC	L0	>100	FTL	y
TOF	L0 or L1	>100	FTL	n
FIT	L0 or L1	100	FTL	n
ACO	L0 or L1	100	TTC	n
TRD	LM&(L0 or L1)	39	FTL&TTC	y
EMC	#L0&L1	42	TTC	n
PHO	#L0&L1	42	TTC	n
HMP	#L0&L1	2.5	TTC	n

Table 2.3: Read-out parameter overview for Pb-Pb beam operation at 50 kHz interaction rate. (* = depending on implementation the ITS on-detector electronics will either use DDL3s to connect to online computing system or GBT data FE-links to the CRU, # = these detectors need a trigger at L0 latency and can additionally use L1, FTL..fast serial trigger link.)

The CTP will provide three trigger signals. The latencies and possible contributors to the three trigger signals are shown in Tab. 2.2. The LM signal is produced by the fast interaction trigger detectors (FIT), with a latency that is compatible with the timing requirements of the TRD wake-up signal. At nominal operation, this is the only trigger contributor and L0, L1 are simply delayed copies of the LM signal. The L0 timing is chosen such that the EMC, PHO, TOF, ACO and ZDC trigger can be used as L0 contributors. The ZDC allows cleaning of the interaction trigger in case of excessive background signals outputs. A possible L1 contributor is the EMC jet trigger. The use of trigger signals by the different detectors is summarised in Tab. 2.3.

2.3.1 Heartbeat trigger

As the online system supports the continuous read-out of detectors, the event building is based on the assembly of data recorded during a time frame of configurable length common to all detectors. In order to minimise the number of events where data are spread across a boundary

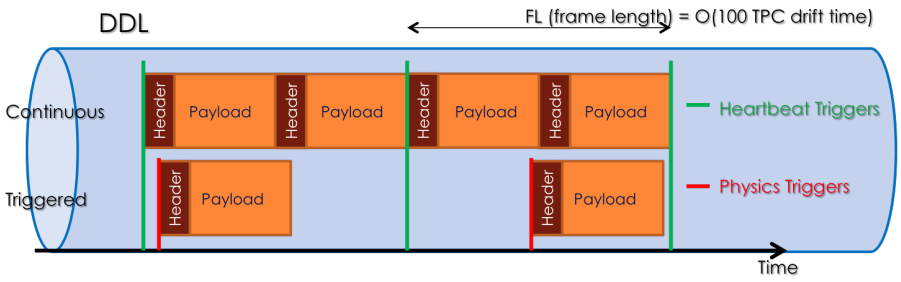


Figure 2.2: The usage of physics and heartbeat triggers for the continuous and triggered read-out.

of two consecutive time frames, the time frame duration will be made long compared to the TPC drift time. A value of at least 100 ms is foreseen.

The time frame boundaries are communicated to the detector read-out electronics via transmission of non-physics heartbeat triggers, allowing the separation of the data stream into pieces for the event building. The heartbeat trigger will be scheduled by the CTP to run with the highest possible priority and with a fixed period [15].

The detector read-out systems implement copies of the bunch crossing, orbit and trigger counters. The hardware compares these counters with the LHC counters only transmitted in full during a heartbeat event. In case of a discrepancy, the detector electronics re-aligns the counters and communicates the error to the online system. Each read-out unit will generate an heartbeat event containing no physics data but indicating the bunch crossing and orbit counter information at which the heartbeat trigger arrived. These events will be used by the online system for data segmentation, fault finding and recovery procedures. The detector electronics of the existing detectors will be modified to handle this combination of physics and heartbeat triggers.

Each read-out card will autonomously tag detector data using the local copy of the LHC orbit and the bunch crossing identification. For continuous read-out, the data will be sent as a continuous flow of successive time frames, each preceded with a header containing the time-based tagging and indicates error cases such as data truncation due buffer overflow. The triggered read-out will function in the same way as is presently the case: it will send a data block preceded with a header for every trigger, physics or heartbeat.

Figure 2.2 shows how the physics and heartbeat triggers will be used for the continuous and triggered read-out.

2.3.2 Trigger, Timing and Clock Distribution System - TTS

Depending on the detector implementation, whether the trigger latency is critical and whether the TTS interface is upgraded, three different TTS configurations are implemented. The distribution system for the upgraded detectors is based on fast serial trigger links between the CTP and the read-out electronics. For non-trigger latency critical systems, such as the TPC and MCH systems, the TTS connects the CTP to the off-detector read-out electronics (CRU), which takes care of distributing the trigger and timing signals to the front-end electronics. In case of latency critical systems, such as the ITS, the TTS connects the CTP directly to the on-detector electronics via optical fast serial trigger links. Those systems which do not upgrade their TTS interface will continue to use the TTC protocol. As a consequence, the upgraded CTP will offer two interfaces. One is based on a fast serial protocol and one is based on the TTC protocol.

The TTS bandwidth based on fast serial trigger links is sufficiently high to transmit the full trigger and timing information for each trigger (physics, software or heartbeat). For the present TTC system, the channel (B-channel) used for the distribution of trigger signals has a saturation rate of 150 kHz for 8 word messages and 225 kHz for 6 word messages. A reliable usage of the B-channel imposes a limit on the trigger rate to half of these values, which will not allow distribution of the full information for each trigger. Detectors which will continue to use the TTC system will receive for each trigger shortened information via the TTC B-channel. In the detector front-end electronics, local copies of the bunch crossing identification, the orbit counters and trigger counters are implemented, which are independently increased and attached to the data packets. The arrival of the heartbeat trigger with the full trigger information allows counter re-synchronisation and, if required, error flagging.

2.4 ALICE Detector Data Link - DDL

The present ALICE data collection is based on common interfaces between the detector read-out electronics and the online computing system: the Detector Data Link (DDL1) [11]. A second version of the link (DDL2) has been developed [12] and will be used by the TPC and TRD detectors during Run2. For the upgrade, a higher performance read-out solution will be selected.

The three generations of DDLs have different clocking speed and form factors. The DDL1 is clocked at 2.125 Gb/s and the DDL1 Source Interface Unit (SIU) is implemented as a radiation-tolerant daughter card plugged on the detector read-out card. The DDL2 SIU is implemented as an Intellectual Property (IP) core and can be clocked at 4.25 or 5.3125 Gb/s according to the capabilities of the detector electronics using it. The DDL3 aims at higher bandwidths using Gigabit Ethernet at 10 or 40 Gb/s or Infiniband (IB) at 56 Gb/s. The performance of the DDL1, of the two variations of the DDL2 and of a first DDL3 prototype based on Ethernet are shown in Fig. 2.3. As expected, for small data blocks the overall data rate is reduced. However, this is not considered an issue, as the detectors with large data rates will have sufficient large event sizes and thus large data block sizes. Furthermore, each DDL is controlled by an FPGA which assembles the data packet to be sent over the DDL. This FPGA has sufficient large buffer memories to assemble the data packets into sufficient large blocks.

2.5 The Common Read-out Unit - CRU

The CRU acts as the interface between the on-detector systems, the online and offline computing system (O^2) and the central trigger processor (CTP). It is based on high performance FPGA processors equipped with multi-gigabit optical inputs and outputs. The interface to the detector control system (DCS) is done via a node of the O^2 system or via a commercial network switch. A block diagram of this system is shown in Fig. 2.1. Where possible, the new detectors or those for which the electronics is redesigned will be read out by the CRU.

Bi-directional front-end links based on the Versatile Link and the GigaBit Transceiver (GBTx) serialiser/deserialiser chip [14] connect the on-detector systems to the counting room-located CRU carrying detector data, configuration and trigger information. Depending whether the automatic SEU error correction is activated, the link bandwidth is 3.2 Gb/s or 4.48 Gb/s.

Bi-directional DDLs connect the CRU to the O^2, carrying hit data and configuration data. The DDL is implemented either as DDL3 or as a slot of the input-output bus of a PC (PCIe Gen 3).

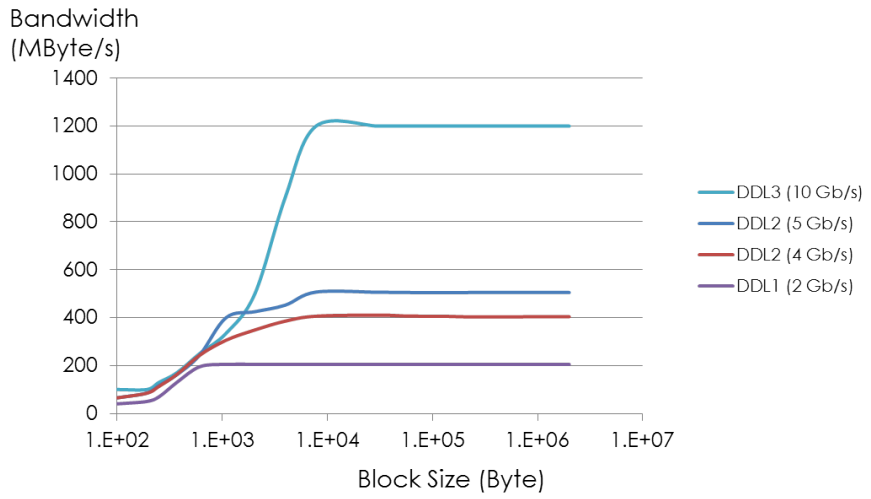


Figure 2.3: The performance of the DDL1 clocked at 2.125 Gb/s, of the two variations of DDL2 clocked at 4.25 and 5.3125 Gb/s and of a prototype of DDL3 clocked at 10.3125 Gb/s.

Presently for all system and cost considerations, a DDL3 bandwidth of 10 Gb/s is assumed.

The fast serial trigger and timing distribution (TTS) links connect the CTP to the CRU, which forwards the trigger data to the on-detector electronics. For some detectors, the TTS links transport the busy signal from the CRU to the CTP. For most detectors, the CRU only multiplexes the data from several front-end links into better performing high speed data links without any data processing. The TPC is one exception, where the CRU re-orders the data samples according to their position in the pad row, allowing a more efficient cluster search in the O^2 system.

The ALICE CRU system evaluation is based on the hardware implementation basis of the AMC40 system developed in the framework of the LHCb read-out [16]. The system is based on the ATCA crate standard. One ATCA carrier board houses 4 advanced mezzanine cards (AMC40) each with up to 36 optical bi-directional links with a bandwidth of up to 10 Gb/s per link. Figure 2.4 shows a picture of the mezzanine card. Figure 2.5 shows a block diagram of one mezzanine card. In the standard configuration, 24 of the bi-directional optical connections are used to connect 24 GBT front-end links, carrying detector data to the CRU and transmitting configuration and optionally trigger data to the on-detector electronics. The DDL3 links use the remaining 12 bi-directional connections to forward the hit data to the online computing system and send configuration data to the CRU. Cost calculations, as shown in the detector description, are based on this configuration. For the transition radiation detector (TRD), the number of links between the online and offline computing system (O^2) and the CRU can be reduced, allowing a higher number of front-end links to be connected.

For the CRU system implementation next to the ATCA crate configuration, a solution where the CRU is plugged directly into PCIe slot of the online computing node is evaluated. In that case, the PCIe bus serves as DDL3, requiring no optical links. However, the trigger distribution cannot be done on the crate back plane.

The present version of the AMC40 system can accommodate FPGAs which are available with three matrix sizes. Currently, all prototypes have been equipped with FPGAs of the smallest size. Should it turn out that the matrix size is insufficient for applications where data processing on top of the data multiplexing is performed, the two larger pin compatible FPGAs can be used with the same printed circuit board. Cost estimates and performance estimates have been done taking the smallest FPGA into account.

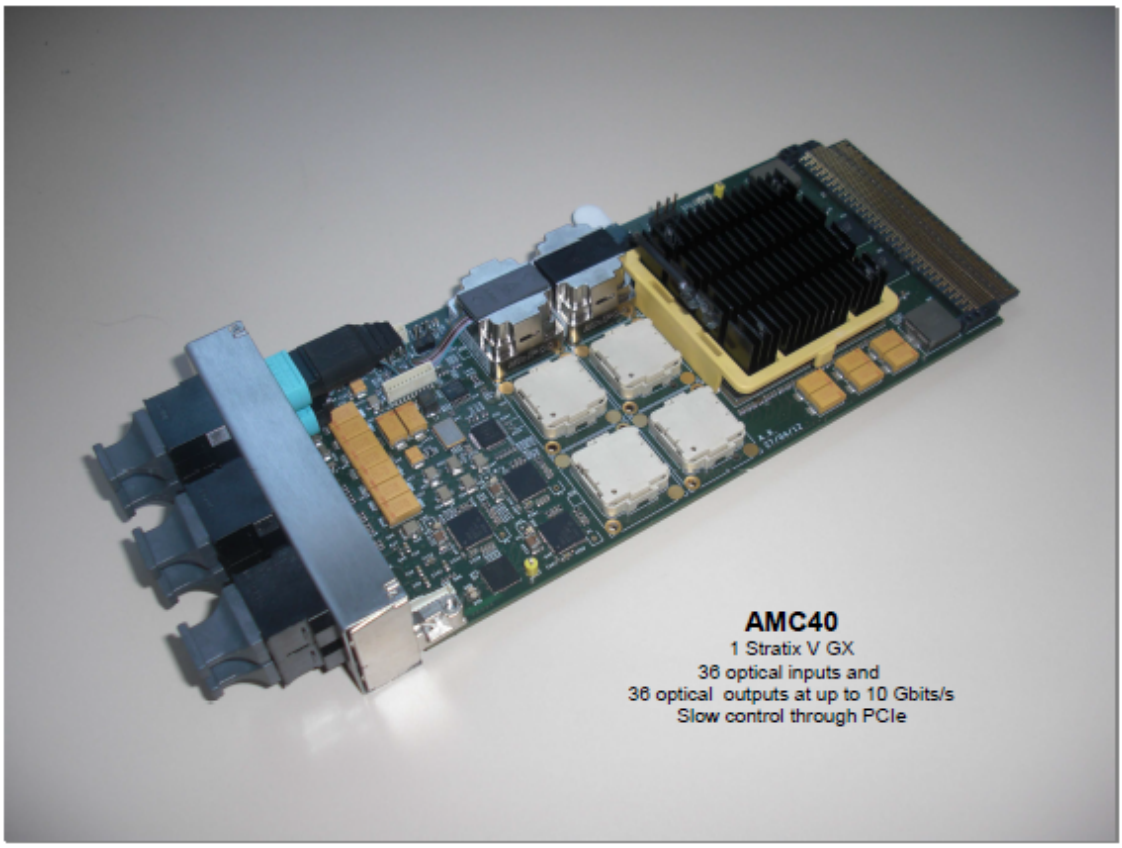


Figure 2.4: AMC40 ATCA mezzanine card. The front-panel contains 36 optical inputs and 36 optical outputs.

The GBT links support forward error correction, allowing the correction of transmission errors due to single event upset effects. When forward error correction is enabled, the data bandwidth is reduced from 4.48 Gb/s to 3.2 Gb/s. Figure 2.6 shows a block diagram containing the main building blocks in the CRU system based on GBT front-end links. Electrical serial e-links [14] connect to the GBTx e-link interface. Each e-link contains a bi-directional data link and a clock output. Depending on operation mode, the GBT protocol allows a bit rate setting of 320, 160 or 80 Mbit/s and offers 10, 20 or 40 e-links, respectively. This allows the adaptation of the e-link data rate to the detector application. For instance, the TPC, with its high data volume, will operate in the 320 Mbit/s mode where only 10 e-links are available for one GBT optical link. The muon chamber detector (MCH) will use the link at 80 Mb/s, as the data rate per front-end unit is much lower in order to profit most efficiently from the GBT data bandwidth. The GBTx ASIC decodes the data and transmits it via the versatile optical link components. Two different types of components are available. The VTRx is a radiation hard optical transceiver component offering one input and one output. The VTTx is a double optical transmitter. These two components allow adaptation of the read-out bandwidth to the detector segmentation. For example, in the TPC system, which has many more data links going to the CRU than TTS links going to the detector, the VTTx component is used for the front-end links and the VTRx component for the fewer TTS links. The MCH has as many front-end links as TTS links and thus will use only the VTRx component. A dedicated slow control adapter (SCA) ASIC [17] provides I2C interfaces to transmit the configuration data to the detector front-end, as well as ADCs to verify the supply voltages and DACs to provide bias.

In the TPC, MCH, MID and ZDC, the trigger latency is not critical and thus one can afford to

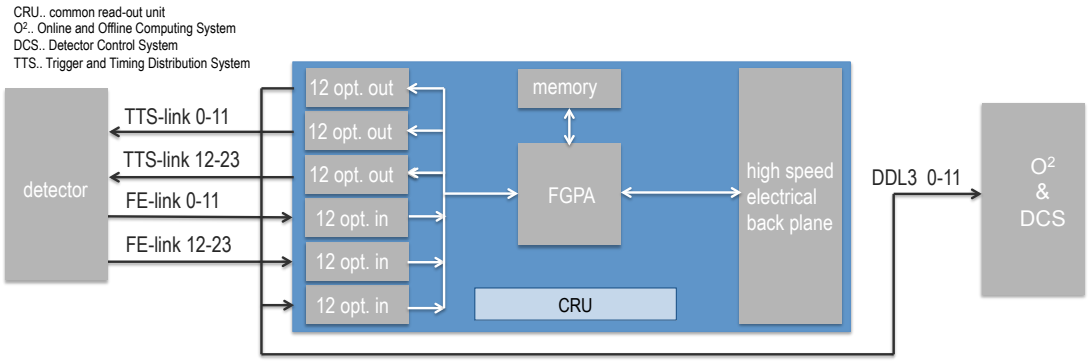


Figure 2.5: CRU block diagram.

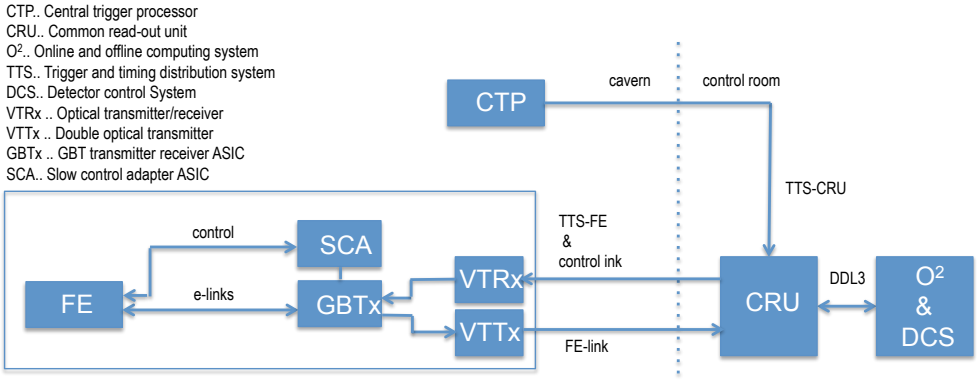


Figure 2.6: System block diagram with GBT and versatile link chip set.

send the trigger data from the CTP in the cavern to the CRU in the counting room and from there to the detector. Assuming a maximum cable length of twice 150 m, an additional $\approx 1.5\ \mu$s of latency applies. It should be noted that using constant latency GBT links from the CTP to the CRU and again from the CRU to the FEC will cause the trigger information to arrive with constant latency at the front-end. Using an ATCA crate solution for the CRU has the advantage that the trigger and timing information can be distributed via the high speed back plane and thus the number of trigger links from the local trigger units (LTU) to the CRU is very low (see Tab. 4.4).

The ITS plans for 976 1 Gb/s electrical front-end links leaving the detector staves, which extend to 184 ITS read-out cards located on the ALICE detector in the so-called mini frame. These cards multiplex the ITS front-end link protocol into either the GBT compatible format or directly to the DDL3 format. Due to maximum latency restrictions, the trigger signal must be routed directly from the CTP to the detector without a detour via the counting room and thus the TTS interface needs to be located on the ITS read-out card.

The TRD will also use the CRU to concentrate the 1044 TRD front-end links. Whether the CRUs will be located in the control room or in the cavern in a low radiation area is currently under study.

The ALICE collaboration has two institutes responsible for the ALICE CRU design. The Wigner Institute, Hungary, is the institute which developed and produced the previous version of common read-out developments, the DDL1 and DDL2, as well as the ALICE Data Acquisition Read-out Receiver Cards version D (D-RORC, see Fig. 2.7). The common version of the RORC (C-DORC) was designed by the University Frankfurt and produced by the Wigner institute

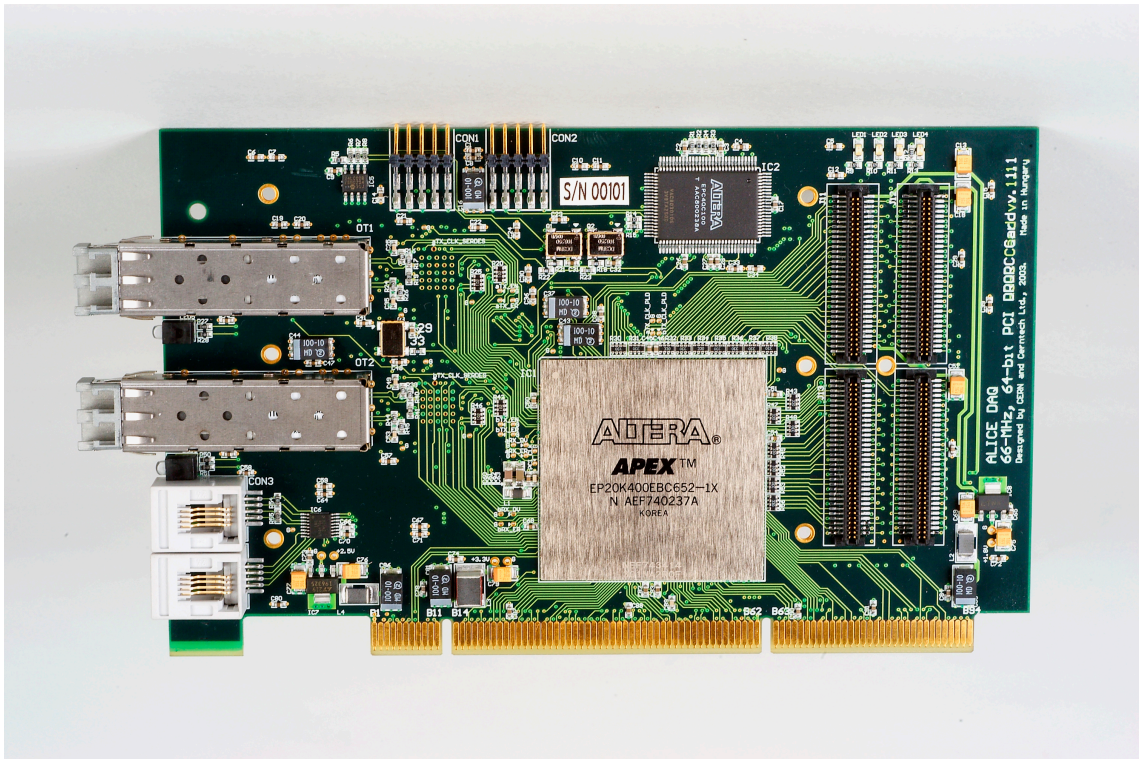


Figure 2.7: ALICE D-RORC.

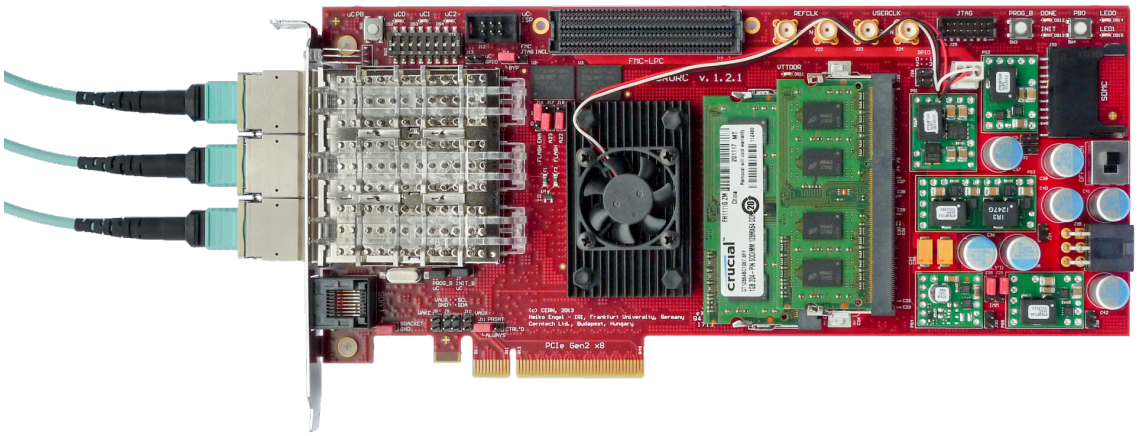


Figure 2.8: ALICE C-RORC.

(see Fig. 2.8). These cards are already PCIe bus plug-in cards. The CRU based on ATCA or PCIe is an evolution of the existing developments. The second institute involved is the Variable Energy Cyclotron Centre, VECC, India. The development will be carried out in collaboration with LHCb.

2.6 Read-out of detectors not using the Common Read-out Unit

Those detectors which do not use the CRU will use detector-specific back-end electronics which interface to the ALICE O^2 via the DDL1 or DDL2.

Table 2.4 summarises the link usage detector by detector and link type. DDL links connect to the online and offline computing system (O^2). CRU-FE links carry hit data from the on-detector electronics to the CRU. TTS-FE links carry trigger data from the CRU to the on-detector electronics (see Fig. 2.6). Detectors with 0 TTS-FE links use the CRU but receive the TTS information directly from the CTP at the on-detector electronics. Detectors with no entries for TTS-FE links do not use the CRU.

Detector	DDL1	DDL2	DDL3	CRU-FE-links	TTS-FE links
	2.125 Gb/s	4.25-5.3125 Gb/s	10Gb/s	3.2 Gb/s	3.2 Gb/s
TPC			1200	6336	1764
MCH			250	500	500
ITS			*60	*184	0
MID			1	16	16
ZDC			1	1	
TOF		72			
FIT		2			
ACO	1				
TRD			36	1044	0
EMC		20			
PHO		16			
HMP	14				
Total	15	110	1555	8081	2244

Table 2.4: Number of DDL, CRU-front-end links and TTS-FE links. (*=depending on implementation the ITS on-detector electronics will either use DDL3s to connect to the O^2 or CRU data FE-links to the CRU. Numbers shown reflect the CRU configuration.)

2.7 Data framing, aggregation and event building

The global architecture of the online system as presented in the upgrade LoI [1] is shown in Fig. 2.9.

Each detector will split its data over several DDLs to accommodate their segmentation and read-out rate. The online and offline computing system (O^2) collects the data of the DDLs.

Data (delimited by consecutive heartbeat events) will be assembled in two stages. The time frames delivered by the DDLs connected to the O^2 will be assembled together on the basis of the time stamping. A first stage of reduction of the data volume will be applied in the O^2

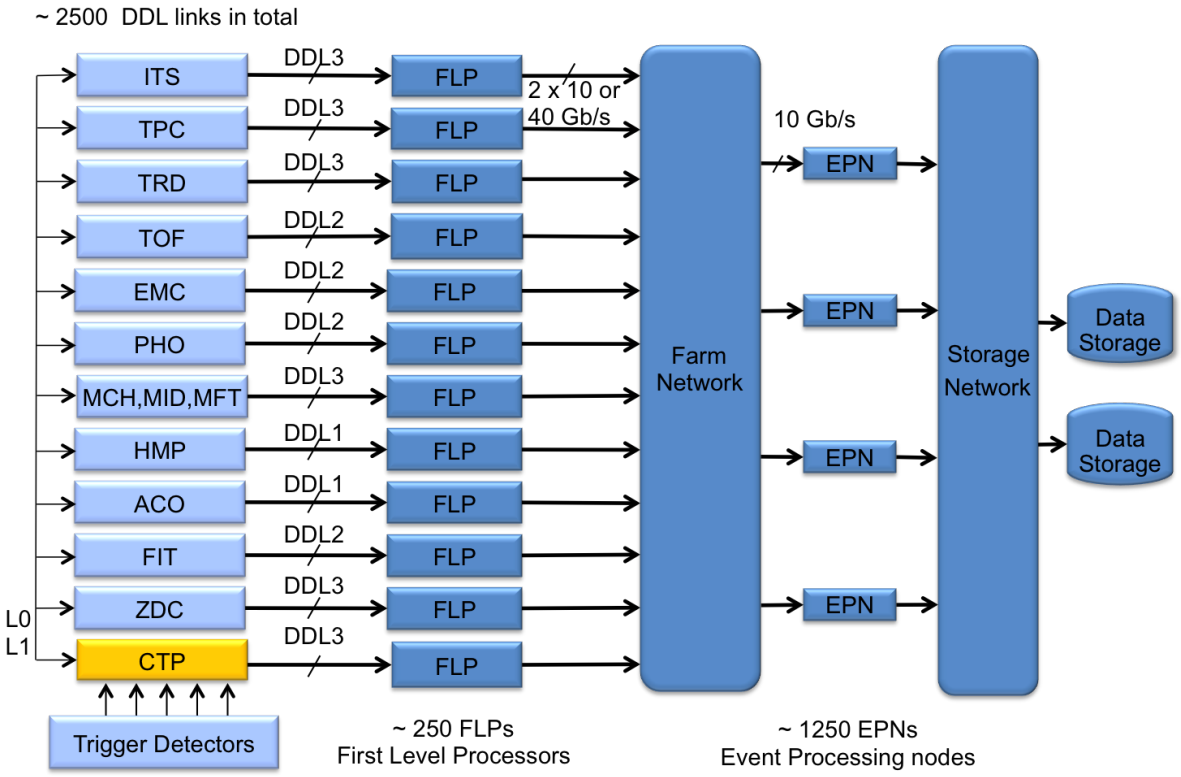


Figure 2.9: The global architecture of the online and offline computing system (O^2).

performing local data processing e.g. cluster or tracklet finder. Event Processing Nodes (EPN) perform the second level of data aggregation and a further reduction of the data volume will be applied in the EPN by performing a global processing allowing, for example, the reconstruction of the tracks and association of them to their primary vertex. This will allow disentanglement of the different interactions included in a timeframe and the performance of the event building.

2.8 System control signals

This section describes the system control signals. The ALICE system works with three control signals: the LHC clock, the trigger signal and the busy signal. Fig 2.10 illustrates the principle.

LHC clock The upgraded ALICE read-out system tags each data sample with a bunch crossing number identifying the bunch crossing at which the signal has been sampled. For those detectors where the sampling time is longer than one bunch crossing the first bunch crossing at which the signal exceeded threshold is taken as reference. The TPC and MCH using the SAMPA ASIC are an example, where subsequent samples belonging to the same event are time-tagged with reference to the initial bunch crossing. The event building process relies on these bunch crossing tags to identify data samples belonging to the same event. As a consequence, each detector needs to receive a common reference timing signal, the LHC clock, which allows identifying the bunch crossing the event took place. The transmission of the clock signal is done to each of the detector front-end and read-out modules on a constant latency distribution network. That means once the ALICE hardware installation is completed, the phase relation between the destination nodes is defined, but can be tuned by remote programming.

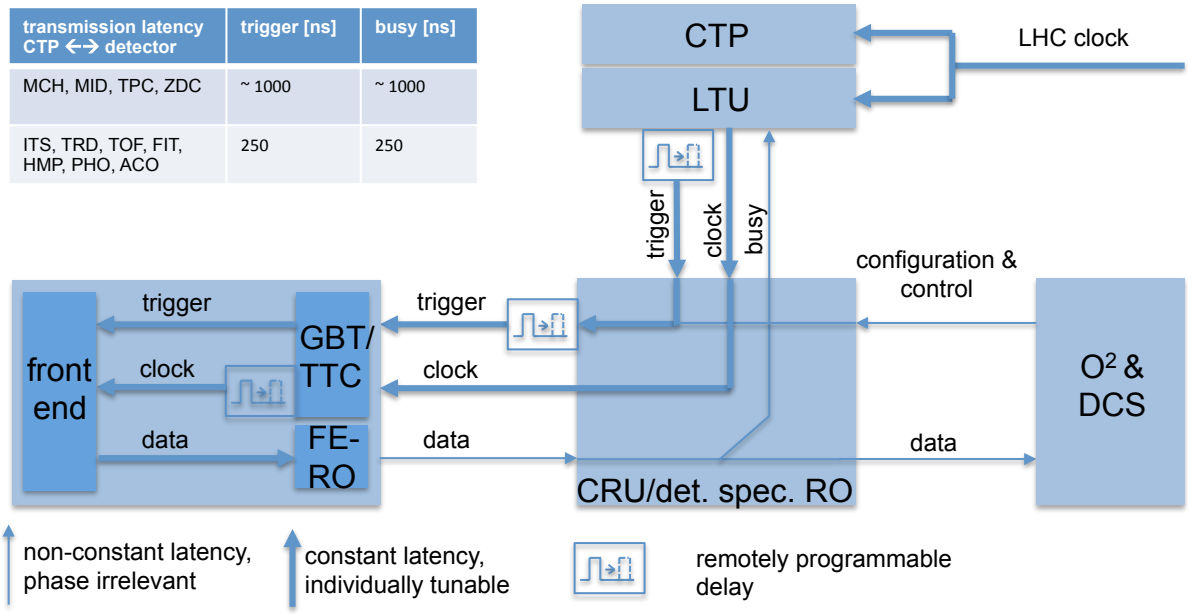


Figure 2.10: ALICE read-out control signal flow.

Trigger signal The upgraded ALICE detector will read out and record all interactions with a nominal rate of 50 kHz in Pb-Pb and 200 kHz in pp. It should be noted, that the interactions arrive at random times, however, within the binning of the LHC bunch crossing period of 25 ns. The ALICE CTP distributes one trigger signal to all detectors for each collision and starts the read-out of detectors. Even though the TPC and MCH can operate in continuous trigger-less mode, optionally, the ALICE trigger signal can be processed by these detectors. The trigger signal is issued by the CTP system and distributed by the LTU module on a constant latency distribution network. After installation, the phase relationship between the destination node is defined by the installation hardware, but can be tuned by remote programming. In addition to the trigger signal, a trigger message is sent to the detector read-out modules which contains the bunch crossing and orbit counter information. Both counter values are attached to the read-out data packets, which allow the online system to assemble the event fragments by identifying the corresponding data packets. Each detector read-out system has a local copy of the bunch crossing and orbit counter information. At the reception of a trigger signal and the message, the detector read-out electronics compares the local copies with those values extracted from the trigger messages. In case of a discrepancy, the online systems are alerted and the counters are resynchronised. The local copies of these counters are reset by a dedicated non-physics trigger signal, the heartbeat trigger, distributed at a fixed position in time during the LHC bunch crossing gap. It should be noted that the heartbeat trigger signal does not interfere with the read-out capabilities of a detector. It only initiates the transmission of empty events containing the bunch crossing number at which the heartbeat trigger has been received. Thus, it does not occupy read-out buffer space.

Busy signal In case the trigger rate exceeds the detector read-out capabilities the read-out systems indicate this situation by asserting a busy signal. The busy signal is transmitted to the the CTP system which stops the transmission to this corresponding detector until it again is able to read out data. In contrast to the Run1 scenario, a detector which is busy will not interrupt the entire ALICE data acquisition. Only the the read-out of the corresponding detector is suspended. The CTP handles one busy signal per detector only which means, if one detector partition is busy, the entire detector is not read out. However, in order to exclude faulty detector

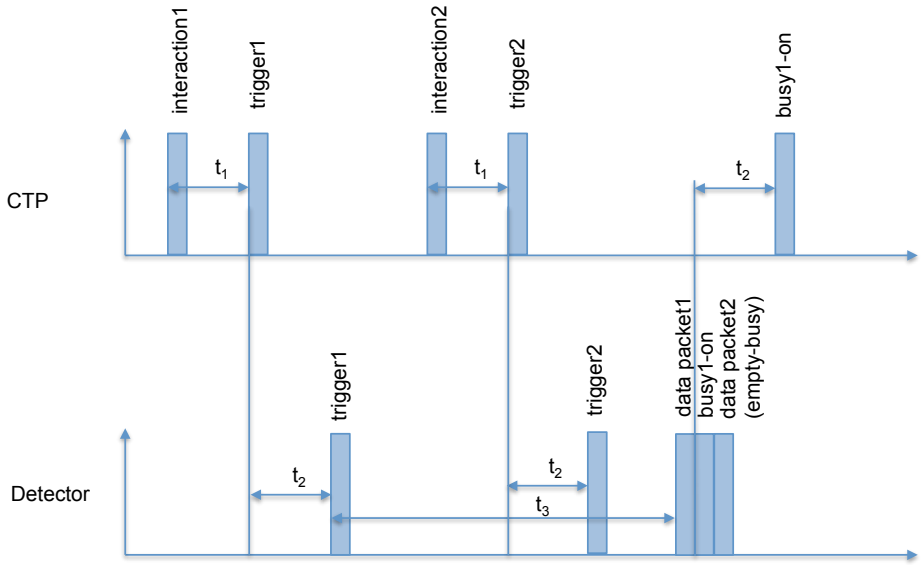
modules, the busy state of the individual detector partitions can be read-out and analysed.

System timing alignment The ALICE system provides two handles to tune the system timing. In the first step of the timing alignment procedure, the trigger distribution delays for all sub-systems are aligned, so that each sub-system refers to the the same bunch crossing and orbit counter identification value for a given bunch crossing. Otherwise, the event fragments belonging to one event coming from different sub-systems or system partitions would either have different bunch crossing identification numbers or the read-out would contain data from wrong bunch crossings. This procedure involves actual beam data taking and histogramming the bunch crossings which contain data and scanning the trigger delay for the sub-system partitions. The LHC bunch crossing gap acts as clear reference indicator where no data must be found. Also it should be noted, that ALICE operates with a reduced interaction rate where a majority of bunch crossings are not filled, which simplifies this alignment procedure. The actual tuning of the trigger delay can be done in several places. The LTU allows tuning with a binning of 25 ns over at least 32 bunch crossing periods for each detector partition individually. This allows cable delay compensation of up to 160 m. The CRU or detector specific read-out systems allow tuning of the delay with finer geometrical granularity. Depending on the detector implementation, the final tuning stage is sitting directly on the detector front-end or read-out where the trigger latency is adapted by remote programming accordingly.

In the second step, the clock arriving at the front-end electronics is phase tuned so that all signals from one given bunch crossing are registered into one bunch crossing time bin. The clock phase can be tuned on the front-end electronics (via the GBTx or TTCrx) with a binning of 50 ps over the full range of one 25 ns period. The clock phase alignment procedure is done independently for each detector sub-system once the beam is available using automated routines, which histogram the occupancy for each bunch crossing bin and optimise the phase accordingly.

Control loop The principle of the ALICE upgrade read-out structure relies on the TTS system distributing the clock and trigger signals on constant latency links to the read-out and front-ends and to receive the busy signal to throttle the trigger distribution if necessary. For the transmission of the busy signal, constant latency is not required. As all data packets leaving the detector are time tagged, the transmission delay of the read-out data path is of no importance and uses non-constant latency links to the on-line farm.

For those detector systems which contain sufficiently large multi-event buffers or even continuous read-out under nominal operation conditions, a busy situation will not occur. In that case, the busy transmission is considered non-latency critical and for example will be routed for the TPC, MCH and ITS through the CRU and from there to the CTP. The latency of this transmission is in the order of 1 μs including serialisation, deserialisation and cable delay from the cavern to the control room and to the CTP system. In the case a busy situation occurs, either due to operation outside the nominal parameters or an error condition, the busy signal will be transferred to the CTP stopping the trigger transmission to these detectors. Furthermore, the experimental control system is alerted of the busy state of the corresponding detectors. Due to the long control loop between trigger distribution and reception of busy, when a detector gets busy, the busy signal might not yet have arrived at the CTP and another trigger might already have been distributed to the detector system. In this situation the front-end will disregard the trigger and the CRU will transmit an empty data packet to the online system containing information about the busy situation. Once the busy situation is terminated by reading or flushing the buffers, normal operation is resumed.

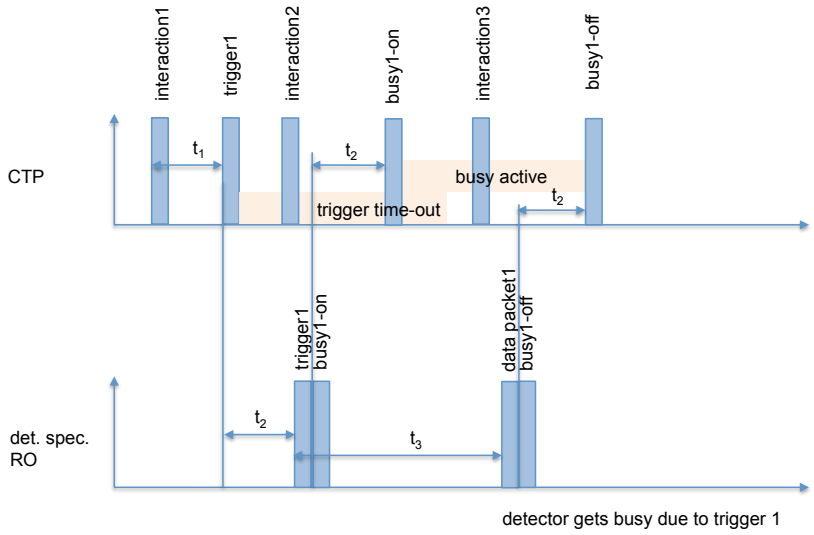


Signal	Note	Latency
t_1	Time between interaction and CTP trigger output	not relevant for control loop constant latency programmable between 775 to 6400 ns
t_2	Propagation of trigger/busy between detector and CTP	for trigger: constant latency ~ 1 µs
t_3	Read-out time	busy is extracted from data stream: > 1 µs

Figure 2.11: Control timing diagram for detectors with sufficient multi event buffer structure.

Figure 2.11 shows a wave diagram illustrating the configuration of detectors with multi-event buffers or continuous read-out assuming that trigger1 initiates a busy state. After the interaction (t_1) the CTP releases the trigger signal which is propagated via the CRU to the detector (t_2). This propagation is done with constant latency, but as the CRU is located in the cavern, this takes of the order of 500 ns. The detector electronics extracts the busy status from the data stream (t_3) and forwards the busy information to the CTP (t_2) and the online system. This will suspend the transmission of triggers to the detector. However, as this control loop is long compared to the interaction rate, triggers might already have been issued in the meanwhile. The detector electronics acknowledges the trigger by sending an empty data packet containing the busy information. That way the online system can assemble the event accordingly. Due to this feature the length of the control loop is irrelevant.

For those detectors which do not contain sufficiently large multi-event buffers busy situations will occur under nominal operation conditions. In that case, a fast transmission of the trigger and busy signals to/from the detector is required. This is managed by direct trigger and busy cable connections between on-detector electronics and the CTP system. As the CTP is also located in the experimental cavern, the maximum cable distance is in the order of 40 m. The total trigger/busy propagation delay from the CTP to the detector and back to the CTP is 2 x $\approx$ 200 ns transmission delay and $\approx$ 2 x 50 ns processing. In order to protect the detector from receiving triggers while already busy, the CTP models the detector multi-event buffer structure taking into account the minimum read-out time. That way the CTP emulates the busy signal in the detector read-out system and does not issue a trigger when the CTP copy of the busy signal is asserted. In addition to this, the CTP applies a time-out corresponding to the transmission delay of trigger and busy before another trigger can be sent to the this detector. This penalty



Signal	Note	Latency
t_1	Time between interaction and CTP trigger output	not relevant for control loop constant latency programmable between 775 to 6400 ns
t_2	Propagation of trigger/busy between det. spec. RO and CTP incl. processing	250 ns
t_3	Read-out time	non-constant, detector specific, ie. TRD: ~ 6 µs, EMC/PHO: ~19 µs

Figure 2.12: Control timing diagram for detectors with no or insufficient multi event buffer structure.

is acceptable compared to the average interaction period of 20 μs in Pb-Pb and 5 μs in pp and to the average read-out time of the detectors.

Figure 2.12 shows a wave diagram illustrating the configuration of detectors with insufficient or no multi-event buffers assuming that trigger1 initiates a busy state. After the interaction (t_1), the CTP releases the trigger signal which is propagated via the detector specific read-out system to the detector (t_2). This propagation is done with constant latency on dedicated cables. The detector electronics sends the busy information to the CTP (t_2) which suspends the transmission of triggers to the detector (interaction3). In order to suppress any trigger distribution during the propagation time of the trigger and busy signal for the detectors without multi-event buffer, the CTP invokes the trigger time-out suppressing any trigger transmission (interaction2). For the detectors with multi-event buffer, this time-out is only invoked in case the copy of the multi-event buffer in the CTP foresees a busy situation. After the read-out (t_3) the inactivated busy signal is transmitted to the CTP (t_2) which resumes the transmission of triggers.

2.9 Operation conditions and read-out efficiencies

In the present ALICE detector a trigger is successful only if every one of a list of read-out detectors, the so-called trigger cluster, is available to read out data. The association between trigger cluster and trigger condition defines a trigger class. This approach allows sharing the available read-out bandwidth with several trigger classes adapted to the physics channels under study. For example, one trigger class would require the read-out of ITS, TPC and TOF and the data set read out from the same interaction would be marked with the corresponding trigger

class. This scheme involves the evaluation of the busy signal of each detector in the trigger cluster. In this example, the CTP would issue a trigger only to these three detectors when all three detectors were non-busy. This means that the faster detectors, in the example ITS and TOF, would wait for the slower TPC in most of cases, although ITS and TOF are free for read-out.

Due to the improved read-out performance of the upgraded detectors a more flexible approach will be pursued as baseline. If a trigger condition is satisfied, all detectors available at that moment are read out and the corresponding detector data are assembled to trigger classes in the online system. That way, each detector is treated as a separate cluster and the busy status of every detector is treated independently. This strategy is made possible by the high read-out efficiency of the upgraded detectors, which will support continuous read-out or have a sufficiently high number of multi-event buffers allowing under nominal beam conditions a read-out with close to 100 % efficiency.

Table 2.3 shows a summary of the sub-detectors with respect to their integration in the read-out system for Pb-Pb beam operation. Horizontal lines separate detectors with similar read-out properties in three groups. The detectors in the first group support continuous read-out and triggered read-out (TPC and MCH), which when operated under nominal beam conditions have a read-out efficiency of 100 % as the size of the multi-event buffers in each channel of the TPC/MCH read-out ASIC, SAMPA, allows loss-free operation beyond the expected interaction rate. The second group of detectors (ITS, MID, ZDC, TOF, FIT, ACO) needs a trigger and has multi-event buffers which de-randomise the arrival time of the data with which a read-out efficiency of almost 100 % will be achieved. As an example study, Fig. 2.13 shows the read-out efficiency of the ITS depending on the number of multi-event buffers in the pixel cell. From these studies it can be concluded that the ITS pixel ASIC needs 2 buffers per pixel to achieve an overall read-out efficiency better than 99.8 %. The other detectors in that group have much lower data occupancy and the buffers in their read-out electronics are dimensioned to sustain fully efficient read-out under nominal conditions. The third group of detectors (TRD, EMC, PHO, HMP) is not fully efficient at 50 kHz interaction rate due to limits in the read-out system that are not feasible for upgrade.

Figure 2.14 shows the read-out performance of the ALICE detectors versus interaction rate. It shows that for ITS/TPC/TOF/MCH/MID/FIT/ZDC the read-out efficiency stays high even beyond the nominal Pb-Pb operation of 50 kHz and pp operation of 200 kHz. The plots take the expected read-out time and the number of multi event read-out buffers into account. For example, the TRD does not contain multi-event buffers. Thus, after each trigger the system is busy for t_{busy} of 6 μs. The read-out efficiency is therefore given by: $(f_{read-out}/f_{trigger}) = 1/(1+ f_{trigger}{*}t_{busy})$. The PHO/EMC system contains 4 multi-event buffers. The ITS system contains three multi-event buffers. The plots for PHO/EMC and ITS are derived analytically [18] and by simulation [5]. For TRD and EMC/PHO the read-out efficiency decreases at high rates. It should be noted that PHO and EMC are treated as one single system and triggers are issued in common to these two detectors. Table 2.5 shows the read-out performance of the main physics channels and the detectors required for these channels as described in the LoI. The read-out efficiency values are derived from the read-out performance of those detectors required for the corresponding physics channel. EMC/PHO can recuperate full efficiency for jet physics by using the EMC/PHO L0 triggers with very modest thresholds. The fact that a fraction of these events has missing TRD information is negligible since momentum resolution and matching are of minor impact for these measurements. The effect of missing TRD information on the different physics channels discussed in the LoI are given in section 2.10.

For possible future needs, it is important that the ALICE system allows for run conditions not

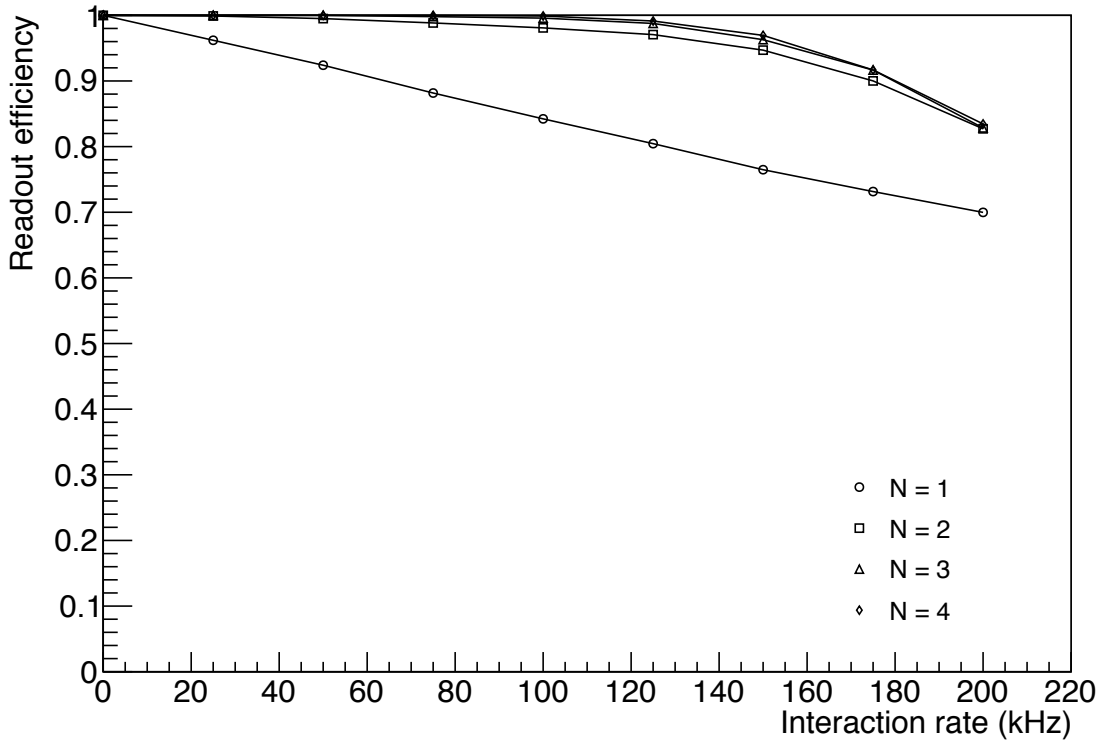


Figure 2.13: ITS read-out efficiency versus the Pb-Pb collision rate with the number of multi-event buffers in the pixel ASIC as parameter. The plot shows that with at least 2 buffers the ITS exceeds 99.5 % read-out efficiency at 50kHz interaction rate.

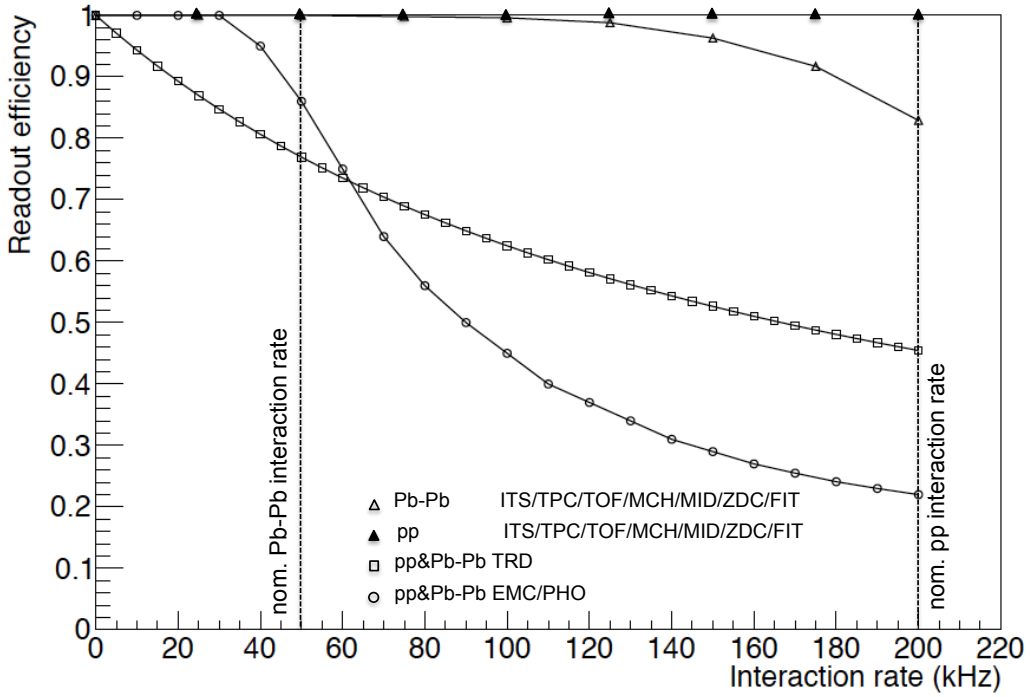


Figure 2.14: Read-out efficiency of the ALICE detectors vs. interaction rate for Pb-Pb and pp operation.

Physics channel	ITS	TPC	MCH	TOF	TRD	PHO/ EMC	Read-out efficiency [%]
Heavy flavour (excl. reconstruction)	x	x	-	x	-	-	99
Low mass dielectrons	x	x	-	x	o	-	$99/75^{+}$
Forward heavy flavour	x	x	x	x	-	-	99
Charmonium to e^+e^-	x	x	-	x	x	-	75
Jets	x	x	-	x	o	x	$84/100^{\#}$
TPC calibration	x	x	-	-	x	-	75

Table 2.5: Read-out efficiency for several detector combinations for 50 kHz Pb-Pb interaction rate. x .. detector is required, - .. detector not required, o .. used if present, $^{+}$ .. including TRD, $^{\#}$ .. EMC self triggered.

foreseen at present. Thus, the method to define trigger classes as in the Run1/2 scenario is still available in addition to the unconditioned, free running read-out. The CTP again can define trigger clusters containing groups of detectors and can balance the bandwidth between a free selection of all available detectors and a restricted choice requiring a given combination.

The assembly of continuous read-out data from the TPC and triggered data from the other detectors is done in the O^2 system. The event building method is very similar to traditional event building where each data sample is tagged with a trigger/bunch crossing identification number. The event building algorithms look for this identification tag in the data samples and merge the corresponding event fragments to one single data set. For the upgrade, the continuously read detectors will be merged in a similar way. The continuous TPC read-out data stream is separated in time frames of constant time duration and assembled in data packets. Each data packet is tagged with the bunch crossing identification number of the first data sample in the packet. The data samples within a data packet are tagged with a time stamp indicating the time difference to the begin of the data packet. In the online system the packet bunch crossing identification number is linked to the triggers issued in that period of time. This creates the link between continuous read out data and triggered data. It should be noted, that due to the drift time being longer than the average interaction/trigger rate, the TPC data stream will pile up. Thus, data from one given moment in time might belong to events from several triggers. The O^2 system will perform a cluster finding on the TPC data followed by an assignment of the clusters to tracks. The bunch crossing of the interaction from which tracks originate will be used to allocate TPC clusters to a particular event. The final step of the event building will be performed after the online reconstruction.

In order to limit the TPC data sample length to be evaluated when assigning TPC data to triggered data, artificial data boundary markers, the so-called heart beat triggers, have been introduced. In a periodic distance in time, larger than the TPC drift time and $\approx$ 100 ms, the heart beat trigger is sent to all detectors. After the currently active read-out has been finished, the detectors respond with an empty event carrying the bunch crossing information at which the heart beat trigger has been received. That way the continuous TPC read-out stream is separated by heart beat markers. The O^2 evaluates data from two subsequent heart beat trigger periods at the same time to cover events overlapping the heart beat trigger period.

2.10 Effect of the TRD read-out efficiency on the upgrade physics programme

In nominal beam operation conditions, the TRD will not provide dead time free read-out. Consequently a sub-set of the events recorded will have no data from the TRD, which provides tracking and electron identification information. The fraction of events (F) with TRD information is driven by an average dead time of 6 μs and is 76 % for Pb-Pb operation at 50 kHz and 45 % for pp operation at 200 kHz.

Two main effects were considered to assess the impact of events without TRD:

- the lack of electron/hadron separation for $p_{\mathrm{T}} > 1$ GeV/c using the TRD; for these events the separation over the full central barrel acceptance will be provided by the TPC and TOF detectors only.
- the deterioration of the track extrapolation from the TPC to the TOF and of the correct matching with the corresponding TOF hit, which implies the lack of charged particle identification from the TOF.

The drop of the matching efficiency to the TOF was estimated using simulations of central Pb-Pb events, in which the TRD detector material was included but the TRD information was not used in the tracking. The drop was found to be of about 40 %, 10 % and 5 % for p_{T} values of 0.3, 0.6 and 0.8 GeV/c, respectively. The drop becomes negligible above 1 GeV/c.

In the following the impact of these effects for heavy-flavour, low-mass dielectron and charmonium measurements is discussed.

Heavy flavour. The TRD is not used for particle identification in the measurements presented in the LoI (hadronic decays for heavy flavour hadrons). The impact of the TOF matching deterioration is expected to be negligible. Indeed, the analyses for which both particle identification and high statistics are crucial are the reconstruction of $\Lambda_{\mathrm{c}} \rightarrow \mathrm{pK}\pi$ and $\Lambda_{\mathrm{b}} \rightarrow \Lambda_{\mathrm{c}}\pi$ decays. However, it has been shown that a single track selection $p_{\mathrm{T}} > 0.8$ GeV/c is very effective for the rejection of the combinatorial background. Therefore, the drop of TOF matching effiency is practically irrelevant for these analyses and the events without TRD information can be used.

Low-mass dielectrons. For this analysis, the study reported in the LoI does not use electron identification with the TRD, because in the low-p_{T} region, that is the most relevant in this case, the electron/hadron separation with TPC and TOF is very efficient. On the other hand, the deterioration of the TOF matching efficiency in events without TRD will imply a loss of signal. The resulting increase of the statistical uncertainties is expected to be significantly smaller than $1/\sqrt{F}$-1=15 %. The low-mass dielectron measurement does not depend crucially on the comparison with pp collisions, therefore the lack of TRD information in this case is not an issue.

Charmonium (J/ψ and $\psi' \rightarrow \mathrm{e}^+\mathrm{e}^-$). In the LoI it is shown that using the TRD, in addition to the TPC, for electron identification reduces very significantly the combinatorial background (from misidentified pions) in Pb-Pb collisions, thereby improving the statistical uncertainties by a factor of almost two. In consideration of this, the optimal analysis approach is to discard the events without TRD information. The resulting increase of about $1/\sqrt{F}$-1=15 % in the statistical uncertainties is not expected to affect significantly the quality of the measurements. In pp collisions, on the other hand, the combinatorial background is much lower than in the Pb-Pb case and electron identification with the TRD

will not be crucial. Therefore, it will be possible to use also the events without TRD for these analyses.

3 Radiation environment

Radiation calculations for the present ALICE detector, performed with FLUKA [19] and the VMC interface [20], can be found in [21]. In this chapter, updated calculations that take into account the recent results on measured multiplicities for Pb-Pb, pp and p-Pb collisions are presented. The hadron fluence, quoted in 1 MeV neutron equivalents (neq), and the Total Ionising Dose (TID) are the numbers that determine the long term radiation damage of sensors and electronics. The two numbers are given in Fig. 3.1 and Fig. 3.2 for a delivered Pb-Pb luminosity of $10\,\mathrm{nb}^{-1}$. The rate of hadrons with a kinetic energy >20 MeV determines the rate of single event upsets in the microelectronics circuitry and is given in Fig. 3.3 for the 50 kHz pp-Pb collision rate. The simulated geometry still assumes the present ITS detector, with detailed implementation of services and support structures. Since the upgraded ITS will use ultra light structures optimised for minimum material budget, one can assume that the upgraded ITS will represent less material than the present one and therefore the obtained numbers present a worst case scenario.

At positions with -100 < z < 350 cm, the radiation numbers are dominated by primary tracks originating from the interaction point. At z < -100 cm, the frontabsorber is absorbing hadrons that are pointing towards the muon system, which leads to a decrease of the TID but an increase of the hadron fluence due to the lateral escape of neutrons from the absorber.

The planned $6\,\mathrm{pb}^{-1}$ pp collisions and $50\,\mathrm{nb}^{-1}$ p-Pb collisions add 13 % to the TID and hadron fluence numbers. To accommodate for uncertainties in simulation, background levels and possible future physics programs, we assume a safety factor of 10 on top of the simulated numbers for TID and 1 MeV neq hadron fluence. A safety factor of 2 is applied to the instantaneous rate of $E_k > 20$ MeV hadrons. Table 3.1 shows the results for specific locations inside the ALICE detector. In case a range of z-positions is indicated, the table refers to the maximum value inside this interval.

The ITS and MFT detectors have to withstand a TID close to 1 Mrad and a hadron fluence up to 10^{13} cm^{-2}. The flux of high energy hadrons is close to $1.6\,\mathrm{MHz/cm}^2$ for these detectors. The radiation levels for the FIT detector are a factor 3-4 lower but still of similar magnitude. The TPC electronics located at the inner radius of the service support wheel has to withstand a dose of 2.1 krad and 3.4 kHz of high energy hadrons. For muon station 1, the radiation levels are very similar, so these numbers set the scale for the radiation tolerance of the common TPC/MCH read-out chip, SAMPA.

It must be noted that the above numbers for TID and 1 MeV neq fluence are only up to a factor of 2 higher than the numbers in [21] that were assumed for the design of the present ALICE detector, because of different assumptions on multiplicity and running conditions. The numbers for $E_k > 20$ MeV hadron fluence are up to a factor of 3 larger than the ones originally assumed. The electronics of TRD, TOF, EMC, PHO and HMP, that will remain unchanged after LS2, are expected to be able to cope with this environment.

Element	r (cm)	z (cm)	TID (krad)	1 MeV neq (cm^{-2})	>20 MeV had. (kHz/cm^2)
ITS L0	2.2	[-13.5, 13.5]	646	9.2×10^{12}	1600
ITS L1	2.8	[-13.5, 13.5]	387	6.0×10^{12}	1000
ITS L2	3.6	[-13.5, 13.5]	216	3.8×10^{12}	500
ITS L3	20	[-42.1, 42.1]	13	5.2×10^{11}	28
ITS L4	22	[-42.1, 42.1]	9	5.0×10^{11}	24
ITS L5	41	[-73.7, 73.7]	6	4.6×10^{11}	10
ITS L5	43	[-73.7, 73.7]	4	4.6×10^{11}	9
MFT D0	2.5	-50	395	6.7×10^{12}	1100
MFT D1	2.5	-58	392	6.4×10^{12}	1040
MFT D2	3.0	-66	767	5.9×10^{12}	760
MFT D3	3.5	-72	427	4.3×10^{12}	520
MFT D4	3.5	-76	541	4.8×10^{12}	560
FIT1	5	-80	181	3.0×10^{12}	280
FIT2	5	340	103	1.4×10^{12}	200
TPC In	79	[-260, 260]	2.1	3.4×10^{11}	3.4
TPC Out	258	[-260, 260]	0.3	5.2×10^{10}	0.7
TRD	290	[-390, 390]	0.4	4.8×10^{10}	0.54
TOF	370	[-370, 370]	0.13	2.6×10^{10}	0.26
EMC	430	[-340, 340]	0.06	1.5×10^{10}	0.02
MCH S1	19	-536	0.42	4.2×10^{11}	3
MCH S2	24	-686	0.19	1.4×10^{11}	1
MCH S3	34	-983	0.14	1.6×10^{11}	0.9
MCH S4	45	-1292	0.18	3.0×10^{11}	1
MCH S5	50	-1422	0.91	2.5×10^{11}	0.7
CTP Rack	600	-1295	4.8×10^{-3}	7.8×10^{9}	0.03

Table 3.1: Total Ionising Dose (TID) and 1 MeV neq hadron fluence for 10 nb^{-1} Pb-Pb + 6 pb^{-1}pp + 50 nb^{-1}p-Pb collisions (including a safety factor 10) as well as high energy hadron fluence for 50 kHz Pb-Pb collisions (including a safety factor 2).

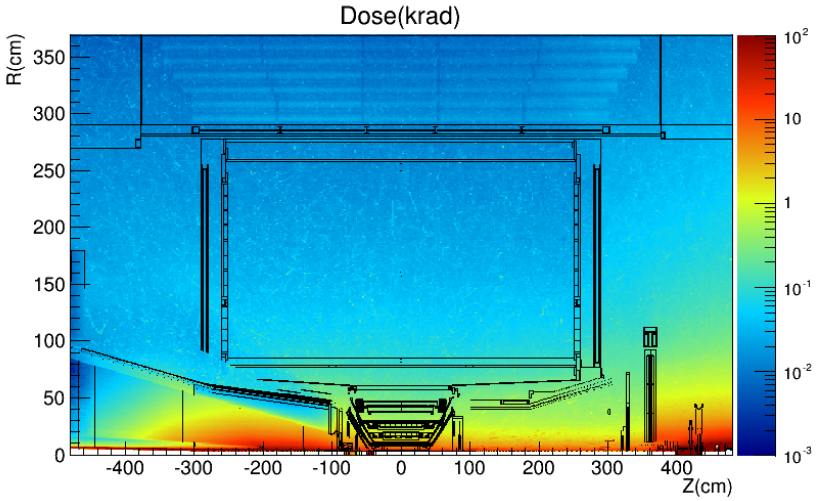


Figure 3.1: Total Ionising Dose for an integrated Pb-Pb luminosity of $10\,\mathrm{nb}^{-1}$ in the ALICE central barrel.

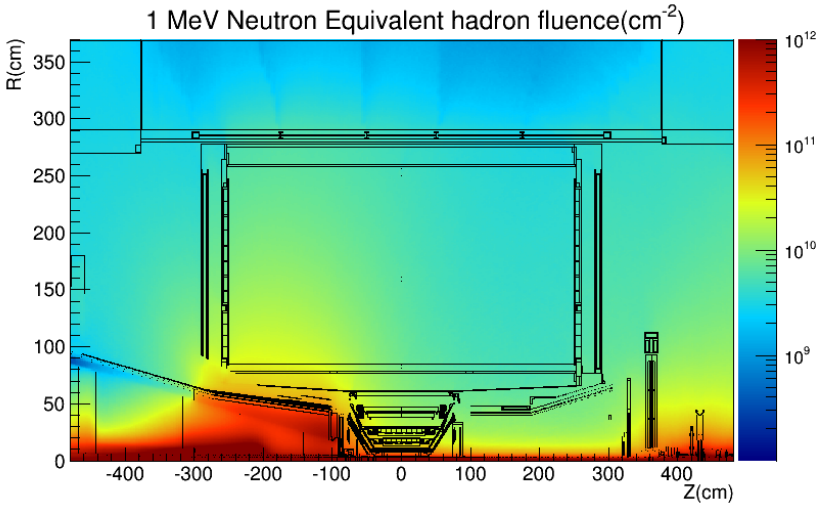


Figure 3.2: Hadron fluence for an integrated Pb-Pb luminosity of $10\,\mathrm{nb}^{-1}$ in the ALICE central barrel.

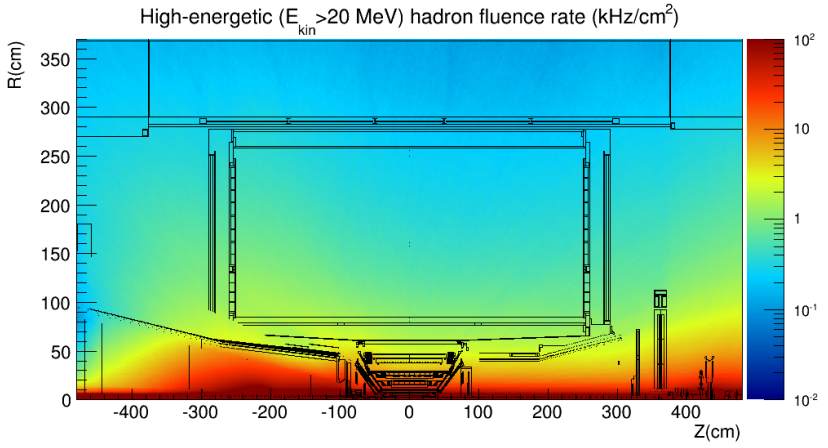


Figure 3.3: Rate of hadrons with energy of $>20\,\mathrm{MeV}$ for a Pb-Pb collision rate of $50\,\mathrm{kHz}$.

4 Central Trigger Processor - CTP

4.1 Introduction

The Central Trigger Processor (CTP) will manage a system of detectors with different properties, as shown in Tab. 4.1. The majority of detectors will read out at the nominal interaction rate dead-time free. However, in order to provide backwards compatibility to detectors not being upgraded, the trigger system must cope with detectors which will have dead-time during the read-out.

The strategy for selecting events for read-out will be different from that employed in previous runs. Previously, despite the fact that ALICE events are highly complex, the trigger strategy was to combine a Minimum Bias sample with a sample selected according to thresholds in high E_t (calorimeter triggers), high p_t, or high multiplicity [2].

The interaction rates will increase to $\approx$ 50kHz for Pb-Pb, and 200 kHz for p-p and p-Pb [1]. Where feasible, a safety margin of 2 is applied in the system design. The strategy for the upgraded ALICE system is to select and read out all interactions and apply an online data reduction in the online computing system. To achieve this, the combination of triggerless read-out and a minimum bias trigger based on the new forward FIT detector is used. A few additional inputs allow for cosmic and calorimeter based triggers.

4.2 Trigger architecture

The overall system architecture is shown in Fig. 4.1. Trigger inputs are collected to satisfy three different latencies, given three different levels shown as LM, L0 and L1. The times, calculated relative to the time of the interaction, are given in Tab. 4.2. The CTP processing time is 100 ns, and propagation of trigger from CTP to detector, not including the trigger distribution in the detector, is about 200 ns.

Table 4.3 shows the number of trigger inputs and different contribution to their latencies.

The LM latency is suitable for generating a wake-up signal for the TRD electronics. The LM trigger will be provided by the FIT detector. However, it will not be possible to generate a trigger signal from the electromagnetic calorimeter (EMC) early enough for this trigger level, and for this reason, the L0 signal is retained. The ZDC is optionally available to clean the minimum bias trigger provided by the FIT. The FIT detector is not suitable for cosmic ray triggers. In this case, TOF and ACO will be used.

As in the present system, trigger decisions are transmitted from the CTP to the individual detectors using an upgraded Local Trigger Unit (LTU). Owing to the reduced number of trigger inputs with respect to Run1 and Run2, for the upgrade it will be possible to implement a lookup-table logic of trigger inputs, allowing full flexibility in the specification of trigger condition. The selection of read-out detectors will be different from previous runs. Previously, a trigger was

Det	triggered by () = optional	Pb-Pb RO rate [kHz]	TTS FTL/TTC	CRU used
TPC	(L0 or L1)	50	FTL	y
MCH	(L0 or L1)	100	FTL	y
ITS	L0	100	FTL	*y
MID	L0 or L1	>100	FTL	y
ZDC	L0	>100	FTL	y
TOF	L0 or L1	>100	FTL	n
FIT	L0 or L1	100	FTL	n
ACO	L0 or L1	100	TTC	n
TRD	LM&(L0 or L1)	39	FTL&TTC	y
EMC	#L0&L1	42	TTC	n
PHO	#L0&L1	42	TTC	n
HMP	#L0&L1	2.5	TTC	n

Table 4.1: Read-out parameter overview for Pb-Pb beam operation at 50 kHz interaction rate. (* = depending on implementation the ITS on-detector electronics will either use DDL3s to connect to online computing system or GBT data FE-links to the CRU, # = these detectors need a trigger at L0 latency and can additionally use L1, FTL..fast serial trigger link.)

Level	Trigger Input to CTP [ns]	Trigger output at CTP [ns]	Trigger decision at detector * [ns]	contributing detectors
LM	425	525	775	FIT
L0	1200	1300	1500	ACO, EMC, PHO, TOF, ZDC
L1	#6100	#6200	#6400	EMC, ZDC

Table 4.2: Latency and contributors of the different trigger signals. * = signal arrival time at detector not including internal distribution to front-end electronics (the values reported here are indicative: differences among detectors exist due to their actual location and more details are provided in the detector chapters when relevant). #= EMC L1 latency is based on Run1 implementation, which will be shortened for the upgrade.

Detector	# CTP inputs	time-of-flight [ns]	processing [ns]	cabling [ns]	cable to CTP	total [ns]
FIT	2	12	192	175	46	425
ACO single/mult	3	110	75/125	160	240	585/635
EMC-L0/PHO-L0	1	15	732	0	96	843
EMC-L1	4					#6100
TOF-L0	6	12	800	0	50	862
ZDC-ZNA-L0	1	375	92	694	5	1166
ZDC-ZNC-L0	1	375	92	549	5	1021
ZDC-L1	4	375	268	966	500	2110

Table 4.3: Trigger input latency. #= EMC L1 latency is based on Run1 implementation, which will be shortened for the upgrade. ZDC-ZNA/C-L0 signals arriving from A/C side of ALICE.

successful only if every one of a list of read-out detectors (trigger cluster) was available to read out the data. The association between trigger cluster and trigger condition defines a trigger class [22]). For the upgrade, if a trigger condition is satisfied, the event is read out with the continuous read out detectors, plus all other available detectors. This strategy in effect treats each detector as a separate cluster. At the same time, the busy requirements of every detector can be treated independently of other detectors. It could turn out that this strategy would lead to insufficient numbers of events being read out with useful combinations of detectors without multi-event buffer. To allow for this possibility, the trigger logic can, in addition, define further clusters consisting of groups of detectors, as at present, and will balance the bandwidth between a free selection of all available detectors and a restricted choice requiring a given combination.

4.3 Central Trigger Processor implementation

The functions discussed in the previous section will be implemented in a new CTP board combining the functions of the current CTP BUSY, L0, L1 and FO boards. This obviates the need to transfer data across the backplane and therefore eliminates the CTP dead-time. The application of a modern FPGA such as the XILINX-7-series KINTEX FPGA, provides sufficient memory to reproduce and extend the snapshot facilities of the current CTP. In particular, the CTP will be provided with 1 GB of DDR3 memory, partitioned so as to allow adequate storage of snapshot data, with reserved space for future applications.

The XILINX-7 series also provides a facility for automatic recovery from radiation induced single and double event upsets for configuration. It is self-correcting after a CRC check. Since the CTP will be placed in a site of only moderate radiation (see Tab. 3.1), this automatic recovery procedure is sufficient for the CTP operation [23].

The board will have a DDL3 link to the computing system for transmission of interaction records and trigger data. Interaction records consist of a series of records listings of each each orbit and the interactions which occur in it. The trigger data for every L0 and L1 trigger consist of event identification, trigger class mask and detector mask (bit patterns describing the active classes and the detectors being read out in an event). A second 1 Gb/s optical ethernet link is available for DCS for configuration, control and monitoring, using the IPbus protocol.

The CTP will also communicate with up to 24 Local Trigger Units (LTUs), one for each ALICE detector, using custom high speed serial links. The LTU is described in the next section.

4.4 Local Trigger Unit implementation - LTU

The Local Trigger Unit combines the functions of transmission of trigger signals and emulation of the CTP for use in detector development (i.e. standalone mode), in a way similar to that implemented in the current LTU [24]. The LTU will have the possibility to send trigger signals to detectors via the fast serial links or the TTC protocol. For the fast serial links, there will be ten separate bi-directional links which can also be used for upstream busy collection. In the TTC case, the LTU optical links will provide the optical signal according to TTC protocol and busy is propagated by dedicated LVDS cables. In addition, there will be provision for clock, orbit and external trigger inputs, especially useful in standalone running. Monitoring and control will be provided by a 1Gb/s optical Ethernet link using the IPbus protocol.

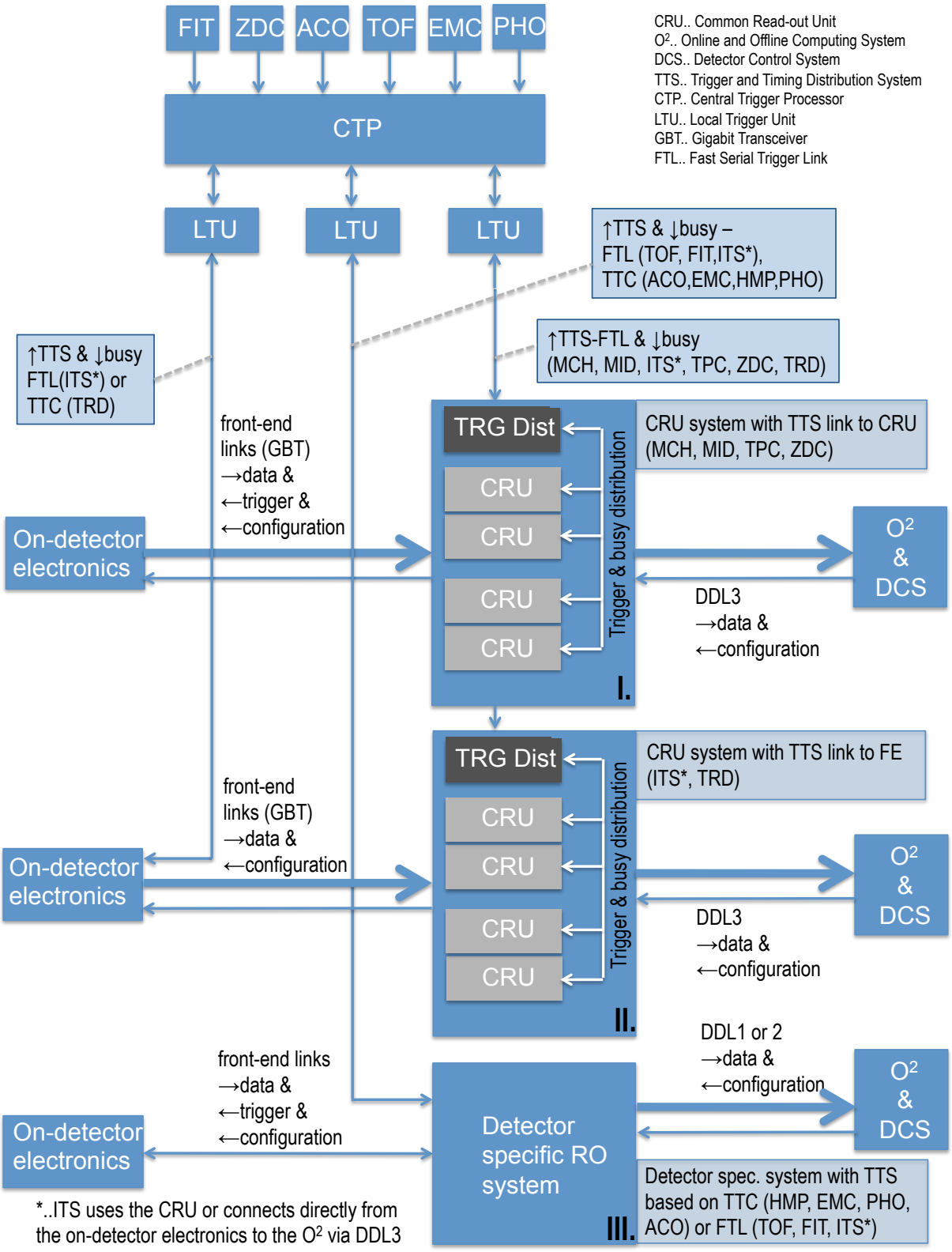


Figure 4.1: ALICE system block diagram.

Detector	TTS links	type	Position trigger interface
TPC	7	FTL	CR
MCH	1	FTL	CR
ITS	184	FTL	Cav
MID	1 & 1	FTL	CR/Cav
ZDC	1 & 1	FTL	CR & Cav
TOF	72	FTL	Cav
FIT	1	FTL	CTP area
TRD	1 & 1	FTL & TTC	CR/Cav
EMC	1	TTC	Cav
PHO	1	TTC	Cav
HMP	1	TTC	Cav
ACO	1	TTC	Cav

Table 4.4: TTS connections to detector systems. CR..Counting Room, Cav..Cavern, FTL..fast serial trigger link.

4.5 Trigger and Timing distribution System - TTS

Three different types of links are used for trigger distribution. The LM trigger signal is distributed by a copper LVDS cable to the TRD, satisfying the low latency requirement. As can be seen from Tab. 4.1, two basic types of link will be used for the transmission of trigger signals and data at L0 and L1 levels. Detectors upgrading their TTS interface will use fast serial links, while the other detectors continue to use the TTC system.

4.5.1 TTS via fast serial trigger links (FTL)

The synchronous trigger signals at L0 and L1 levels will be followed by a trigger message containing event identification.

With respect to the distribution links, the detectors using the fast serial trigger protocol are considered individually, as there are several distinct cases, as shown in Tab. 4.4. For the TPC, MCH, MID and ZDC, the distribution of trigger signals will use the CRU. The reception of trigger signals is not time-critical. The design of the system implies that under nominal operation conditions it does not get busy. The detector only gets busy in case of an error condition or during operation under non-nominal conditions. Thus, the busy transmission is not time-critical and generating the busy signal at the level of the CRU is sufficient. Consequently, bi-directional trigger links connect the CTP with the counting room-located CRU. Table 4.4 shows the number of required TTS links. Even for the TPC, only seven links are needed, which corresponds to the number of ATCA crates estimated.

The trigger latency of the ITS detector is time critical. In this case, a propagation detour via the counting room is avoided by directly routing the links from the CTP to the 184 mini-frame-located ITS read-out boards. The busy signal transmission is done via the data links.

TRD front-end electronics still uses a trigger interface based on TTC, whereas the CRU-based read-out electronics uses fast serial TTS links. TOF and FIT will upgrade the TTS interface to fast serial links.

4.5.2 TTS via TTC

The restricted bandwidth of the TTC transmission channel used to transport trigger messages (B-channel) dictates the format for the transmission of trigger signals and data. While in Run1 and Run2 the bulk of the trigger data was transmitted to each TTC destination as a broadcast message in the B-channel, the increased interaction rate in the upgraded system means that this strategy would lead to excessive delays before the data could be transmitted. Instead, a synchronous trigger will be generated (in the latency constant A-channel) and only the 12 least significant bits of event identification will be transmitted in the B-channel, asynchronously. The full trigger data will be transferred as CTP read-out, and attached to the data at the event-building stage.

4.6 Software triggers

The CTP will provide several different types of triggers in addition to physics triggers, i.e. those which are initiated by coincidences between different trigger inputs. The software triggers are initiated by a request from the CTP trigger processor. There are two types of software triggers. An asynchronous trigger is generated at the moment the trigger request is issued. A synchronous trigger is issued at a specific selected bunch crossing.

During data taking, detectors will require a number of different types of calibrations. These can be fulfilled by generating a special class of triggers called calibration triggers. Calibration triggers are treated as a special class of software triggers, allowing the generation of a calibration pulse before the read-out triggers are sent [25].

For the upgrade, in addition, the heartbeat software trigger (see section 2.3.1) will be provided to designate the boundary between two data frames for continuous read-out detectors and to provide a synchronisation check for local LHC counters.

	Unit cost [kCHF]	Number of units	Cost [kCHF]
CTP	32	3	95
LTU	36	5	180
Crate	10	3	30
Optical splitter	1	10	10
Total			315

Table 4.5: CTP cost estimate.

Date	Item
2014/15	Design Specification
2016	LTU design & construction
2017	LTU delivery
2017	CTP design & construction
2018	CTP delivery
2018	Installation & commisioning

Table 4.6: CTP schedule.

4.7 Schedule, funding and institutes

The cost estimate for the trigger system consisting of CTP, LTU and optical splitters is given in Tab. 4.5.

University of Birmingham will take responsibility of the system design, implementation, production and installation. Table 4.6 shows the schedule for upgrade development items.

5 TPC/MCH read-out ASIC - SAMPA

Operating the time projection chamber (TPC) at a Pb-Pb collision rate of 50 kHz requires the present limitations imposed by the operation of the gating grid to be overcome. Thus, the present multi wire proportional chamber (MWPC)-based read-out chambers will be replaced by gas electron multiplier (GEM) detectors, which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As the drift time will be higher than the average time between interactions, a triggerless, continuous read-out is implemented. This implies the upgrade of the existing front-end ASICs to a new read-out ASIC, the SAMPA ASIC, providing continuous read-out.

Furthermore, in order to operate the muon chambers (MCH) with an interaction rate of 50 kHz, the present front-end electronics cannot be used and will be replaced by the SAMPA ASIC. The SAMPA ASIC adapts to the different detector signals with programmable parameters.

The SAMPA ASIC is an evolution of the presently used TPC front-end electronics, where front-end amplifier and shapers sit in the 16-channel PASA ASIC [7][26]. The 16-channel ALTRO [8] chip digitises, processes, compresses and stores the data in a multi-event memory. The Analog-to-Digital converters embedded in the chip have a 10-bit dynamic range and are used in the TPC at 10 MHz. After digitisation, a pipelined Data Processor is able to remove from the input signal a wide range of perturbations related to the non-ideal behaviour of the detector, temperature variation of the electronics and environmental noise. Moreover, the Data Processor is able to suppress the pulse tail within 1 μs after the peak with 1 % accuracy. The signal is then compressed by removing all data below a programmable threshold, except for a specified number of pre- and post-samples around each peak. This produces non-zero data packets. Eventually, each data packet is marked with its time stamp and size - so that the original data can be reconstructed afterwards - and stored in the multi-event memory. A further evolution of the system is the S-ALTRO ASIC [9]. The architecture is based on the ALTRO ASIC. The main difference is the integration of the charge shaping amplifier in the same ASIC. The SAMPA ASIC will integrate 32 channels of the full data processing chain and support continuous and triggered read-out. The design of the SAMPA has already been started, taking the additional specifications compared to its predecessors into account. Tab. 5.1 summarises the SAMPA specifications.

5.1 System overview

SAMPA contains positive/negative polarity Charge Sensitive Amplifiers (CSA), which transform the charge signal into a differential semi-Gaussian voltage signal that is digitised by a 10-bit up to 20 Msamples/s ADC. After the ADC, a digital signal processor eliminates signal perturbations, distortion of the pulse shape, offset and signal variation due to temperature variations. SAMPA contains 32 channels per chip that concurrently digitise and process the input signals. Fig. 5.1 show the SAMPA block diagram. The data read-out takes place continuously at a speed of up to 1.28 Gbps by four 320 Mb/s serial links [14].

Specification	**TPC**	**MCH**
Voltage supply	1.25V	1.25V
Polarity	Positive/Negative	Positive/Negative
Detector capacitance (Cd)	18.5pF	40pF - 80pF
Peaking time (ts)	80ns or 160ns	300ns
Shaping order	4th	4th
Equivalent Noise Charge (ENC)	< 536e@ts=80ns* or < 482e@ts=160ns*	< 950e @ Cd=40p* < 1600e @ Cd=80p*
Linear Range	100fC or 67fC	500fC
Sensitivity	20mV/fC or 30mV/fC	4mV/fC
Return to baseline time	<164ns@ts=80ns or <288ns@ts=160ns	<541ns
Non-Linearity (CSA + Shaper)	< 1%	< 1%
Crosstalk	< 0.3%@ts=80ns or < 0.2%@ts=160ns	< 0.2%@ts=300ns
ADC effective input range	2Vpp	2Vpp
ADC resolution	10 bit	10 bit
Sampling Frequency	10 Msamples/s or 20 Msamples/s	10 Msamples/s
INL (ADC)	<0.65 LSB	<0.65 LSB
DNL (ADC)	<0.6 LSB	<0.6 LSB
SFDR (ADC)**	68dBc	68dBc
SINAD (ADC)**	57dB	57dB
ENOB (ADC)	9.2-bit	9.2-bit
Power consumption (per channel)		
ADC	2mW (4mW)	2mW (4mW)
CSA + Shaper	6mW	6mW
Channels per chip	32	32

*$R_{esd} = 70\Omega$
** @ 0.5MHz, 10 Msamples/s

Table 5.1: Specifications of the front-end ASIC (SAMPA).

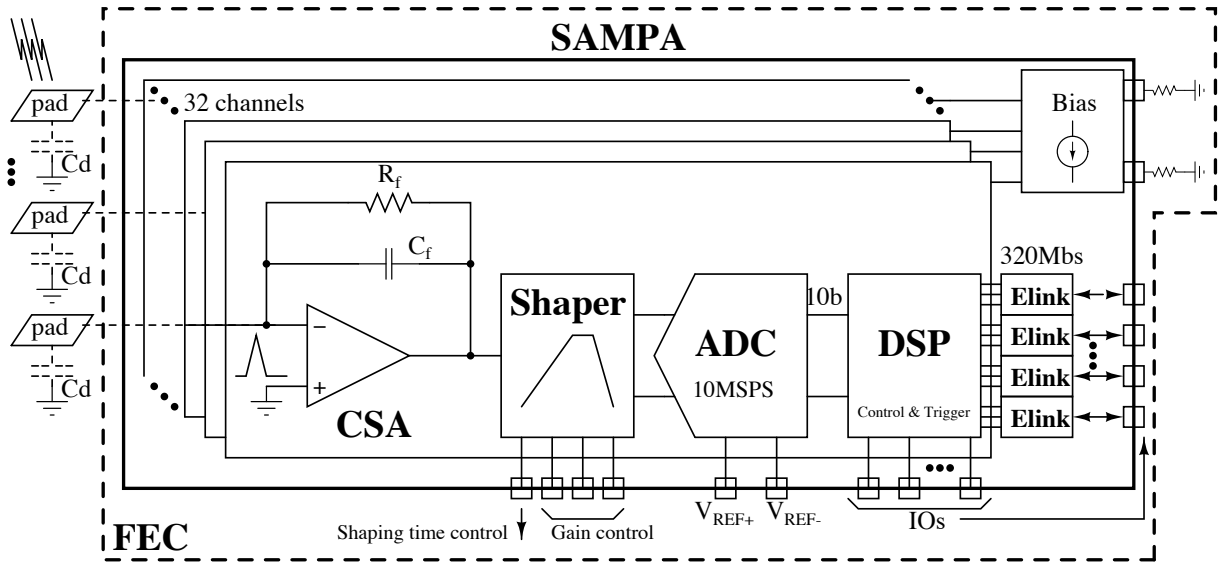


Figure 5.1: SAMPA system block diagram

The data read-out can be performed in continuous mode or triggered mode. In continuous mode, the read-out is performed triggerless if the input signal exceeds the programmable threshold value. For the TPC application, a design rate of 50 kHz with 30 % occupancy is assumed. For the MCH, the design rate is 100 kHz and 10 % occupancy. Software triggers are accepted during read-out in continuous mode for calibration and synchronisation purposes. In triggered mode, data read-out is performed only upon reception of an external trigger with a maximum latency of 9.6 μs. Triggers arriving during an active read-out will be accepted. In that case, the active read-out will be extended by the new arriving trigger, and status information is sent to acknowledge the read-out extension. Optionally, a programmable number of pre/post-samples before/after the input signal crossed the threshold in continuous mode or the external trigger mode arrived can be read out.

5.2 ASIC building blocks

The SAMPA ASIC is composed of a positive/negative polarity Charge Sensitive Amplifier (CSA) with a capacitive feedback C_f and a resistive feedback R_f connected in parallel, a Pole-Zero Cancellation (PZC) network, a high pass filter, two bridged-T second order low pass filters, a non-inverting stage, a 20 Msamples/s 10-bit ADC and a Digital Signal Processor(DSP) block, as shown in Fig. 5.2. The first shaper is a scaled-down version of the CSA and generates the first two poles and one zero. A copy of the first shaper connected in unity gain configuration is implemented in order to provide a differential mode input to the next stage. The second stage of the shaper is a fully differential second order bridged-T filter and it includes a Common-Mode Feed-Back network (CMFB). The non-inverting stage adapts the DC voltage level of the shaper output to use the full dynamic range of the ADC. It consists of a parallel connection of two equally designed Miller compensated amplifiers. The ADC is a differential 10-bit 20 Msamples/s SAR (successive approximation) ADC implemented with a low power switching technique. The DSP part is composed of digital filters, a data format unit, a ring buffer, a trigger manager block, a configuration register bank, a control state machine and four 320 Mb/s serial links. The chip will be fabricated in 0.13 μm CMOS technology.

5.2.1 Front-end

Since the charge (Q_i) delivered by the TPC or MCH detectors is very small and short (typically 7 μA during 1 ns), it is unsuitable for immediate signal processing. Therefore, the input signal is first integrated and amplified by the CSA, producing at its output a voltage signal (V_{CSA}) whose amplitude is proportional to the total charge Q_i and is characterised by a long decay time constant $\tau = R_f \cdot C_f$. The CSA shaping time can be configured to values of 80 ns and 160 ns for the TPC and 300 ns for the MCH. The sensitivity can be set to 20 or 30 mV/fC for the TPC and 4 mV/fC for the MCH by two external pins. The C_f values are adapted to the three shaping times (ts) modes available and are 600 fF@ts=80 ns, 1.2 pF@ts=160 ns and 2.4 pF@ts=300 ns, which are defined by the gain and linear range requirement. The R_f value of $6M\Omega$ is defined by the noise specification [26][27]. The relatively long discharge time constant of the CSA (τ) makes it vulnerable to pile-up. The low frequency part of the pulse is then removed by the high pass filter ($C_{dif} \cdot R_{dif}$). Due to the exponential decay of the CSA feedback network in combination with the differentiator network (R_{dif}, C_{dif}), an undershoot is created at the shaper output with the same time constant as the CSA of $\tau = R_f \cdot C_f$. This undershoot is removed by creating a pole-zero cancellation circuit by adding a resistance R_{pz} in parallel to the capacitor C_{dif} in the differentiator stage. It creates a Zero in the transfer function that cancels

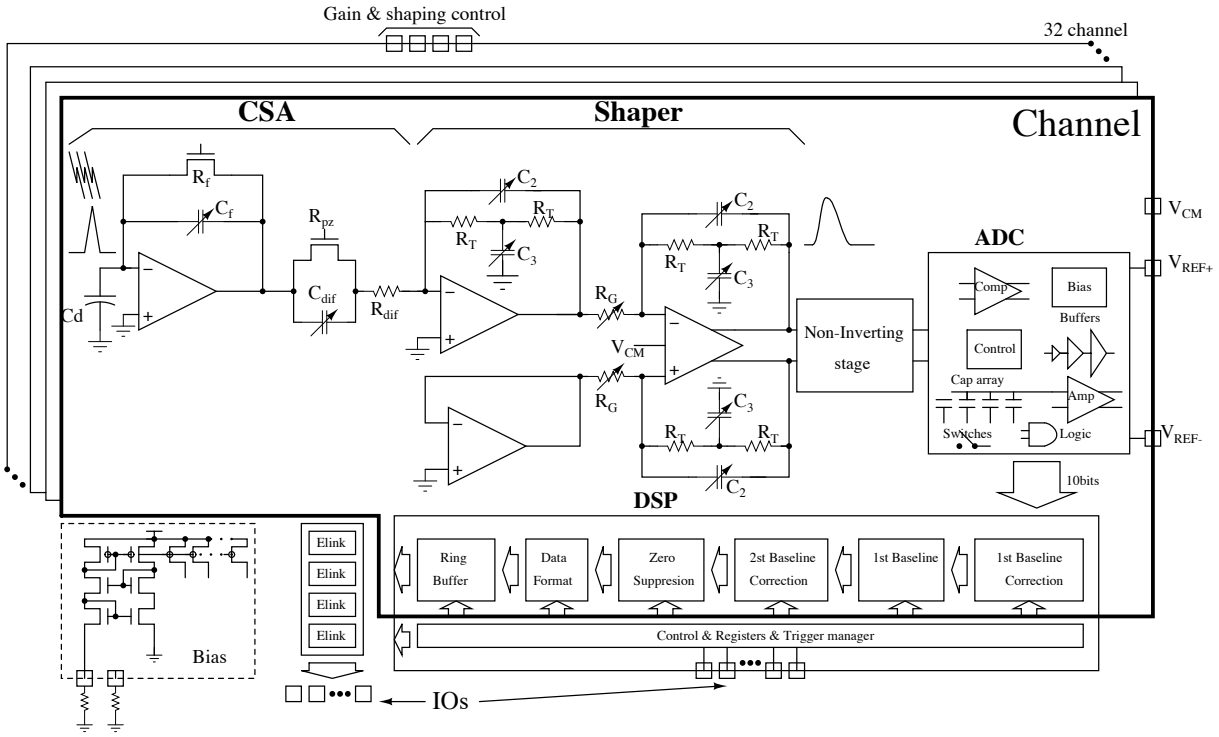


Figure 5.2: Detailed SAMPA block diagram.

the low frequency pole introduced by the CSA feedback network [28][29]. The chosen topology of the CSA amplifier (Fig. 5.3) is based on a single-ended folded cascode amplifier followed by a source follower. The CSA has been optimised for the specification of detector capacitance and shaping time listed in Tab. 5.1.

As shown in Fig. 5.3, switches S_1-S_2 are used to adjust capacitances C_f and S_3 - S_4 to adjust C_{dif} for each case of peaking time. The capacitors of the T-bridge network of the semi-Gaussian shaper are adjusted for 80 ns, 160 ns or 300 ns of shaping time, achieved by placing additional capacitors in parallel. It is performed with switches based on NMOS and PMOS transistors, sized to provide low series resistance. The required sensitivity is controlled by R_G trimming (Fig. 5.2) which is made by putting additional resistances in parallel. The maximum amplitude of the output pulse is 2 Vpp. The output pulse waveform of the semi-Gaussian shaper is shown in Fig. 5.4 for 160 ns of shaping time (20 mV/fC of sensitivity) and 300 ns of shaping time (4 mV/fC of sensitivity).

The CMFB network of the second shaper stage establishes a stable common-mode voltage V_{CM} of 600 mV at the output of the second shaper. The chosen CMFB network consists of a resistor-capacitor network. This configuration takes the average of the two amplifier outputs and compares it with an externally given voltage V_{CM} and adjusts the polarisation current of the first stage of the amplifier.

A capacitive successive approximation (SAR) topology is used to design the 20 Msamples/s 10-bit full differential ADC. The block diagram of the ADC is shown in Fig. 5.5. The main parts of the circuit are: capacitive array, switches, comparator and the SAR control logic. The capacitor array samples and holds the analog value and performs the digital to analog conversion. A switching strategy with low energy dissipation per cycle is utilised.

The chip will be fabricated in TSMC 0.13 μm CMOS technology with a nominal voltage supply of 1.2 V. The analog blocks and digital blocks will have separate supply pads (voltage supply and

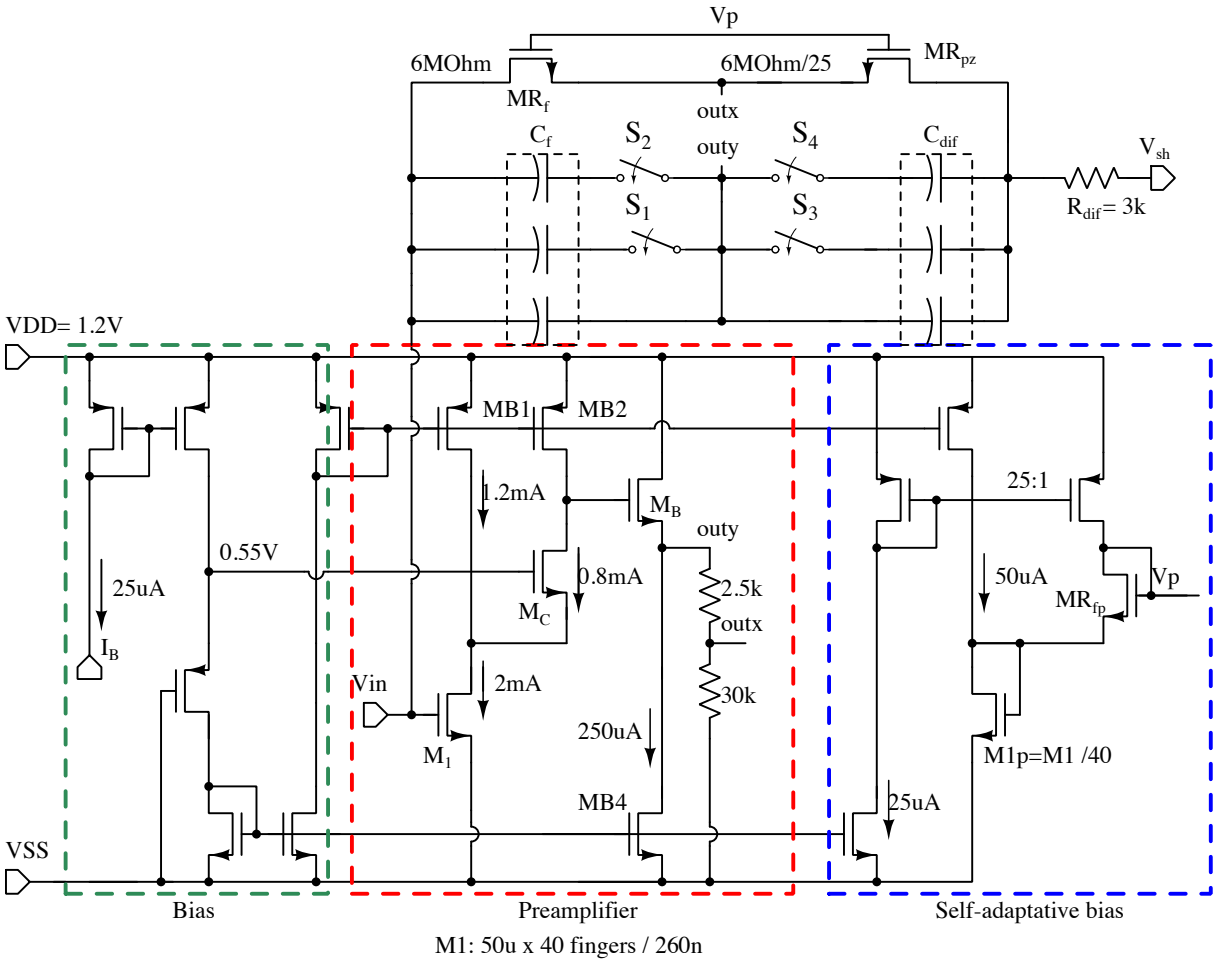


Figure 5.3: Transistor level schematic of the CSA.

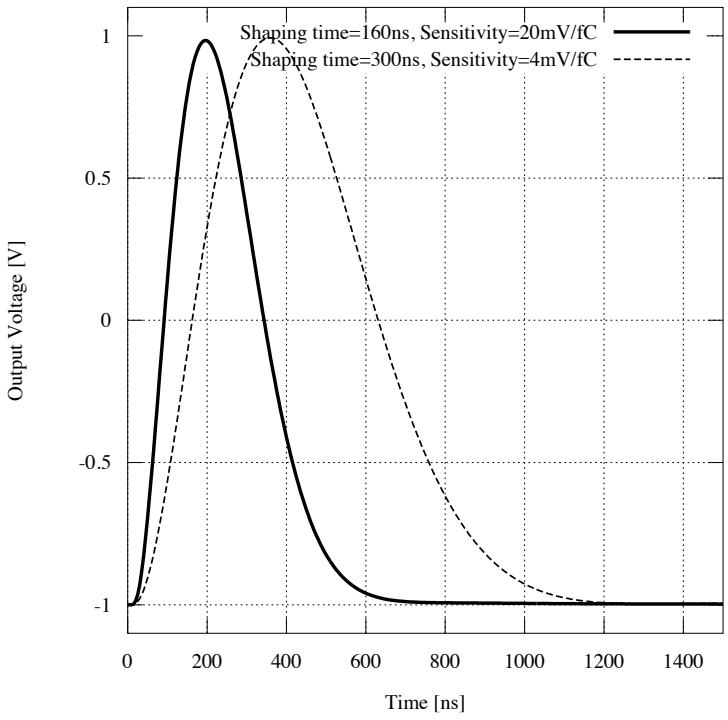


Figure 5.4: Output pulse waveform of the semi-Gaussian shaper.

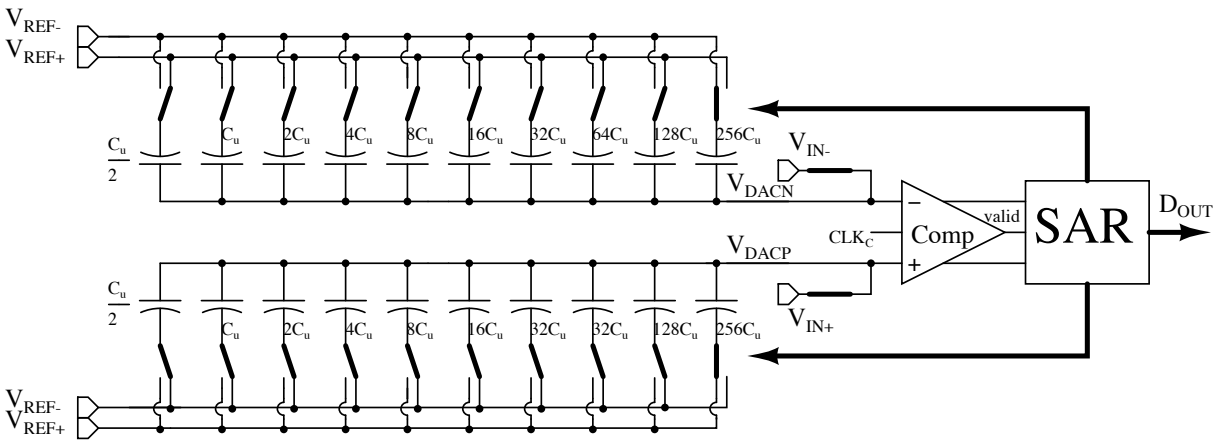


Figure 5.5: The block diagram of the 10b SAR ADC

ground) with high isolation to avoid digital noise coupling. A 25 μA stable current is generated on chip to bias the CSA and the Semi-Gaussian shaper (32 channels). An external resistor of high precision is used to control the bias current value. Another external resistance is used to control the bias of the ADC. It minimises switching noise coupling from the ADC.

5.2.2 Digital signal processing

The signal processing is performed in 4 steps: a first correction and subtraction of the signal baseline, the cancellation of long-term components of the signal tail, a second baseline correction and zero suppression.

The purpose of the first baseline correction (BC1) is to decrease noise and systematic error effects. This block has two operation modes: subtraction mode and conversion mode. The subtraction mode consists of subtracting a value from the input (D_{in}). This mode is divided in three kinds:

- Fixed: subtracts a constant value, called fixed pedestal, set previously in a register.
- Time dependent: is available in triggered mode only and subtracts a variable value which is stored in the pedestal memory (4096 x 10 bit). The values are accessed from first to last, so the order of the subtractions is the same for every processing window.
- Self-calibrated: a baseline value is calculated outside the processing window. It is called variable pedestal (V_{pd}), and its calculation is performed by an infinite impulse response (IIR) filter. If this option is selected, the filter is activated receiving as input D_{in} and providing $D_{in} - V_{pd}$ as output.

The conversion mode uses the input data to address the pedestal memory, giving the output as a function of V_{in}.

The Tail Cancellation Filter (TCFU) is a 4-stage IIR filter used to cancel a slowly varying signal. The signal rise time is fast, but its fall time is much slower and has a rather complex shape that varies from pad to pad.

The second level of baseline correction (BC2) is applied to the signal during the PTW (Processing Time Window) and corrects signal perturbations created by non-systematic effects. The

threshold values have a constant component which is the same for the whole chip and a variable component which is channel specific so it must be set individually for each of the channels.

The zero suppression (ZSU) block eliminates data below a programmable threshold. An option to switch off the zero suppression is foreseen.

5.3 Read-out

SAMPA supports two read-out modes: continuous mode and external triggered. In continuous mode when the programmable threshold is exceeded in one channel this channel is read out automatically. In triggered mode, upon reception of the external trigger, a 1024-sample long time frame is started. Those channels which exceed the threshold during this time frame will be read out. The trigger is sent either via an external pin or via an instruction with maximum latency of 9.6 μs. In both modes, when the zero suppression mode is activated, data samples above the threshold will be read out. Thus, triggered mode can be seen as a sub-mode of continuous mode, where data samples are read out only if the external trigger signal has been provided.

Subsequent ADC data samples above threshold are called a cluster. The programmable number or pre/post-samples defines the number of ADC samples added to the cluster before/after the signal passed above/below the threshold. The number of pre/post samples are common to the 32 channels. When small signals are sampled and the digitised values are close to the threshold, the scheme of assembling the data samples into clusters results in a high number of clusters and an inefficient data format. Thus, two clusters separated by up to two samples below threshold are merged to each other.

In continuous read-out mode, a new time frame is started immediately after the preceding frame has finished. Thus, every 1024 ADC clock cycles, a 1024-bin long time frame is initiated. All 32 channels of the SAMPA use the same time frame. The sync input of the SAMPA sets the start time of a time frame and thus allows in the TPC/MCH systems to align the time frames of all SAMPA ASIC with respect to each other.

In triggered read-out mode, the time frame starts upon an external trigger and thus is again synchronous for all channels in the ASIC. If the trigger is sent to all SAMPAs in the systems at the same time, the time frames in all SAMPAs in the system are also synchronous to each other. Fig. 5.6 illustrates the concept of time frames.

In triggered operation, if a trigger is issued during an active read-out, the active read-out time frame is terminated and a subsequent full length read-out cycle is immediately started. Provided the interaction rate does not exceed specifications, no data loss occurs. In case a heartbeat trigger is registered during an active read-out, a dedicated header acknowledging the heartbeat trigger with the bunch crossing identification number at the reception of the heartbeat trigger is sent after the active read-out time frame.

Provided the average interaction rate and occupancy does not exceed specifications, the SAMPA buffers do not overflow and the ASIC does not get busy as the SAMPA is specified for continuous read-out. However, during operation the interaction rate or occupancy might get too high for the design read-out rate. In that case, the SAMPA data buffers will overflow. The SAMPA read-out controller will truncate the read-out packets of a time frame, balance the read-out buffers and inform the CRU via the data header that truncation occurred. The CRU forwards status information to the CTP which throttles or stops the triggers. This transmission via the

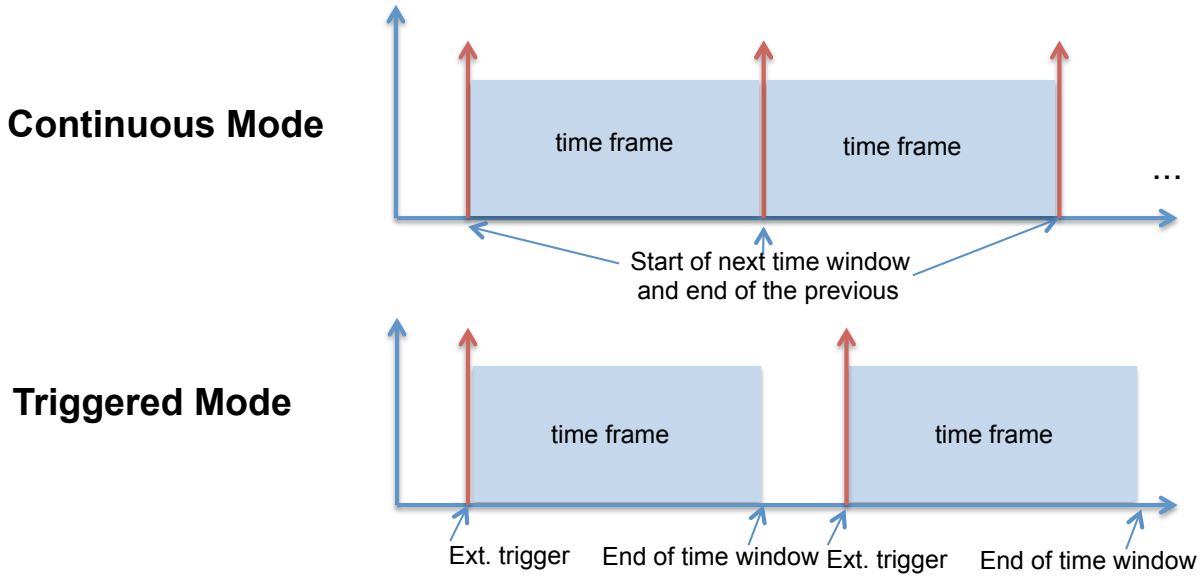


Figure 5.6: Time frame concept.

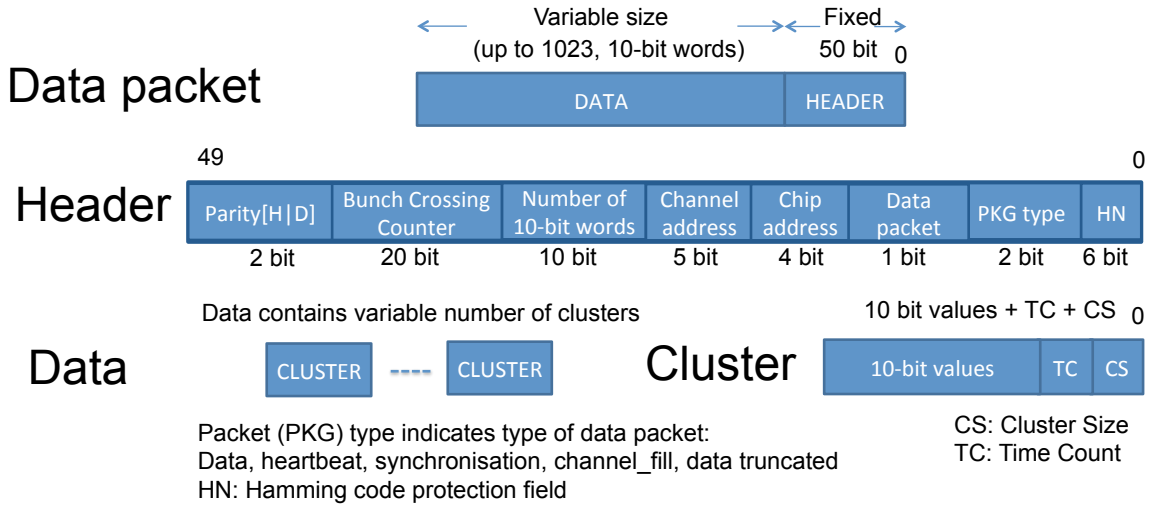


Figure 5.7: Data packet format.

CRU to the CTP is slower than a dedicated busy link from the TPC/MCH front-end to the CTP but completely sufficient for this purpose.

Data from each time frame are assembled in one data packet. Fig. 5.7 shows the read-out data packet format. A data packet consists of a header word followed by the hit data information. The 50-bit header contains the bunch crossing counter, the channel and chip address and the hamming code protecting the number of hit data words which follow. The variable number of 10-bit data words contain the number of samples in the cluster, the time stamp with a binning of one ADC sampling period and the ADC sampling values. In case no hits have been registered, the header will be followed by channel_fill patterns. For off-detector synchronisation, a special synchronisation pattern is sent after reset and upon instruction. The header contains the packet type field, giving information whether the data packet contains normal data, synchronisation fields, channel_fill patterns or whether the data stream has been truncated because of an early arrival of a trigger or buffer overflow.

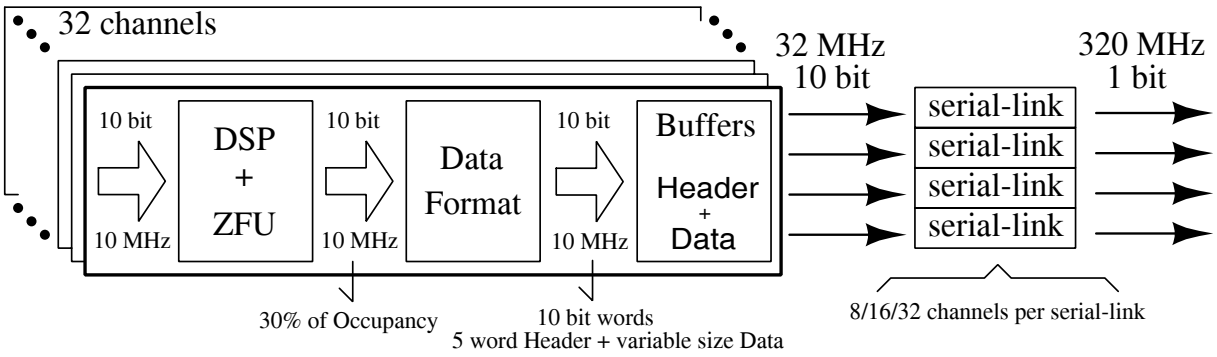


Figure 5.8: Data block diagram.

The off-chip data read-out is based on four serial links which can be operated at 320 Mb/s, 160 Mb/s or 80 Mb/s, each connected to the read-out FIFOs of 8 channels. In the SAMPA, the read-out controller polls the data from the channels and reads them out in a round robin-based fashion. As base-line, the size of the channels FIFOs has been set to 16 time frames (16k x 10 bit) for each channel.

The TPC application defines the maximum data band width. It is designed for a channel occupancy of 30 % and a sampling rate of 10 MHz. Given the 32 channels * a sampling rate of 10 MHz * a word length of 10 bit * 30 % occupancy, a data rate of 960 Mb/s per ASIC or 240 Mb/s per serial link needs to be accommodated. The 320 Mb/s serial links offer sufficient margin for transmission overhead.

In order to adapt the number of serial link outputs to application data rate, the hit data can be routed through either all 4, 2 or 1 serial links, programmable via instruction. Furthermore, data from neighbouring ASICs can be routed through a SAMPA (daisy chained read-out) to further decrease the number of output links in system. An additional serial input is available for this purpose. In the MCH application, this allows daisy chaining two SAMPA ASICs and the read-out of one front-end card by one single serial link only.

For pedestal runs, where the zero suppression is deactivated, the read-out is stopped when the buffers are full and restarted once they have been read out.

When the SAMPA is operated together with the GBTx serialiser ASIC, it receives a 40 MHz alignment clock (clk_GBTalignment) from the GBTx. This signal is used to align the SAMPA word boundaries to the transmission phase of the GBTx.

For test purposes of the detector system and the online computing system, SAMPA allows the transmission of pre-programmable data sequences. The SAMPA data flow block diagram is shown in Fig. 5.8. The SAMPA configuration and status registers are accessed via an I2C interface.

5.4 ASIC I/Os

Fig. 5.9 shows the IO connections of the SAMPA. All the digital IOs of the SAMPA ASIC are differential SLVS ports with the exception of the CMOS hard-coded configuration pins. Table 5.2 shows the SAMPA IOs.

The sensitivity and shaping time programming options of the ASIC are listed in Tab. 5.3.

SAMPA IO
Digital inputs: **Clocks:** There are three different clock inputs: clk_serial, clk_ADC, clk_GBTalignment. Optionally clk_ADC and clk_GBTalignment can be derived from clk_serial internally or provided via the input pins.
clk_serial: 320/160/80 MHz, a jitter of less than 30 ps RMS is expected. **clk_ADC:** 10/20 MHz, this clock is either derived from the serial clock or taken from this input. The phase of the ADC clock can be adapted to the GBT alignment clock. **clk_GBTalignment:** 40 MHz, this signal allows alignment to the GBT transmission word phase. **config_clk:** hardwired pins to select whether the clocks are provided externally or are derived from clk_serial.
Digital control: **Reset global:** resets all registers. **Sync:** This signal resets the internal event counter, the time stamp and defines the time frame start. **Trigger:** external trigger signal, synchronised to ADC sampling frequency with programmable phase. **Heartbeat trigger:** external trigger signal, synchronised to ADC sampling frequency with programmable phase. **Address:** 5-bit hard-coded address field which can be read via the configuration ports and is added to header information.
Digital data input: **Serial link data input:** allows merging data stream of neighboring ASIC.
Digital outputs: **4 serial link outputs:** 320/160/80 Mbit/s data stream.
Status outputs: **Status read-out active signal:** is active when at least one channel is above threshold. **Status buffer full signal:** is active, when buffers in the ASIC are full, data loss occurs and data read-out is truncated.
Configuration: **I2C interface.**
Analog inputs: **32 Detector inputs:** 32 pins.
Analog settings: **Sensitivity control (gc0 and gc1):** 2 pin. This value also can be programmed by instruction. **Shaping time control (ptc0 and ptc1):** 2 pin. This value also can be programmed by instruction. **External bias resistances:** 2 pins. **Reference voltages (V_{REF-}, V_{REF+}):** 2 pins. **Common voltage (V_{CM}):** 1 pin. For the references an internal reference cell is foreseen. The external pins allow overriding of the internal values.

Table 5.2: SAMPA IO.

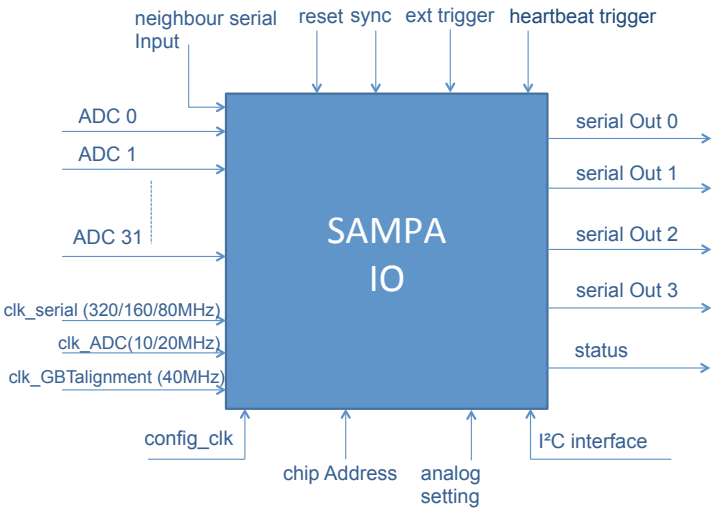


Figure 5.9: SAMPA IOs.

ptc0	ptc1	gc0	gc1	Shaping time	Sensitivity
0	0	0	0	160ns	30mV/fC
0	0	1	0	160ns	20mV/fC
0	0	0	0	80ns	30mV/fC
0	0	1	1	80ns	20mV/fC
1	1	1	1	300ns	4mV/fC

Table 5.3: Gain and shaping time programming options of the ASIC.

5.5 Schedule, funding and institutes

The project schedule is presented in Tab. 5.4. Before the final production two multi-project wafer (MPW) prototyping ASIC productions are needed and a third run is reserved if required. The first run will contain each block individually and a complete version of four channels (preamplifier, shaper, ADC and digital blocks). The test boards will be designed and implemented by Polytechnic School of the University of Sao Paulo and the ALICE collaboration. The radiation tolerance test will be performed by the Nuclear Physics Department of USP and University of Oslo. Tests involving chamber prototypes will be conducted by the TPC and MCH teams. A second MPW run contains the full functionality of all 32 channels.

Date	Activity
2014 Q1	Definition of analog/digital specifications
2014 Q2	Design & submission of MPW1 (4 ch.)
2014 Q2	Design & production of test setup
2014 Q4	Design & submission of MPW2 (32 ch. & full digital funct.)
2015 Q2	Design & submission of MPW3 (clean-up)
2015 Q4	Fabrication of final Version
2016 Q1	Delivery of pre-production
2016 Q2	Delivery of production quantity

Table 5.4: SAMPA schedule.

Activity	Material Cost [kCHF]	Manpower Cost [kCHF]	Total Cost [kCHF]
1. ASIC Design	255	80	335
2. ASIC Tests			
2.1 Validation Tests	78	110	188
2.2 Detector Oriented Tests	145	135	280
2.3 Radiation Hardness Tests	50	16	66
3. Production (83000 ASICs)			
3.1 Production - Engineering (12 wafers)	280		280
3.2 Production - Construction (283 wafers)	499		490
3.3 Acceptance Tests	120		120
Contingency (20 %)	285		285
Total	1712	341	2053
Packaged and tested ASIC out of 58000			
with additional man power cost	35.4 CHF		
without additional man power cost	29.5 CHF		

Table 5.5: SAMPA cost estimate.

Institutes
EPUSP, Escola Politécnica, Universidade de São Paulo, Brazil
IFUSP, Instituto de Física, Universidade de São Paulo, Brazil
IFGW, Instituto de Física Gleb Wataghin, Universidade Estadual de Campinas, Brazil
University of Bergen, Norway
University of Oslo, Norway
IPNO, Institut de Physique Nucléaire d'Orsay, Université de Paris-Sud, IN2P3/CNRS, France
SPhN, Service de Physique Nucléaire , CEA-IRFU Saclay, France

Table 5.6: SAMPA Institutes.

Tab. 5.5 shows the cost estimate for the SAMPA project. The estimate is based on preliminary TSMC pricing information available via the CERN frame contract and includes 3 multi project wafer (MPW) productions, 1 engineering run, design, construction of test setups, radiation tests and outsourced man power. An ASIC size of 90 mm^2 and a conservative yield of 70 % is assumed. The estimate is based on the production of 83000 ASICs. TPC and MCH need 51000 ASIC plus 15 % spares. Table 5.6 shows the involved institutes.

6 Muon Tracking Chambers - MCH

6.1 Introduction

The muon chambers (MCH) consist of 156 multi-wire proportional chambers with more than one million electronic channels. In order to support the interaction rate of 50 kHz, the design read-out rate has been set to 100 kHz as safety margin. Approximately 34000 front-end ASICs and 17000 front-end cards need to be replaced and are connected via $\approx$ 500 GBT optical links to the common read-out (CRU). The front-end read-out uses the SAMPA ASIC, which supports triggered and continuous read-out.

6.2 The present system

The muon chambers are based on multi-wire proportional chambers with cathode pad read-out, the so-called Cathode Pad Chambers. The system consists of 5 tracking stations, with each station composed of 2 chambers. Because of the different sizes of the stations (ranging from few square metres for station 1 to more than 30 m^2 for station 5), two different designs were adopted. The first two stations are based on a quadrant structure [30], with the read-out electronics distributed on their surface (see Fig. 6.1, left). Four independent quadrants constitute one chamber. For the bigger stations, a slat architecture [31] was chosen (see Fig. 6.1, right). The maximum active size of a slat is 40 $\times$ 240 cm^2 and the electronics is implemented on the top and bottom part of each slat. Slats are mounted on a frame support to constitute one half-chamber. One half-chamber consists of 9 slats for station 3, and 13 slats for stations 4 and 5. The total number of detectors is 156, 140 slats and 16 quadrants. The slats and also the quadrants overlap to avoid dead zones on the detector. The tracking system covers a total area of about 100 m^2.

The present electronics contains the front-end electronics and the read-out system, CROCUS (Cluster Read Out Concentrator Unit System), which concentrates the data signals from the

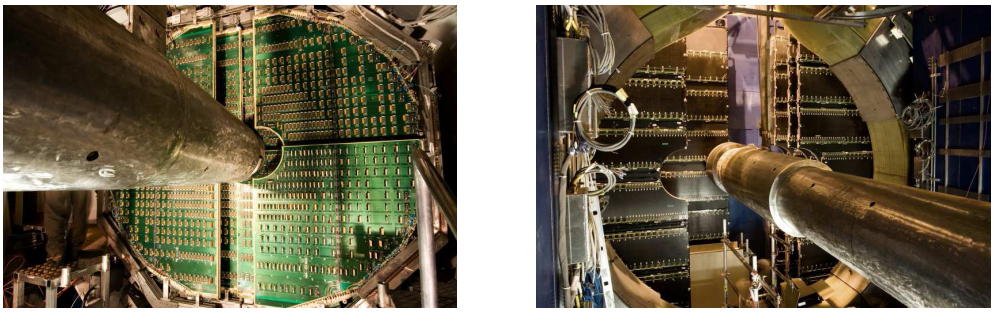


Figure 6.1: Layout of station 2 of the muon chambers; the read-out electronics is distributed on the surface of a quadrant (left). Layout of stations 4 and 5 of the muon chamber system; the read-out electronics is distributed on the top and bottom edge of the slats (right).

front-end electronics (FEE) and sends them to the Data Acquisition System (DAQ) on optical fibers and to the interface with the ALICE Central Trigger Processor. Data, control and trigger signals are transmitted on buses buried in the detector PCBs and on ribbon cables between the detector and the CROCUS. Translator boards located on the external edges of the detectors make the link between buses and ribbon cables to adapt the signal levels and allow an easy connection/disconnection of the detectors.

6.3 Muon Tracking Chamber system upgrade

In order to achieve a design read-out rate of 100 kHz, an architecture has been adopted where the signals are continuously sampled. The dead time free data read-out supports continuous, self-triggered read-out mode and triggered mode. The data flow will be reduced by the combined online and offline computing system.

The muon chamber electronics upgrade architecture employs ALICE common electronics developments, the front-end ASIC, SAMPA used by MCH and TPC (see Chapter 5) and the common read-out unit (CRU, see section 2.5). Programmable parameters in the SAMPA allow taking specification differences between the two systems into account. The CRU will replace the CROCUS boards to concentrate the data before transmitting them to the online and offline system. The data transmission between FEE and CRU is based on optical GBT links [14].

6.3.1 Front-end electronics (FEE)

The FEE parameters are defined by the following specifications:

- The detector implementation will not be modified. Therefore, the location, physical layout and connections to the chambers of the 64 channel FEE boards will be unchanged.
- The chambers will be operated with the present gas and high voltage parameters (gain:$\simeq 2{\cdot}10^4$).
- The spatial resolution is better than 100 μm, which corresponds to a required charge resolution at the percent level.
- The maximum input signal will be 500 fC and the gain $\simeq$ 4 mV/fC, considering an 2 V effective ADC range.
- The cooling system remains unchanged allowing no significant increase in power consumption ($\simeq$ 13 mW/ch).

For the expected signal distribution, the dependence of the charge and spatial resolution on shaping time, sampling frequency, ADC resolution and noise has been studied. Shaping times of 160 ns, as for the TPC application and 300 ns, have been considered. Three sampling frequencies, 10, 25 and 40 MHz and three different ADC resolutions with 10, 11 and 12 bit, respectively, have been evaluated [32]. In order to avoid resolution degradation due to the suppression of ADC samples before/after the read-out cycle, the SAMPA ASICs allow transmission of a programmable number of pre- and post-trigger samples.

The SAMPA parameters for the MCH have been found to be as follows:

- 10-bit ADC resolution.

- 10 MHz sampling rate.
- shaping time of 330 ns.
- noise below 2000 electrons (large pads), 1000 electrons (small pads).

6.3.2 Read-out electronics

The muon chambers will use 17000 FEE boards containing two 32-channel SAMPA ASICs. The FEE cards are connected to 500 GBT read-out boards multiplexing the SAMPA serial output links of 40 front-end cards into one multi gigabit serial GBT link and forwarding the data to the CRU. This configuration is illustrated in Fig. 6.2.

Physically, two different types of FEE cards are used for the quadrants and the slats. The MCH hit rate is sufficiently low, that the data traffic of one SAMPA ASIC is routed through only one serial output link operating at 80 Mb/s. One of the two SAMPA read-out ASICs on the FEE card sends its data read-out stream to the other SAMPA on the FEE card which merges the data stream of its neighbour to its own data stream. That way each FEE card has only one single serial output link.

Each FEE card serial link is connected to one out of 40 GBTx e-link inputs [33] on the GBT read-out cards. The GBTx e-link outputs send trigger information to the SAMPA ASICs. The maximum distance between the FEE cards and the GBT read-out cards is 2.5 m which is a comfortable distance for the 80 Mb/s e-links. Depending on the chamber type the connection between the FEE cards and the GBT read-out cards is made either directly on a PCB (quadrant electronics PCB) holding the structure or on cables (FE2GBT cables). The data transmission from the GBT read-out cards to the CRU in the counting room is done via bi-directional GBT links.

The GBT link chip set is a common LHC development and contains the GBTx ASIC, SCA ASIC and the optical transceiver module VTRx [34]. The GBTx transmits detector data and receives timing and trigger data via the VTRx optical transceiver. The slow control adapter ASIC (SCA) is directly connected to the GBTx and allows communication via I2C to the SAMPA ASICs and allows the measurement of supply voltages.

As the trigger latency for the MCH is not critical the CTP sends trigger and timing information via the trigger and timing distribution system (TTS) to the CRUs in the counting room. The CRU forward the data to the FEE cards via the bi-directional GBT links. The CRUs are connected to the online computing system (O^2) via the DDL3 interfaces, send the detector data to the O^2 and receive DCS information from the O^2. The DCS data stream is merged with the trigger information into the GBT link to the detector.

The muon chamber electronics will support read-out upon a trigger signal at interaction rate and triggerless, continuous read-out designed for a maximum interaction rate of 100 kHz, presenting a safety factor of 2 compared to the nominal interaction rate of 50 kHz.

6.3.3 Data rate and format

In addition to the raw data output of the acquired ADC samples, optionally the SAMPA allows compression where the signal charge and a time stamp is read out only. A simple sum of sampling

SAMPA read-out mode	SAMPA data word type	avg. packet length [bit]	SAMPA data rate [Mb/s]	MCH data rate [Tb/s]
triggered	raw ADC samples	170	49	1.62
triggered	charge sum	90	26	0.86
continuous	raw ADC samples	156	49	1.62
continuous	charge sum	83	26	0.86

Table 6.1: MCH data packet length and data rates. The continuous read-out data rates do not contain any beam noise contribution possibly increasing the effective channel occupancy.

values including a programmable number of pre- and post-samples is foreseen. Nominally one pre-sample and one post-sample is considered.

For data bandwidth considerations, an occupancy of 9 % and an interaction rate of 100 kHz is assumed. The data word length considerations assume a shaping time of 330 ns and a maximum pulse width over threshold of 1000 ns corresponding to 10 samples over threshold at 10 MHz sampling rate. Successive ADC samples above threshold are called a cluster.

Section 5.3 gives detailed information about the SAMPA data format. In triggered read-out mode the SAMPA sends out a 50-bit header word for each channel when data above threshold has been registered. If no channel is hit only one header for all 32 channels is transmitted. In raw ADC sample read-out mode each ADC sample above threshold is read out. The average data packet length per trigger and SAMPA ASIC can be calculated as follows: 50-bit header + 10 samples * 10-bit ADC value + 10-bit cluster time stamp + 10-bit cluster length = 170 bit. Applying the channel occupancy of 9 % and a trigger rate of 100 kHz yields an average data rate for 32 channels of 49 Mb/s. This calculation does not consider the negligible contribution of headers sent in case no hit has been registered in a SAMPA chip for a given trigger.

When activating the read-out of the charge sum instead of reading out the raw ADC samples in triggered mode the calculation of the average data rate is as follows: 50-bit header + 20-bit charge sum + 10-bit cluster time stamp + 10-bit cluster length give a word length of 90 bit. Applying the channel occupancy of 9 % and a trigger rate of 100 kHz an average data rate for 32 channels of 26 Mb/s can be calculated.

In continuous and raw ADC sample read-out mode all clusters are packed into a 1024-time bin long data frame of 102.4 μs length. In that time duration, on average each channel fires: 100 kHz interaction rate * 102.4 μs * 9 % occupancy = 0.92 times. The average length of the data packet read out in each time frame of 102.4 μs is: 50-bit header word + (10 samples * 10-bit ADC value + 10-bit cluster time stamp + 10-bit cluster length) * 0.92 = 156 bit. This results in a data rate for 32 channels of 49 Mb/s.

When activating the read-out of the charge sum instead of reading out the raw ADC samples in continuous read-out mode the average packet length read out each time frame of 102.4 μs is: 50-bit header + (20-bit charge sum + 10-bit cluster time stamp + 10-bit cluster length) * 0.92 = 83 bit. This results in a data rate for 32 channels of 27 Mb/s.

Table 6.1 summarises the date rates per SAMPA ASIC and for the full MCH system. The continuous read-out data rates do not contain any beam noise contribution possibly increasing the effective channel occupancy.

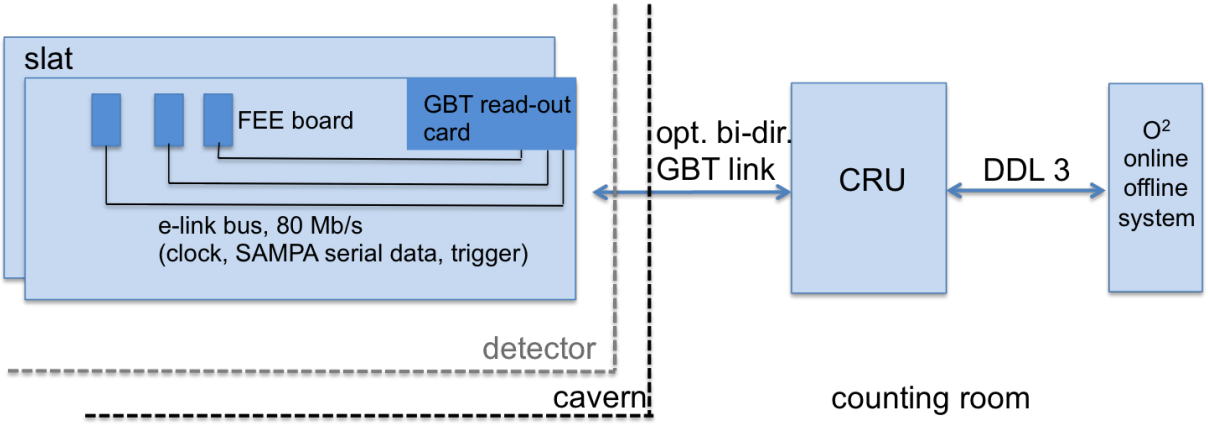


Figure 6.2: MCH read-out configuration.

6.4 Schedule, funding and institutes

The cost estimate of the muon chamber electronics upgrade, including spares, is given in Tab. 6.2. The involved institutes are shown in Tab. 6.3. The FEE boards and GBT read-out boards will

Item	#	Price [CHF]	Total cost [kCHF]
SAMPA	38000	29.5	1121
FEE board (PCB+passive comp.)	19000	39	745
FE2GBT cable	11040	15	163
Quadrant electronics PCB	36	3389	122
GBT read-out card (PCB+passive comp.)	575	200	115
VTRx	575	200	115
GBTx	575	60	35
SCA	575	20	12
optical FE-link (passive)	575	300	173
CRU (# of inputs)	575	361	234
Total with SAMPA			2835
Total without SAMPA			1714

Table 6.2: Cost estimate for the MCH electronics upgrade, including 10 % of spare (CORE cost only)

be taken in charge, both technically and financially, by the following laboratories from the MCH collaboration: Orsay (IN2P3) will design and produce the FEE boards. Cagliari (INFN) and IRFU (CEA Saclay) will design and build the GBT read-out boards and the links between the FEE cards and GBT read-out boards (Quadrant electronics PCB, FE2GBT cables).

Common parts (CRU & SAMPA) will be shared between the present MCH collaboration and the institutes responsible for the design (CRU: Wigner Institute/Hungary, VECC/India; SAMPA: University of Sao Paulo/Brazil, Univ. Bergen). For the SAMPA, University of Sao Paulo plans to act as the main financial contributor. IRFU is involved in the SAMPA front-end design.

Table 6.4 shows the schedule for upgrade development items.

Institutes
INFN and Università degli Studi di Cagliari, Italy
IPNO, Institut de Physique Nucléaire d'Orsay, Université de Paris-Sud, IN2P3/CNRS, France
SPhN, Service de Physique Nucléaire , CEA-IRFU Saclay, France
UNICAMP, Universidade Estadual de Campinas, Brazil
IFUSP, Instituto de Física, Universidade de São Paulo, Brazil
EPUSP, Escola Politécnica, Universidade de São Paulo, Brazil
Wigner Research Centre for Physics, Institute for Particle Nuclear Physics, Hungary
VECC, Variable Energy Cyclotron Center, Department of Atomic Energy, Kolkata, India
SAHA Institute of Nuclear Physics, Kolkata, India
Aligarh Muslim University, Aligarh, India
Bhabha Atomic Research Centre, Mumbai, India
Bose Institute, Kolkata, India

Table 6.3: MCH institutes.

Year	Activity
	FEE card, Quadrant PCB, FE2GBT cables, GBT read-out cards
2014	Design
2015	Prototype
2015	Test prototype
2016	Production
2018	Installation

Table 6.4: MCH upgrade schedule.

7 Muon Identifier - MID

7.1 Overview

The Muon Identifier (MID) is the proposed future designation, after LS2, of the present Muon Trigger system [2]. This choice will be justified in this chapter. The Muon Trigger detector is composed of 4 planes of single-gap Resistive Plate Chamber (RPC) detectors, organised in two stations of two planes located at 16 m and 17 m from the interaction point. The planes in the same station are 17 cm apart. The total detection area is about 150 m^2. The RPC signals are collected by means of a total of 21000 strips and the same number of Front-End (FE) electronics channels. The signals from the FE electronics are propagated to the 234 local cards, acting as read-out interface and in charge of the first stage of the trigger decision. Read-out is performed by two DARC (Dimuon-trigger ALICE Read-out Controller) [35] cards interfaced to the local cards by means of 16 regional cards.

The FE electronics is located on the RPC detectors and its upgrade has been already discussed in the Letter of Intent (LoI) for the ALICE upgrade [1]. The main motivation is to prevent ageing of the RPCs. The present FE chip, called ADULT [36], will be replaced by a new ASIC, FEERIC. Unlike ADULT, FEERIC will perform amplification of the analog signals from the RPCs. The RPCs will be operated in "genuine" avalanche mode (like in ATLAS [37] and CMS [38]) with a significant reduction of the charge produced in the gas, hence limiting ageing effects.

In the LoI, it was proposed to preserve the muon trigger decision functionalities and to read out the detector upon a muon trigger signal with a rate that is typically one order of magnitude smaller than the Pb-Pb minimum bias interaction rate. Specifically, it was proposed to keep the local cards and to replace only the DARC and regional cards.

Subsequent to the LoI, it has been decided to change this strategy and to read out all muon detectors for each minimum bias trigger with the goal of maximising the muon physics potential. This implies some changes in the upgrade strategy because:

- the read-out rate will be more than one order of magnitude larger compared to the initial design.
- there is no need for fast, hardware-based, p_T-dependent muon trigger signals.

As a consequence, the local, regional and DARC cards must be replaced in order to cope with the given read-out rates. The detector, separated from the muon chambers by an iron wall of 1.2 m thickness, will, however, keep its crucial role as muon identifier, which motivates the change of name to MID. Indeed, the hadron contamination in the muon chambers, for matched tracks with the ones in the MID, is dramatically cleaned [39, 40] and all present data analyses request this matching condition. Finally, the MID helps to reduce pile-up effects in the muon chambers when track matching is requested, thanks to its excellent timing properties, allowing the separation of two tracks belonging to two adjacent 40 MHz bunch crossing cycles.

In conclusion, the upgrades of the MID system consist of:

interaction rate	100 kHz Pb-Pb $\sqrt{s}_{NN} = 5.5$ TeV	200 kHz pp $\sqrt{s} = 14$ TeV
counting rate	75 (mean) - 125 (peak) hits/s/cm^2	6 (mean) - 15 (peak) hits/s/cm^2

Table 7.1: Expected counting rates of the RPCs.

- Replacement of the FE electronics.
- Replacement of all the read-out electronics, including local, regional and DARC cards.

There is no indication for a need of a major upgrade of the RPC detector design and consolidation of the system is foreseen.

7.2 Front-End electronics upgrade

The expected counting rates of the RPC detectors are given in Tab. 7.1 for pp and Pb-Pb. These values are extrapolated from the present measurements [41]. The counting rate in pp does not account for the beam-induced background, which can be quite large.

It can be seen from Tab. 7.1 that the counting rate of the RPC could exceed 100 hits/s/cm^2 in Pb-Pb collisions. As discussed in [1], in the current operating mode of the RPCs, without amplification in the FE, the mean total charge is of the order of 100 pC per hit. In these conditions, the R&D results [42] on efficiency set an instantaneous counting rate limit below 50 hits/s/cm^2, including some safety margins in case of short running periods. Another limitation comes from RPC aging : from our R&D [42], safe operation of the detectors cannot be guaranteed for a cumulated dose larger than 50 mC/cm^2 (500 Mhits/cm^2 in the present mode of operation).

The total particle fluence numbers for the upgrade physics program and safety factors discussed in Chap. 3 would result in a charge deposit of more than 100 mC/cm^2 for the most exposed RPCs. Keeping in mind that the RPCs will have accumulated already a significant dose before LS2, these arguments strongly favour operating the RPCs in “genuine avalanche” mode, with a reduced charge per hit. Based on e.g. ATLAS results [43], a reduction by a factor $3-5$ for the charge per hit can be achieved, which requires the mentioned change of the FE electronics.

An R&D program has been launched in order to evaluate the actual performance of the MID RPCs equipped with the new FE electronics and is described as follows:

- measurement of the channel noise for the RPC installed in the cavern, which gave values in the range of $25-50$ fC depending on strip size and position.
- realisation of a FE card prototype called BARI-FE (Fig. 7.1) with the CMS RPCs ASIC[44].
- measurements of the RPC performance (efficiency curves, time resolution, cluster size) with BARI-FE prototypes on the Torino RPC production test bench [45].
- design of the FEERIC ASIC.

The efficiency curves for RPCs equipped with BARI-FE cards (for threshold values of 200 mV and 250 mV) and ADULT cards (with 7 mV threshold without signal amplification) are compared in Fig. 7.2.

As expected, it can be seen that the voltage at the efficiency knee is shifted towards lower values by several hundreds of volts with BARI-FE cards. As a direct consequence, the charge at

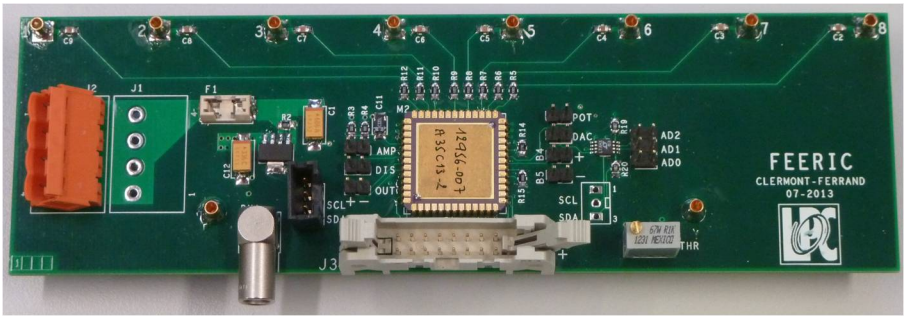


Figure 7.1: FE card with the first prototype of the FEERIC ASIC

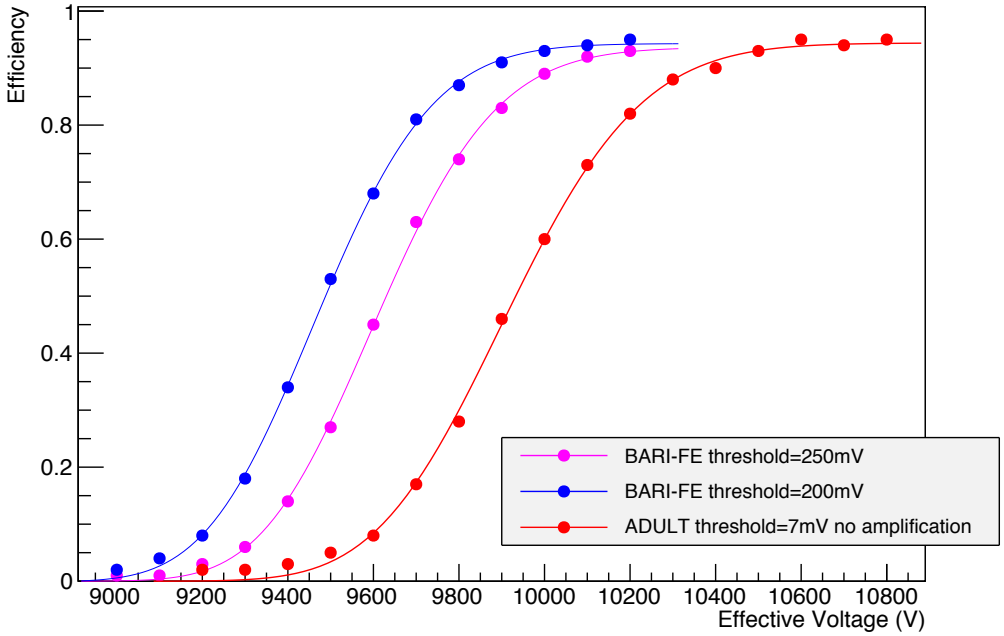


Figure 7.2: Comparison of efficiency curves for RPCs equipped with BARI-FE and ADULT FE cards

operating voltage is lower. From test bench measurements, it is difficult to evaluate the charge per hit achievable in cavern at operating voltage, which depends in turn on the threshold value, hence on the noise level. For this reason, we foresee equipping before the end of the LS1 one of the ALICE RPCs in cavern with a FEERIC FE card pre-production (typically 50 cards of 8 channels each). This allows accurate quantification, on a long time scale, the achievable RPC performance in realistic conditions. The FE production follows, with final installation scheduled during the LS2. The possibility of using the I2C bus for threshold remote control is considered.

As there is no available ASIC fulfilling all MID requirements, the design of the FEERIC ASIC has been carried out. The CMS RPC ASIC is the closest to the needs but it is designed for negative signals only, while the MID is read out on both sides of the RPC plane and thus requires positive and negative signal processing. The block diagram of the FEERIC ASIC is shown in Fig. 7.3. It includes a two stage transimpedance amplifier with $\approx 0.1\ \Omega$ input impedance, a zero-crossing discriminator, a one-shot circuit preventing from re-triggering during 100 ns and LVDS drivers.

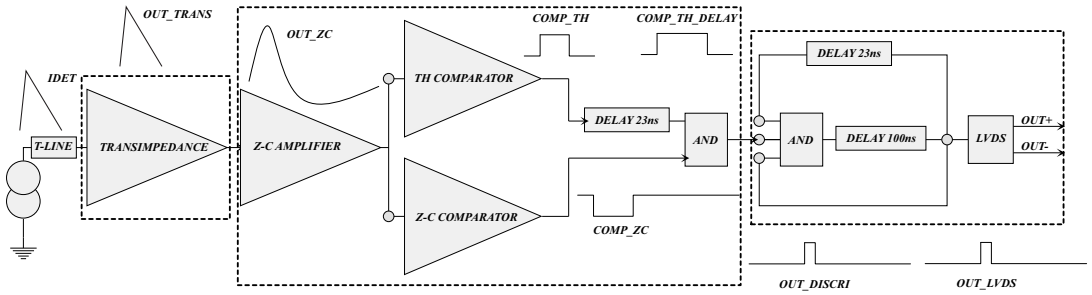


Figure 7.3: Block diagram of the FEERIC FE ASIC.

	FEERIC ASIC Specifications and simulated performance	FEERIC FE card prototype performance
ASIC technology	0.35 μm CMOS	
Number of ch.	8	
Dynamic range	Q=20 fC - 3 pC	
Noise level	$<$ 2 fC (r.m.s.)	25 fC (thr. above noise)
Power cons.	70 mW/ch	60 mW/ch
	Req. $<$ 100 mW/ch	
Power supply	3 V	
Input polarity	+/-	
Amplification	0.4 mV/fC	0.33 mV/fC
One shot	yes (100 ns)	
Discriminator	zero crossing	
Time jitter r.m.s.	$<$ 200 ps	$<$ 500 ps
for Q $>$ 100 fC	Req. $<$ 1 ns	
Time walk	600 ps	900 ps
for 100 $<$ Q $<$ 3000 fC	Req. $<$ 2 ns	
Output signal format	LVDS, 23 ns	23 ns

Table 7.2: Main specifications and simulated performance (central column) of the FEERIC ASIC. Measured performance (right column, preliminary) of the first prototype of the FEERIC FE card. The noise level obtained in simulations is an intrinsic r.m.s. value of the ASIC noise while the measured value corresponds to the threshold above noise in environmental conditions.

The main specifications, requirements and simulated performance of the FEERIC ASIC are summarised in Tab. 7.2. The operating range is expected to be above a threshold of typically 100 fC.

The first prototype of the FEERIC ASIC has been delivered at LPC Clermont-Ferrand in September 2013. Qualification tests are ongoing: preliminary measurements (Tab. 7.2) show that this first version of the ASIC is fully operational. A second submission will be launched by early 2014 to optimise the ASIC performance while fine-tuning its layout. The FEERIC FE card pre-production will be built using the ASIC from this submission.

7.3 Read-out electronics upgrade

The present MID is divided into 16 vertical regions. Each of the 16 regional areas is read out by 1 out of 16 VME crates. Each crate contains one regional card multiplexing the data from up

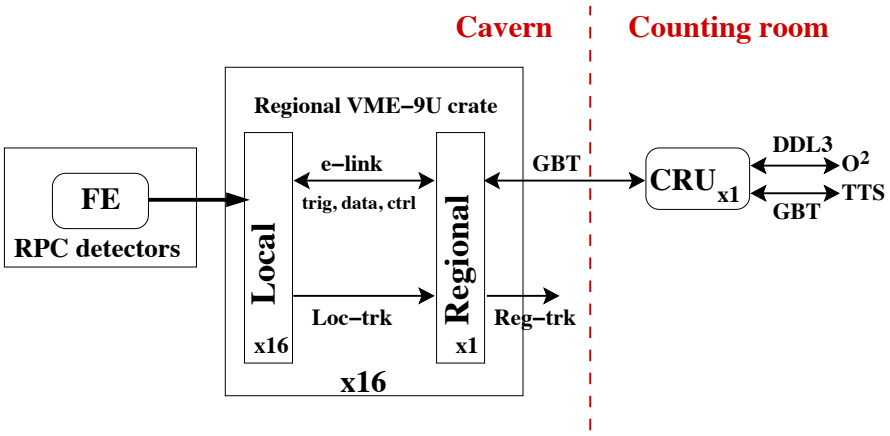


Figure 7.4: Read-out electronics architecture.

to 16 local cards. Each local card is connected to 128 FE channels via eight cables containing 34 wires from four detector planes and the two orthogonal coordinates. In total, 234 local cards are used. The system is located on the upper gangways at the C-side where the radiation level is low. For the upgrade, this segmentation will be maintained.

Figure 7.4 shows the upgraded MID system architecture. In order to increase the read-out rate to 100 kHz, both the local and regional read-out cards will be re-designed. The hardware implementation of the regional and local card will be identical, reducing the design and production effort by re-using the same hardware and adapting the FPGA firmware.

The local card receives the binary chamber signals via LVDS signals indicating whether the corresponding channel has been hit for each bunch crossing. The FPGA in the local card performs the following functions:

- applies a remotely configurable noisy channel mask.
- compensates the different transmission delays (max.: 35 ns, per steps of 2.5 ns) from cables of different lengths coming from the FE.
- calculates a Loc-trk signal for each bunch crossing corresponding to a track crossing in any of the two detector stations.
- provides 16-bit counters for monitoring the detector counting rate.
- zero-suppresses the input data.
- provides a multi-event buffer.
- and provides a trigger, clock, control and data interface to the regional card using one 320 Mbit/s serial bi-directional connection.

The same card, used as regional card, receives the local information via 16 serial links, assembles the raw events in their final format and adds the trigger information. The cards offer two bi-directional 3.2 Gbit/s GBT links to send the data to the CRU in the counting room, which forwards the MID data on one DDL3 link to the O^2 system. For the data rate in the MID, one GBT link per regional card is sufficient. However, it is foreseen to implement a second link on the regional card for redundancy and possible further upgrade. The regional card provides a Reg-trk signal for each bunch crossing $\approx$ 300 ns after the interaction by ORing the local Loc-trk

Component	Number
FE cards/channels	2384/20992
Local cards	234
Regional cards	16
CRU AMC cards	1
electrical serial links (e-link)	234
GBT (bi-directional)	16
DDL3	1

Table 7.3: Total number of MID cards and links.

signals. Figure 7.5 shows a block diagram of the local/regional hardware implementation. The number of cards and links is in Tab. 7.3.

As the MID is not latency critical, the trigger and timing interface (TTS) connects the MID via the LTUs and the CRU in the counting room. From there, the CRU forwards the trigger and timing information via the GBT front-end links to the regional and local cards.

The adopted architecture has the advantage of limiting the number of high speed GBT links thanks to the regional interface between the local cards and the CRU. The cost of the project is consequently reduced.

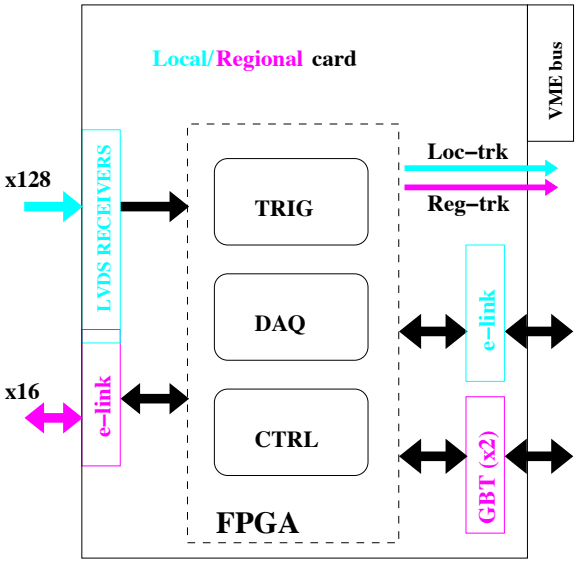


Figure 7.5: New local/regional card scheme: the specific local (regional) components are represented in cyan (magenta) while the common ones are in black.

Events are stored in the local card multi-event buffer at each trigger. The range of the acceptable trigger latency is 0.5 - 9.6 μs. The multi-event buffer in the local card is larger than the size of one software event (registered at very low rate), which includes, in addition to the standard physics event information, the counters. The maximum size of a software event, obtained in case of calibration with a generator, is 50 words of 32 bit. It corresponds to a depth of 10 physics events (maximum 5 words of 32 bit).

The implementation of 2 GBTs per local/regional card leaves the option of a complete FE data transfer (5.12 Gbit/s), at 40 MHz without zero suppression, from the local cards directly to the CRUs (one CRU per regional area in this case). This solution corresponds to a continuous read-out, however, with an increased cost due to the higher number of optical GBT links to the

200 kHz pp $\sqrt{s} = 14$ TeV	100 kHz Pb-Pb $\sqrt{s_{NN}} = 5.5$ TeV	
Total data flow to O^2	Total data flow to O^2	Max data flow per link from local to regional card
540 MB/s	300 MB/s	1 MB/s

Table 7.4: Expected data flow.

CRUs.

The expected data flow in pp and Pb-Pb is given in Tab. 7.4. It includes a preliminary evaluation of event separators and headers which contribute significantly to the event size. The total data flow in Pb-Pb at 100 kHz amounts to 300 MB/s. The read-out dead time is expected to be negligible with a single DDL3 link at 10 Gbit/s. In any case, a busy mechanism will be implemented.

7.4 Schedule, funding and institutes

The involved institutes are summarised in Tab. 7.5.

Institutes
Sezione INFN and Dipartimento dell'Università di Torino, Italy
Konkuk University, Seoul, Republic of Korea
Subatech, Ecole des Mines et Université de Nantes, France IN2P3/CNRS
Laboratoire de Physique Corpusculaire, Université Blaise Pascal de Clermont-Ferrand, France IN2P3/CNRS

Table 7.5: MID institutes.

Table 7.6 shows funding and schedule with a start of local/regional card prototyping during LS1, CRU interfacing and local/regional card production in 2015 – 2016 and installation and commissioning during LS2.

Year	Activity	Cost [kCHF]	
2014	Test-RPC installation	67	
2015	Test Front-end electronics in realistic conditions & Front-end electronics production (start)	188	
2016	Front-end electronics production (cont.)	109	
2017	Front-end electronics production (end)	77	
	Total RPC & Front-end electronics		441
2014	Local/Regional card prototypes	36	
2015	Local/Regional card production (start)	71	
2016	Local/Regional card production (cont.)	160	
2017	Local/Regional card production (end)	38	
	Total Local/Regional card		305
	Total MID		746

Table 7.6: MID schedule and funding in kCHF (CORE cost only)

8 Transition Radiation Detector - TRD

8.1 TRD upgrade strategy

The Transition Radiation Detector (TRD) has originally been designed for a Pb-Pb interaction rate of 8 kHz and for a significant event rejection from the level 1 (L1) trigger [46]. The existing processing and read-out of the front-end electronics (FEE) as well as the read-out and trigger functionality are optimised for these conditions and provide a fast L1 trigger contribution, implementing jet and electron triggers.

For the ALICE upgrade, the TRD detector must operate at much higher interaction rates, and the FEE and read-out system must accept the largest possible fraction of interactions without the need to provide a trigger.

Based on measurements in Pb-Pb collisions in Run1, it has been estimated that the chamber currents reach 6 μA at 50 kHz interaction rate. This leads to a total accumulated charge of 0.8 mC per cm of wire per year, assuming an average interaction rate of 50 kHz. As the chambers were validated for charges above 10 mC/cm, it is expected that no ageing effect will occur for the planned running time. The voltage drop at these currents, however, may result in significant gain variations in case of large variations of interaction rate, e.g. over the duration of a fill. No problems on detector stability or concerning space charge effects are expected.

An upgrade of the FEE hardware is not realistically feasible. Besides the design and production effort, it would require a complete disassembly and reconstruction of the 18 TRD supermodules and the FEE mounted on the 522 individual detector chambers. The chosen strategy is a reduction of event read-out time with the existing FEE by changing its mode of operation and limiting the amount of event data read from the FEE as detailed in Sec. 8.2. The impact on performance for tracking and electron identification has been extensively studied (see Sec. 8.3) to validate the proposed strategy.

The read-out of the optimised FEE data format at the full minimum bias event rate requires new hardware with increased bandwidth to the O^2 system as described in Sec. 8.4. The use of the proposed ALICE Common Read-Out Unit (CRU) is envisaged for this purpose.

8.2 Frontend operation and read-out

8.2.1 Current FEE read-out

The TRD FEE [47] is bound to operate in a triggered mode of single event read-out. An initial trigger level (LM, the functionality corresponds to the pretrigger in Run1) fixes the time reference for sampling and processing. A subsequent event can only be triggered after completion of the FEE event read-out or after the abort of the read-out sequence due a negative higher level trigger.

The front-end electronics comprises a hardware preprocessor for the calculation of quantities relevant for the finding of online tracklets, which are track segments in a single detector chamber. The preprocessor provides its results at a fixed time after the sampling has been started by an LM trigger. Further processing is done in CPUs in the FEE.

Figure 8.1 shows the timing sequence for a typical event. To recover the information before the arrival of the LM trigger, the digitised data are delayed in pipeline stages. With a drift time of 2.2 μs and a delay of 900 ns, the processing in the CPUs can start 3.1 μs after the interaction when all data have passed through the preprocessor and its results are available. The processing time depends on the complexity of the calculations. Finding tracklets using the preprocessor results takes about 1 μs.

The FEE read-out is organised in 60 trees (2 per chamber) per supermodule, each with 64 FEE devices (multi chip module - MCM) and equipped with one optical read-out interface (ORI). The read-out can operate in two modes: tracklet mode and raw read-out mode. The tracklet mode is implemented as pure push mechanism up the read-out tree without any handshaking. This avoids latency but is limited to the read-out of four 32-bit words for each MCM. The raw read-out mode has no practical limitation on the number of transmitted words but requires handshaking, which results in a total overhead of 8.32 μs in each read-out tree, in addition to the time for the actual data transfer with 8 bit at 120 MHz.

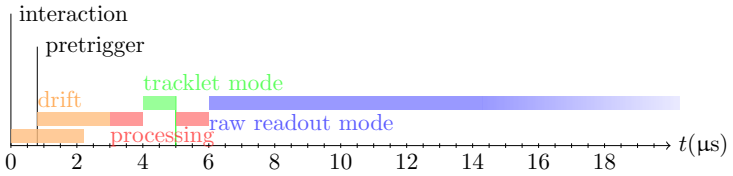


Figure 8.1: FEE event processing and read-out sequence as used in Run1. The event read-out timing is shown for an event with 25% of tracklet words.

The event read-out time, i.e. the time from an interaction until the FEE has finished shipping all data, depends on the FEE processing effort and the maximal data volume in a single read-out tree. With the raw read-out mode, the event read-out time will be of about 16 μs in addition to the transfer time for the actual data volume of a given event. The currently used read-out of full zero-suppressed ADC data results in event read-out time of several 10 μs and puts a severe limit on the maximum read-out rate.

8.2.2 Read-out with modified data formats

New data formats can be implemented within the capabilities of the existing FEE hardware, with the goal to minimise dead time by a reduction of data volume. Two different approaches have been investigated:

- Tracklet Read-out

  A significant read-out time reduction can only be achieved by avoiding the handshaking overhead in the raw read-out mode and by transferring information exclusively via the four data words associated to each MCM.

  In this mode, the event read-out time is in the range of 4 μs up to an upper limit of around 8 μs, imposed by the maximum number of words available in this read-out mode.

The most stringent constraint is the limitation to four 32-bit words (128 bits) per MCM which limits the acceptable local occupancy. Currently, in the tracklet mode one MCM can send up to four tracklet words, each with the following information: z-position (longitudinal) in units of padrow (4 bits), y-position (transverse) in units of 160 μm (13 bits), y-deflection (transverse) in units of 140 μm (7 bits) and PID information (8 bits).

In order to extend the charge information used for PID, the read-out of 3 tracklets with 18 bits for PID information, or 2 tracklets with 40 bits for PID is foreseen. The bin widths for the position information would remain unchanged. Two charge slices are available directly from the preprocessor without additional delay. More slices could be calculated in the CPUs by looping over the data in the event buffers.

- Partial Data Read-out

  Another option to reduce the amount of data is a partial raw data read-out in the raw read-out mode. The read-out can be restricted without information loss to regions where TRD information is relevant, i.e. only ADC data belonging to tracklets which fulfill a simple criterion for electron candidates. The selection of regions for read-out has to be implemented within an MCM, based on a simple criterion optimised for data reduction and not necessarily for purity. A data volume reduction by a factor 5 can be achieved; more studies are needed especially to evaluate the effect on track propagation from the inner detectors.

Running with alternative data formats requires only a change of FEE configuration. Therefore, new formats can be tested and optimised with real data throughout Run2 without major disturbance for normal data taking. Depending on the rate requirements, either tracklet read-out or partial data read-out could be used in different running periods after the upgrade.

Front-end read-out rates with new data formats

The read-out rate performance of the new data formats is shown in Tab. 8.1 for the case of Pb-Pb collisions which constitute the biggest challenge for the read-out given the large event sizes at comparably high interaction rates of 50 kHz or above.

Cases for the tracklet read-out are shown for the maximum event read-out time of 8 μs and another more typical value of 6 μs. Accepted event rates in the range of 60 kHz can be achieved for 100 kHz interaction rate, which is significantly higher than the accepted rates for any data format using the raw read-out mode of the FEE.

In all read-out scenarios with reduced or tracklet data, the data volume is below 14 Gb/s/sector.

For the given read-out rates and data volumes, a Pb-Pb minimum bias raw event size of 210 kB/sector (28.3 kb/event/link) is assumed, derived from the experimental value of 170 kB/sector (2011 Pb-Pb data at $\sqrt{s_{NN}} = 2.76\ TeV$) and scaled to $\sqrt{s_{NN}} = 5.5\ TeV$. For the tracklet event size, occupancies of 25 % (6 μs case) and 50 % of the maximum number of tracklet words (8 μs case) are assumed. For the partial raw data read-out, a factor 5 of data reduction with respect to the full zero-suppressed ADC data is assumed. The numbers of accepted events are estimated based on FEE read-out time and interaction rate only.

Possible rate limits coming from the increased power consumption at the upgrade read-out rates were investigated in test runs where tracklets were produced artificially by adjusting the FEE baseline and cluster thresholds. Only the digital 1.8 V low voltage channels, which are used

	interaction rate [kHz]	Accepted rate [kHz]	Accepted fraction [%]	deadtime [%]	data volume [Gb/s/sector]
tracklet read-out only					
avg. deadtime 6 μs	50	38.5	76.9	23.1	4.73
	100	62.5	62.5	37.5	7.68
	200	90.9	45.5	54.5	11.17
avg. deadtime 8 μs	50	35.7	71.4	28.6	8.78
	100	55.6	55.6	44.4	13.65
partial raw data read-out	50	23.3	46.5	53.5	7.8
full zero-suppressed ADC data	50	16.6	33.2	66.7	27.9

Table 8.1: TRD read-out rates and data volume for different TRD data formats and event scenarios.

for components in the FEE chip that are clocked exclusively during event processing, show a significant dependence on read-out rate. Measured currents are below 150 A for all running scenarios up to 100 kHz read-out rate, well below the 200 A current limit of the LV supplies.

The TRD currently calibrates gain, drift velocity v_d, $E \times B$ effects and time-offset; about 30000 pp or 1500 Pb-Pb minimum bias events are needed to achieve a calibration point. The existing calibration procedures can be preserved with the new data formats by reading the full zero-suppressed ADC data instead of the tracklet words for a small subset of events, with negligible effects on deadtime and data volume. It is also conceivable that calibration could exclusively use tracklet words, doing gain calibration with the charge information available in the tracklet words and integrating other calibration parameters in a global alignment procedure.

As a conclusion, the tracklet read-out scenario would allow - with the existing FEE hardware - the reading out of more than 70 % of events at the envisaged Pb-Pb minimum-bias 50 kHz interaction rate, including also the TRD detector. A study on the impact on tracking and particle identification performance of the new format Pb-Pb is presented in the next section.

8.3 TRD Performance with new data formats

The performance for tracking and PID of the reduced information content of the tracklet read-out scenario described above is assessed by comparing it to the performance of the offline reconstruction based on full zero-suppressed ADC data (ZS) (for details see [48]) and TPC seeding. Results from pp data at 8 TeV (production LHC12f) are presented for two tracklet reconstruction scenarios:

- read-out tracklets obtained online as currently used for trigger purposes
- tracklets calculated offline from ZS data with an improved PID content.

Their matching was done with respect to corresponding global tracks by their azimuthal and polar positions at the radial distance of the anode wire of the corresponding TRD chamber. The offline residual misalignment is applied in both cases.

The tracklet reconstruction efficiency for online relative to offline scenarios is presented in Fig. 8.2 (left) for a single pp run. Due to systematic effects induced by drift being perpendicular to

magnetic field deflection (E x B effects), positive and negative charged particles are influenced differently. They are therefore shown separately in order to assess the $p_T \sim 1.5\ GeV/c$ threshold above which reconstruction is not affected by particle charge. From Fig. 8.2 (left), we conclude that the TRD contribution to global tracks should remain unchanged within 4 % when using the tracklet read-out format.

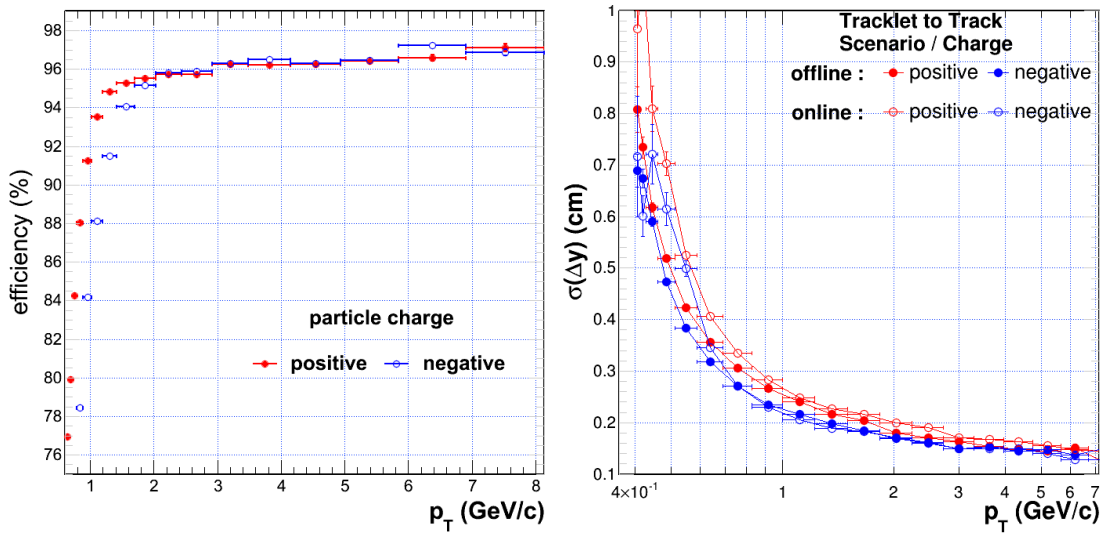


Figure 8.2: TRD reconstruction performance relevant for tracking. The reconstruction efficiency of online relative to offline (left) and the quality of azimuthal residuals (Δy) resolutions (right) for positive [red] and negative [blue] charged particles for the two tracklet reconstruction scenarios (right).

The quality of TRD reconstruction for track position in the azimuthal plane with respect to global tracks is presented in Fig. 8.2. The residuals (Δy), obtained chamber-wise, are characterised by Gaussian shapes with comparable sigmas, i.e. resolutions (Fig. 8.2 right) for both tracklet reconstruction scenarios. The TRD tracking performance remains unchanged for positive particles above $p_T \sim 1.5\ GeV/c$ and for negative particles above $p_T \sim 0.8\ GeV/c$.

The online tracklet performance at low p_T develops asymmetrically with particle charge due to the missing correction for the ion tails (Tail Cancellation - TC).

Characteristics relevant for particle identification of the estimation of the track angle, in a single TRD chamber, by the two tracklet scenario are presented in Fig. 8.3 (right). The Gaussian shaped residuals ($\Delta\phi$) are described by shifts with larger values obtained for the online tracklets and are mainly due to missing TC corrections and to limited calibration precision for the drift velocity and $E \times B$ effects.

In the left panel of Fig. 8.3, the particle identification (PID) performance is compared for online reconstructed tracklets optimised for triggering and normalised to global track inclination and offline tracklets, respectively. The pion efficiency at 75 % electron efficiencies for the online scenario is projected on the much higher statistics offline data set using a normalisation factor of 15 %. The target 1 % pion efficiency at 2 GeV/c momenta will be reached at 75 % electron efficiency.

The identification of particle species in this case is done offline based on reconstructed secondary vertices (V_0 candidates) due to photon conversion, K_0 and Λ decays. It is worth noting that the TRD 1-dimensional PID is formed out of two ingredients, the total charge and the track inclination. For online tracklets, PID and inclination (local momentum) cannot be optimised

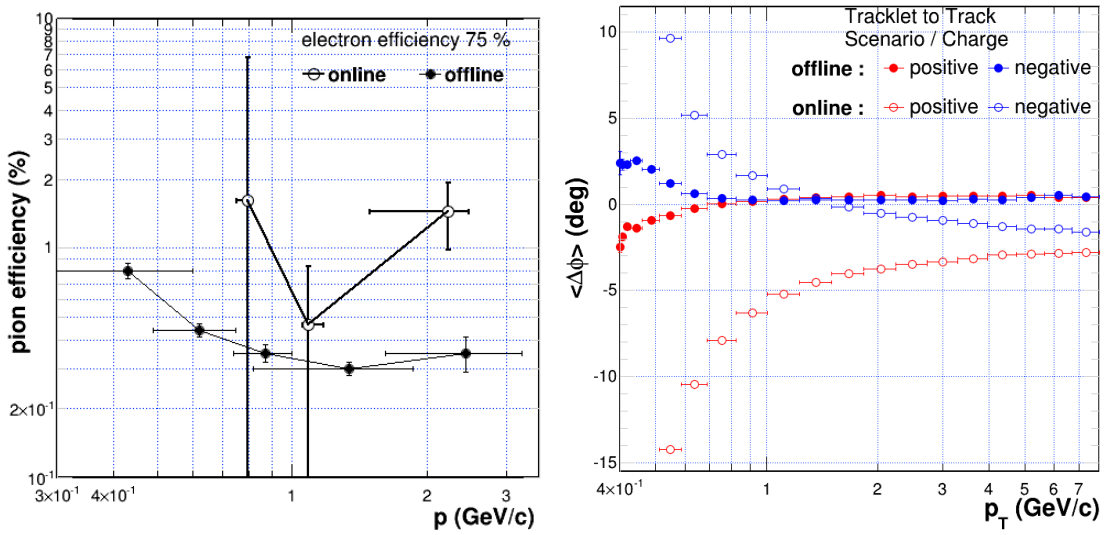


Figure 8.3: TRD reconstruction performance relevant for particle identification. The online [open symbols] tracklet scenario, trigger tuned and normalised, π efficiency for 75 % electron efficiencies and the corresponding ofline [filled symbols] performance for particles registered in 6 TRD layers (left) and the characteristic shifts of angular residuals ($\Delta\phi$) in the bending plane for positive [red] and negative [blue] charged particles for the two tracklet reconstruction scenarios (right).

simultaneously. Rather, PID can be best calculated after global tracking is performed using the good online position information. For the upgrade data without TRD electron trigger, this poses no limitation.

8.4 TRD read-out and trigger

8.4.1 TRD read-out unit

In the following paragraphs the specifications for a new TRD read-out unit are presented (see also Fig. 8.4). The major upgrade is the higher bandwidth interface to the O^2 system: instead of the full zero-suppressed ADC data for a small subset of L1 accepted events, the full minimum bias triggered front-end electronics (FEE) data stream has to be transferred. Currently the GTU modules implement the TRD read-out functionality [49].

The expected data volume per sector is below 20 Gb/s (see Tab. 8.1). This translates into two read-out units (RU) per TRD sector, each with one DDL3 link to the O^2 system. The read-out has 30 optical input links, each transferring data from the FEE of one TRD half chamber at a net data rate of 2 Gb/s. In case of tracklet read-out, the data transfer from the FEE is active for less than 12 % of the time for all scenarios shown in Tab. 8.1. Together with the 5 times higher bandwidth of the DDL3, the 30:1 ratio of FEE input links and DAQ output link on one read-out unit is adequate.

The read-out must be able to handle different event types: (A) tracklet data (B) full zero-suppressed raw events for calibration, (C) partial raw data and (D) full non zero-suppressed raw events (not in physics runs). Table 8.2 shows event sizes and buffer requirements for typical cases of the various event types.

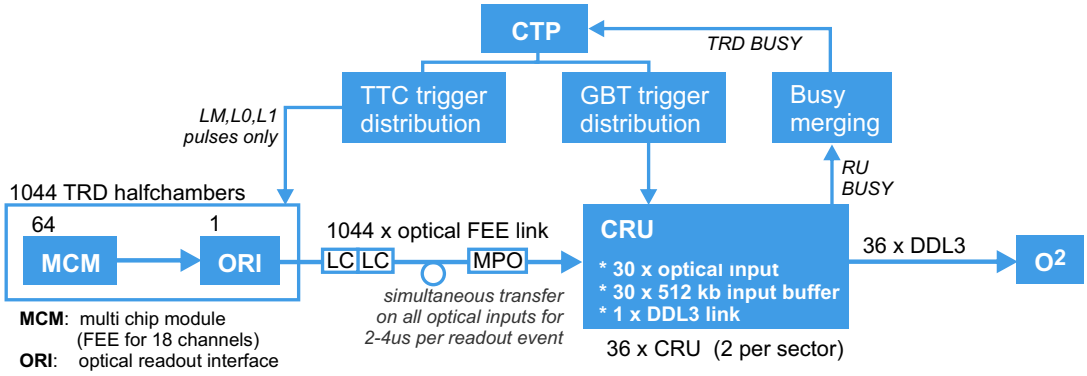


Figure 8.4: Block diagram of the TRD read-out unit.

Event type	event size [kB/event/sector]	data volume [kb/evt/input link]	number of events in 512 kb link buffer
50 % tracklet words (A)	30.8	4	128
minimum bias raw (B)	200	27	19
central raw (B)	$\approx$ 700	100	5
minimum bias partial (C)	40	5.4	95
non zero-suppressed raw (D)	$\approx$ 3000	400	1

Table 8.2: Event size and read-out input buffer capacity for various event types.

The input buffers on each FEE link act as multi-event buffer (MEB) for the read-out. The FEE data transfer to the read-out units uses a pure push mechanism without handshake or busy. To avoid data loss during this transfer, the read-out input buffer size and bandwidth have to be large enough to accept at least one event of maximum possible size simultaneously on all links. The largest possible event type, a non-zero suppressed raw event, requires a buffer size of 400 kb. This size allows the storage of a sufficient number of events for all event types in physics runs as shown in Tab. 8.2. With e.g. 512 kb link buffers, the single buffer can equally hold five central raw events or 64 events with maximum number of tracklets using a dynamic event buffer size.

For the interface to the O^2 system, there are no specific requirements from the TRD. Any chosen common ALICE DAQ link can be implemented for the TRD read-out with the choice of a suitable FPGA device. The goal for the TRD read-out is to use the ALICE common read-out unit (CRU). The scheme of 30 FEE optical links inputs and 1 DDL output maps to one AMC40 card.

The CRUs for the TRD are ideally located in the counting room, allowing full accessibility during data taking. Alternatively, the CRUs can be installed in the current GTU racks in the C-area, re-using the existing fibers from the TRD supermodules to the GTU (1044 fibers) and from the GTU to the DAQ area. In the C-area, the level of radiation is not a concern for the CRU. Besides the impact on cost for the extension of 1044 optical fibers to the counting room for the first option, the feasibility in terms of the optical power that can be driven by the FEE for the extended optical links and with the additional multi-fiber push-on (MPO) connectors (see Fig. 8.4) for both options has to be evaluated carefully.

Contributing Institutes
University of Frankfurt, Germany
Gesellschaft für Schwerionenforschung, Darmstadt, Germany
University of Heidelberg, Germany
University of Münster, Germany
NIPNE Bucharest, Romania
Tokyo University, Japan

Table 8.3: TRD Institutes.

Schedule		
New data formats	2015-17	test runs with beam (pp, Pb-Pb); performance evaluation and optimisation of data content
	2016-18	modification of software (offline reconstruction, calibration, data quality monitoring)
Read-out unit	2015-17	firmware development and tests with prototypes
	2018	commissioning of all units

Table 8.4: TRD schedule.

8.4.2 Trigger and busy handling

For operating the TRD, trigger sequences need to be provided to the FEE and in parallel to the CRUs. The FEE mounted on the detector chambers will remain unchanged for the upgrade, employing a TTCrx device to receive and distribute trigger information to all FEE devices. Therefore, a TTC system for trigger distribution is needed for the TRD. The FEE requires a special trigger sequence on the TTC A-channel, which is not compatible with the standard ALICE TTC trigger sequence. It consists of individual pulses, one bunch crossing wide with a fixed timing for each provided trigger level. No TTC trigger messages are used on the FEE, thus no rate limit is imposed by using the TTC at high rates for the TRD.

For the TRD FEE, a single trigger level (LM) is sufficient to initiate the full processing and read-out sequence. The timing of the LM signal has to be identical to the current TRD pretrigger with an arrival time at the FEE of, at the latest, 900 ns after the interaction, in order to record the full signal shape including the early amplification peak. The FEE supports up to two additional trigger levels: an L0 or L1 trigger, which, in case of tracklet read-out mode, is faster than 4 μs, can abort the FEE processing and thus reduce the dead time for L0 or L1 rejected events.

The CRUs receive a full standard trigger sequence including trigger messages which are used for busy generation and event formatting.

The CRU generates the TRD busy signal for the CTP. Each CRU asserts busy upon arrival of an LM trigger and releases the busy as soon as event end-markers are received on all FEE links or a time-out occurs. Moreover, busy is asserted in case of full buffers.

8.5 Schedule, funding and institutes

Tables 8.3, 8.4 and 8.5 show the TRD institutes, schedule and funding.

		Funding
Read-out unit	36 CRUs, fiber connectors, crate, trigger & busy distribution	420 kCHF (CRUs in C-racks)
		additional cost for fiber routing to counting room
Manpower	firmware and software development	
	2015-16	1 FTE
	2017-19	2 FTE

Resources for funding will be requested from BMBF

Table 8.5: TRD funding.

9 Time Of Flight detector - TOF

9.1 Introduction

This chapter discusses the implications of the increased interaction rate after the upgrade and the resulting requirements for the read-out of the TOF detector. During Run1, the current of the MRPCs increased linearly with the LHC luminosity, as shown in Fig. 9.1 (left) [50] and no abnormal noise currents were observed. Taking into account the average track multiplicity and the ALICE interaction rate, the two horizontal axes were aligned to the same detector load (number of particles hitting the TOF). Considering again the interaction rate at ALICE and the TOF hit multiplicity per event, we estimated the average rate of particles in the detector as a function of the total TOF current. This is shown in Fig. 9.1 (right) [50] and we observed a maximum average TOF rate of 14 Hz/cm^2. From the two plots in Fig. 9.1, it is possible to extrapolate the TOF rate to the luminosity foreseen in the ALICE upgrade beyond 2018. The expected rates will be 60 Hz/cm^2 in Pb-Pb: test beam results [51] indicate that also in the high-luminosity LHC period the MRPCs will be able to operate without loss in performance. From Fig. 9.1 (right) it is also possible to compute an average induced charge of $\approx$ 6 pC per track. This value is slightly higher than what was obtained in test beam [52], but still compatible. The difference depends on the fact that in ALICE the particles are of different species and cross the MRPC at different angles and with different momentum spectra. This low charge ensures a good rate capability and protects the detector from aging [51]. Further details can be found in [50].

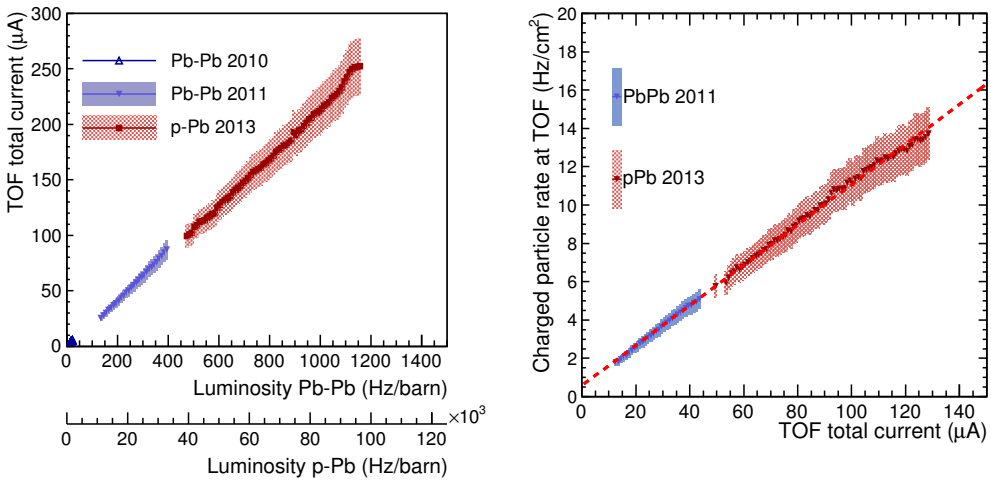


Figure 9.1: The TOF current versus luminosity in Pb-Pb and p-Pb (left). The TOF estimated rate versus HV current (right). In both figures the points and the bands indicate the average and the spread of the measurements, respectively. The dashed line is the linear fit to the 2013 data.

The present TOF read-out can already cope with triggers of tens of kHz. For the ALICE upgrade program, the main aim will be to further increase the present limit up to the foreseen minimum bias trigger rates both in pp and Pb-Pb interactions. As explained in the Letter of Intent, this can be achieved without major modification of the present hardware. A continuous read-out would be instead unaffordable both for hardware and budget reasons.

In the following, the TOF read-out will be briefly reviewed and the main hardware and software modifications for the upgrade will be described. With respect to what was anticipated in the Letter of Intent, and consist with the ALICE trigger strategy discussed in this report, we do not foresee updates of the existing TOF trigger capabilities. At present, after the upgrade, it is envisaged to use the TOF trigger only for commissioning purposes to provide a cosmic trigger to central barrel detectors.

9.2 TOF present read-out and limitations

The existing TOF read-out [53] is shown in Fig. 9.2. Each of the 18 azimuthal sectors of ALICE houses a TOF SuperModule, which is read out by 4 electronics crates. In each crate 1 DRM (Data Read-out Module) collects the data of 10 TRMs (TDC Read-out Module) [54], each of them including 30 HPTDC [55, 56] chips: 2400 channels are read-out in each crate. The pipelined internal architecture of the HPTDC chips coupled with read-out buffers in the TRMs allows a zero dead-time read-out. The local trigger modules (LTM) and the cosmic and topological trigger modules (CTTM) provide a trigger input to the CTP.

The read-out is done in three distinct phases:

(1) HPTDC read-out: The read-out of HPTDC chips internal buffers and shipping of data to TRM internal memories.
(2) VME read-out: The read-out, over the VME bus, of the 10 TRM cards.
(3) DAQ read-out: The shipping of data from the DRM to the ALICE Central DAQ over a DDL link.

In terms of DDL links, data segmentation is equal to the number of crates, which is 72. At L1 arrival ($\approx$ 6 μs after collision), a trigger is sent to the HPTDC and step (1) is performed. At the L2 arrival ($\approx$ 80 μs after collision), the TRMs are read out (step (2)) and data are sent to DAQ (step (3)). The large latency between L1 and L2 is exploited to read HPTDC. This will be different in after the upgrade.

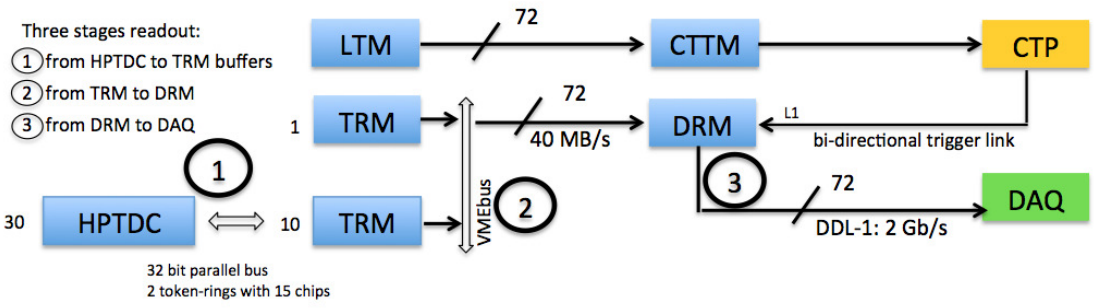


Figure 9.2: Current read-out TOF scheme.

The existing limitations of the current scheme were discussed in the Letter of Intent and, extensively, in [57].

In short, the system which was operated during Run1 was limited by several factors. The first limitation was the number of DAQ LDCs serving multiple TOF DDL links and the servers used for that purpose. In practical terms, the read-out was limited to some tens of kHz, already close to the foreseen targets for ALICE upgrade in Pb-Pb runs. These limitations will be removed in the new online computing scheme.

The system analysis in 2012 and further measurements performed in 2013 showed that the read-out time of the HPTDC chips inside TRM cards sets a 265 kHz upper limit for the absolute maximum trigger rate that can be sustained by the TOF. This corresponds to the time needed to perform a full scan (via a token ring) of the 30 HPTDC housed in each TRM when there are no hits to be read out. Replacement of these cards (and of the HPTDC chips) is therefore not planned.

Between the maximum theoretical achievable rate and present DAQ limitations, subsequent additional bottlenecks come from the data transfer speed over VME (currently $\approx$ 40 MB/s), the current trigger dispatch protocol and the performance of DDL links with small size payload per event. A hardware upgrade of the existing read-out card might not be strictly needed because a 50 -100 kHz sustained rate could be potentially reachable by upgrading the firmware but this would limit the TOF contribution in pp runs and it would not allow the exploitation of the new DDL and TTS link capabilities.

In the Letter of Intent, the roadmap towards the preparation of this TDR to study and remove these limitations was described. Results and work in progress are presented in the next section together with the conceptual design of the anticipated new read-out card.

9.3 Upgrade implementation architecture

The ALICE DAQ group performed rate tests with the last generation of DDL1 RORC over PCIe and most recent PC mother-board with respect to those used at ALICE during Run1. On the transmitting side, a test bench card similar to the on-detector part of the DDL was used to verify maximum achievable rates with an event size comparable to the foreseen payload from TOF crates ($\approx$ 340 bytes). The test card implemented a custom source interface unit (SIU), which is identical to the current version installed in TOF DRM cards. Rates up to 400 kHz have been reached even with a lower block size (200 bytes), making it clear that the TOF will not suffer limitations from the DAQ bandwidth for the upgrade. The installation of DDL2 on the new DRM cards will further avoid any bottlenecks on this respect.

The data segmentation will remain the same (i.e. the whole TOF is read-out via 72 DDL links, each corresponding to the read-out of one VME crate).

The data size per DDL link will depend on event multiplicity. For almost empty events (in minimum bias events in pp collisions, 50 hits/event are expected in the full TOF) this will be $\approx$ 340 bytes growing up to $\approx$ 1500 bytes for most central collisions in Pb-Pb. Average multiplicity in Pb-Pb is foreseen at 2000 hits per event (500 bytes/event crate payload).

Internal HPTDC buffers allow to comfortably wait, with zero dead-time, for the arrival of a trigger signal. Upon trigger reception, the signal will be passed to HPTDCs and VME read-out will start immediately after they are made available on the read-out FIFOs inside the TRMs. It is important to note this is currently done when awaiting the L2 accept signal, so this does not

add to the read-out time. After the upgrade, this will be different. The previously discussed time to scan and read out HPTDCs (could be up to ≈ 7 μs in the highest multiplicity events) will be the main limiting factor. The time transfer over VME will then determine the maximum achievable TOF rate.

To improve the VME throughput over the backplane, we plan to take advantage of the fact that all VME cards (master and slaves) work on the same LHC clock. This can be exploited particularly by implementation of a synchronous protocol as the 2eSST VME standard. On the other hand, we are limited by the existing hardware (both FPGAs and VME bus transceivers) mounted on the VME slave cards. The implementation of a simplified 2eSST protocol was tested by demonstrating that a peak rate of 160 MB/s is achievable, avoiding initial rate negotiation as foreseen by the original industrial standard [58]. The theoretical achievable throughput, limited by the performance of the existing VME slave cards, is 160 MB/s, but the actual rate depends also crucially on the time spent during the initial data transfer phase (asserting addresses on the backplane). Further optimisations are planned already in 2014 and the upgraded firmware (for the VME read-out) will be tested extensively during Run2.

Taking together the set of these results and developments, it is possible to confirm that the only hardware intervention to adapt the TOF to the upgrade environment will be the production of a new DRM card.

In front of a relatively small investment, the TOF will gain greater benefits upgrading its DRM card. This will allow to reach higher rates without any busy time (likely up to the foreseen 200 kHz target in pp) which will ensure that in a short time a high statistic sample can be acquired in pp collision with events containing ITS, TPC and TOF read-out. The benefits for the ALICE physics program are evident. Moreover, this hardware upgrade will allow the use of more modern TTS and DDL links, including a better handling of the busy signal over the new TTS system implemented using GBT links. Even if the multibuffer system - built-in inside the HPTDC architecture - allows the TOF to safely handle many triggers, the busy will need to be dispatched with minimal latency (O(μs)) to protect against FIFO overflow and other potential busy reasons (DAQ not coping with data and some VME cards not ready). With a new DRM card, we might further expect some benefits on the 2eSST obtainable performance (that is a 160 MByte/s bandwidth), improving the hardware of bus transceivers on the master card. However, this is not guaranteed because the hardware of the VME slave cards will not be upgraded.

Figure 9.3 shows the read-out scheme after the foreseen upgrade.

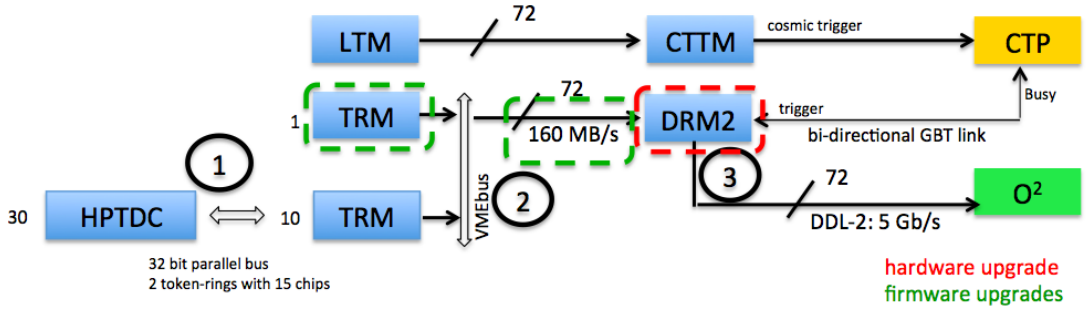


Figure 9.3: New TOF read-out scheme, with upgraded components highlighted.

Not all the technical implementation details of the new DRM card (DRM2) have been already defined, mainly due to some remaining uncertainties about the new hardware supporting trigger and DAQ links. Production of prototype cards is expected to start in 2014 following availabilty

of chosen standards.

A conceptual design layout of the card is shown in Fig. 9.4 and we list here some considerations and information about hardware choices and differences with respect to the existing card.

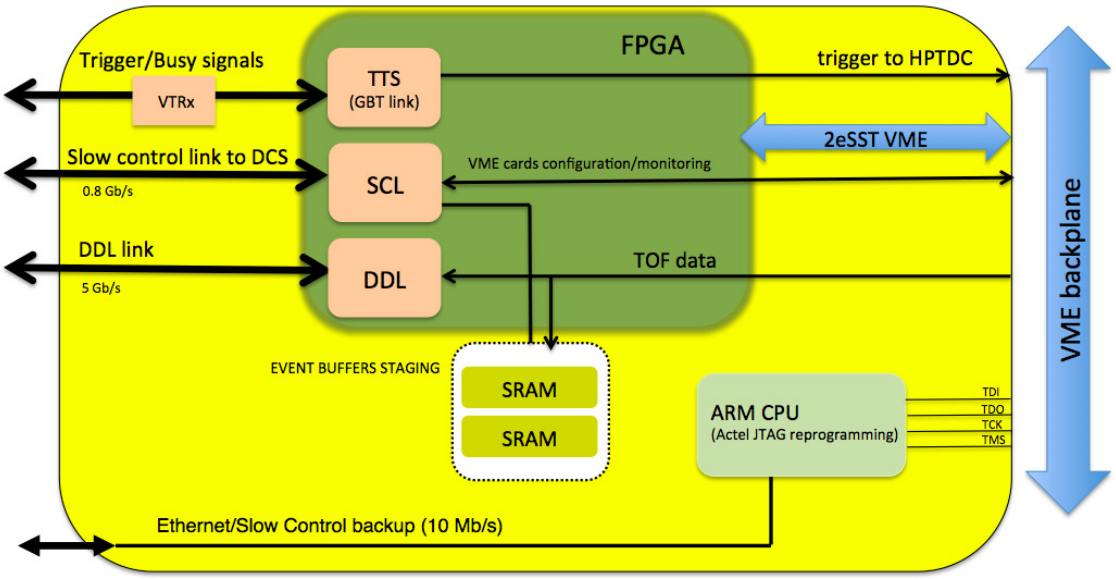


Figure 9.4: Conceptual design of new version of the TOF Data read-out Module

- a SmartFusion2 FPGA from Microsemi is the current favourite candidate for DRM2 and an obvious successor of the Actel APA750 currently used on the DRM. Being Flash programmed, it provides SEU-immune configuration cells and it has several built-in radiation tolerant features such as SEU-protected memories. Interestingly, this FPGA features high-speed serial interfaces (important to implement IP cores towards new TTC and DDL links) and an ARM CPU core. Given its capabilities are much higher than the current FPGA used in the DRM, we are very confident it will be able to replace the second FPGA (an Altera Cyclone) currently on board on the existing DRM, taking care of the slow control optical link.

- the Slow Control Link is used by the TOF DCS servers to monitor and configure Front End Electronics. It is additionally used to collect and monitor data during data acquisition, to perfrom data consistency verification and monitoring of several DCS parameters (namely temperatures and thresholds). The memories shown in the Fig. 9.4 are used to stage collected data in multi-events buffers for DCS transfers. This arrangement worked very well during Run1. Before Run2 the back-end links will be already upgraded to PCIe, similarly to what the ALICE DAQ did for D-RORC cards.

- an ARM processor was installed inside the current DRM to enable remote programming of Actel FPGAs inside TOF VME cards, via a custom JTAG bus implemented on the VME backplane. The current hardware, a commercial piggy-back card mounting an ARM Atmel processor running Linux, could be reused. However, we will explore whether the ARM core inside the Microsemi FPGA could be used for this purpose, simplifying the design of the card.

- for the TTS link, a bi-directional GBT link is foreseen, also to provide the busy signal to the Central Trigger Processor.

- The interface to the back-end DAQ will be a DDL2 link as baseline option. The encoding will be again implemented inside the FPGA via an IP core provided by the ALICE DAQ group. The implementation of a DDL2 link on the new DRM will take advantage of the expertise gained by TPC and TRD groups during Run2 (a DDL2 link is operating on the Read-out Control Unit (RCU) for these detectors).

Radiation tests will be carried out as necessary. We plan to use largely the existing tested components on the DRM, exploiting the know-how gained during DRM electronics development (with features like a watchdog microprocessor protecting against latchup). We will also rely on irradiation tests which are currently being carried out by other ALICE groups on SmartFusion2 FPGAs.

9.4 Schedule, funding and institutes

A total cost of 750 kCHF (600 kEU) is foreseen for the production of the new DRM cards and related R&D costs (prototype cards, radiation tests, software licenses, test setup in laboratories, etc.). The foreseen upgrade schedule with spending profile is shown in Tab. 9.1.

Year	Activity	Cost [kEUR]
2013	Firmware development (2eSST)	15
2014	Test of new FPGA with GBT and new DDL links	35
2015	Prototype card: finalisation of specifications, radiation tests, tendering	50
2016	Start of production of DRM cards	250
2017	End of production	250
2018	Installation and commissioning	
	Total	600 / 750 kCHF

Table 9.1: TOF upgrade plan: spending profile is also shown.

The involved institutes in this project are summarised in Tab. 9.2.

Institutes
Sezione INFN and Dipartimento di Fisica dell'Università, Bologna, Italy
Sezione INFN and Dipartimento di Fisica dell'Università, Salerno, Italy
Centro Studi e Ricerche e Museo Storico della Fisica "Enrico Fermi", Rome, Italy
Gangneung-Wonju National University, Gangneung, South Korea
Institute for Theoretical and Experimental Physics, Moscow, Russia

Table 9.2: TOF institutes.

10 Fast Interaction Trigger - FIT

10.1 Introduction

The present ALICE detector employs three forward detector systems, the T0 [59], V0 [60] and FMD [61], that provide minimum bias trigger, multiplicity trigger, beam-gas event rejection, collision time for TOF, offline multiplicity and event plane determination. In order to adapt these functionalities to the collision rates of the ALICE upgrade, it is planned to replace these systems by a single detector system, called the Fast Interaction Trigger (FIT). Two sensor technologies are investigated for FIT. They represent improvements of the current T0 and V0 detectors. We refer to these modified detector components as T0-Plus and V0-Plus. While it would be possible to build the FIT based on only one technology, it might lead to loss of redundancy and partial reduction of functionality. We intend to investigate both sensor technologies concurrently and to develop front-end electronics suitable for both technologies. The read-out system adopted for FIT will follow the scheme of the current T0 detector using the modified DRM (Data Read-out Module) and TRM (TDC read-out Module) developed for the TOF detector. For this reason, even if FIT employs both sensor technologies, it will appear as a single detector system.

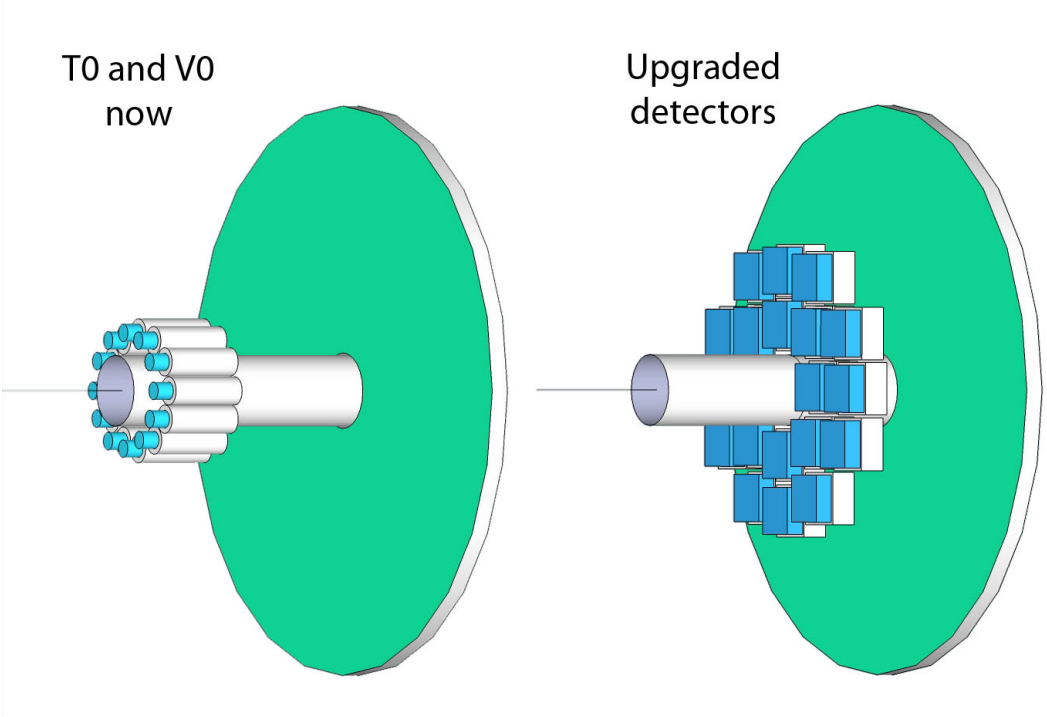


Figure 10.1: Conceptual drawing of the trigger detectors on the C-side as they are now (left) and after the upgrade (right). The new T0-Plus detector will consist of 20 rectangular modules. Although the upgraded V0 detector will have a modified light collection system, the area covered by the scintillator would remain the same.

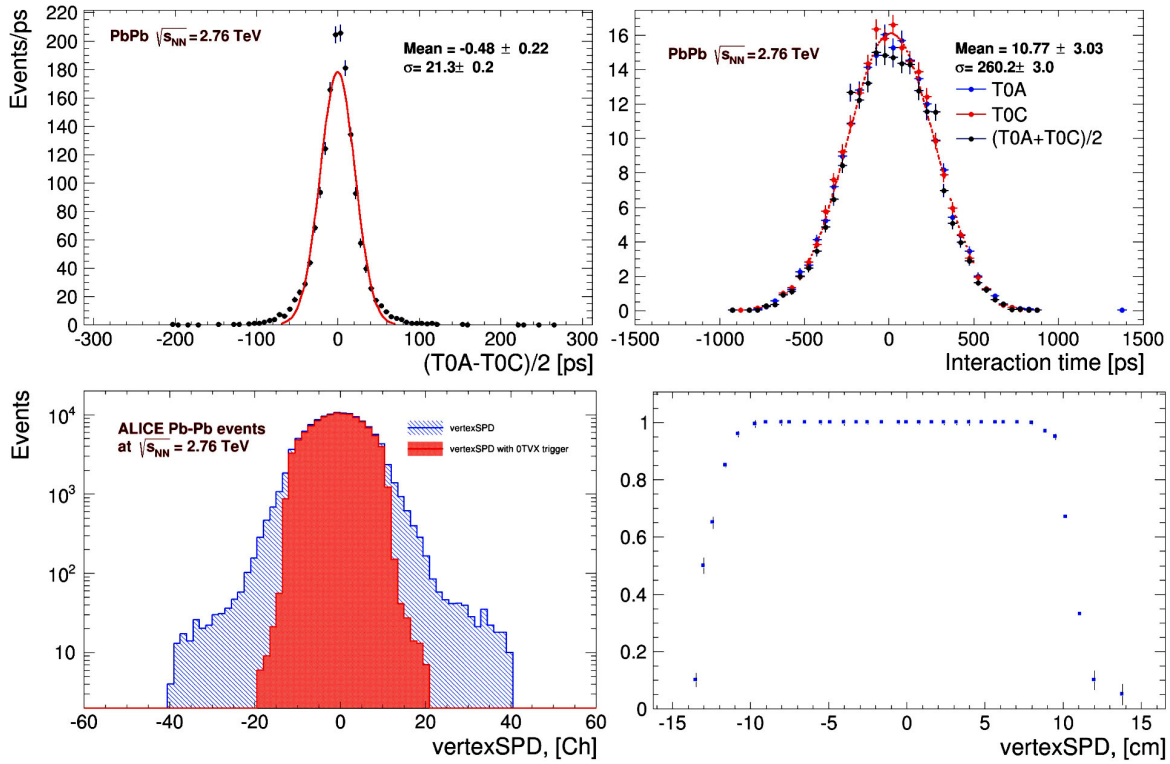


Figure 10.2: Performance of the current T0 detector for Pb-Pb collisions as measured in 2011. Distribution of (T0A-T0C)/2 corrected for slewing and vertex (top left). Distribution of the interaction time measured by T0 (top right). Background rejection by T0 (bottom left). T0 vertex trigger efficiency for central and semi-central collisions (0-50%) (bottom right).

10.2 Performance of the current T0 detector

The current T0 detector consists of two arrays of Cherenkov counters (T0C and T0A) positioned at the opposite sides of the Interaction Point (IP) at distances of -70 cm and 370 cm. Each array has 12 cylindrical counters equipped with a quartz radiator and a photomultiplier tube (see Fig. 10.1). T0C covers the pseudo-rapidity range $-3.28 < \eta < -2.97$ and T0A covers $4.61 < \eta < 4.92$. Due to the small acceptance of the T0 arrays, the time resolution and efficiency of the T0 detector improve considerably with event multiplicity. For instance, in pp collisions, the T0 system achieves a 40 ps time resolution and 50 % vertex efficiency. For central and semi-central events (centrality range 0-60%) in Pb-Pb collisions at $\sqrt{s_{NN}} = 2.76$ TeV, the corresponding values are ~ 21 ps for time resolution and close to 100 % for vertex efficiency, as shown in Fig. 10.2.

T0 electronics

The block diagram of the electronics and read-out scheme used by the present T0 detector is shown in Fig. 10.3. The signals of each of the 24 PMTs are fed to preamps housed in the so-called shoeboxes, placed 6 meters from the detector. The main reason for the shoebox was to provide the wake-up signal for the TRD. However, this will be derived in a different way already after LS1. Nevertheless, because of the considerable distance between the photo-sensors and the electronics racks where the fast electronics will be located, we envisage the first stage of

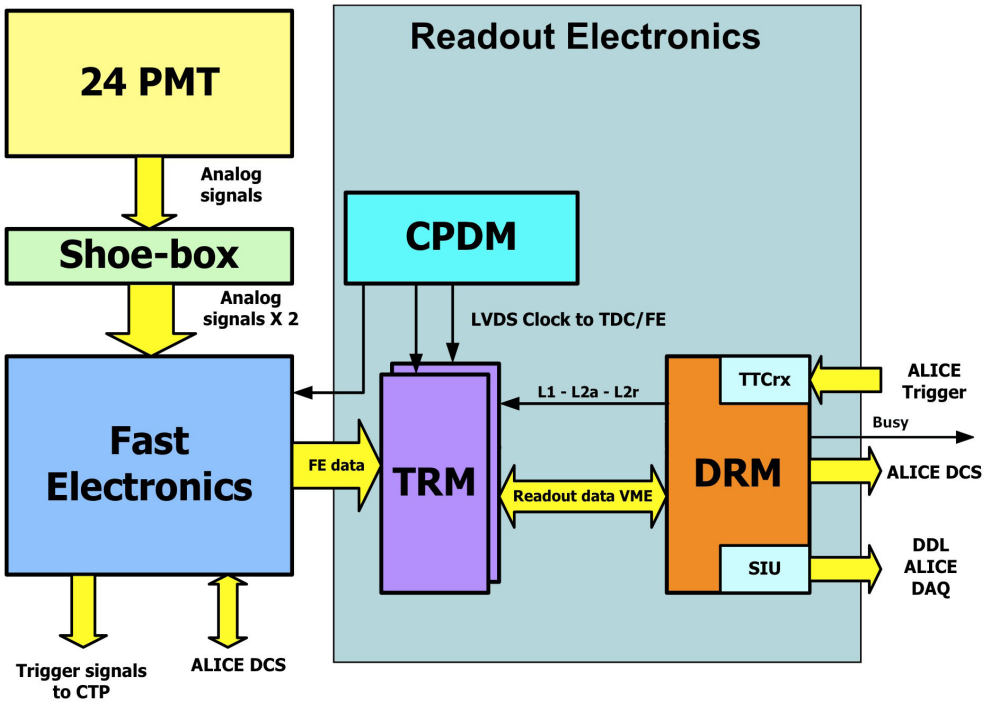


Figure 10.3: Trigger and read-out electronics of the present T0 deteector.

signal amplification at a distance of no more than 3 m from the detector. From the shoebox, the signals are sent to the trigger and read-out electronics located in the racks outside the magnet. The fast trigger electronics includes processing of the PMT signals, generation of the required trigger signals and shaping for digitisation and storage by the TRM and DRM modules.

The read-out electronics processes, digitises, and sends for storage the arrival time and amplitude from each of the photo sensors. The main components of this system are custom VME crates (SY2390), the TRM, the CPDM (Clock and Pulse Distribution Module) and the DRM. All these components are equivalent to the ones developed for the TOF detector. The same general architecture, with an increased channel number, will be used by FIT.

10.3 Performance of the current V0 detector

The V0 system consists of two discs at distances of -90 cm and 329 cm from the IP and cover the pseudo rapidity-ranges $2.8 < \eta < 5.1$ and $-3.7 < \eta < -1.8$. The two detectors are segmented in four rings and 8 sections in the azimuthal direction. The system is made of plastic scintillator from Bicron and light is collected with wave length shifting (WLS) fibers embedded in both faces of V0A or glued along the radial edges of V0C.

The V0 systems generate two types of trigger signals. One type is based on pre-adjusted time windows that corresponds to beam-beam or beam-background in coincidence with the time signals from the detectors (see Fig. 10.4 left). This is used for minimum bias, beam-gas and multiplicity triggers. The second type is based on total charge and is used to trigger on multiplicity.

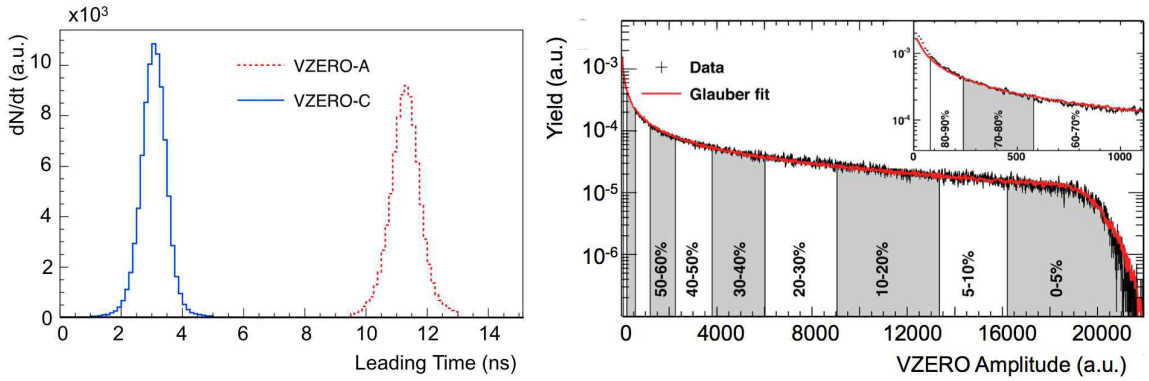


Figure 10.4: Time of flight distribution of V0A and V0C obtained with pp collisions after a weighted average [60]. The RMS value of the distributions are 450 ps and 350 ps respectively (left).The sum of amplitudes in Pb-Pb collisions at $\sqrt{s_{NN}}$=2.76 TeV. The red line shows the Glauber model. The shaded areas define centrality classes [60] (right).

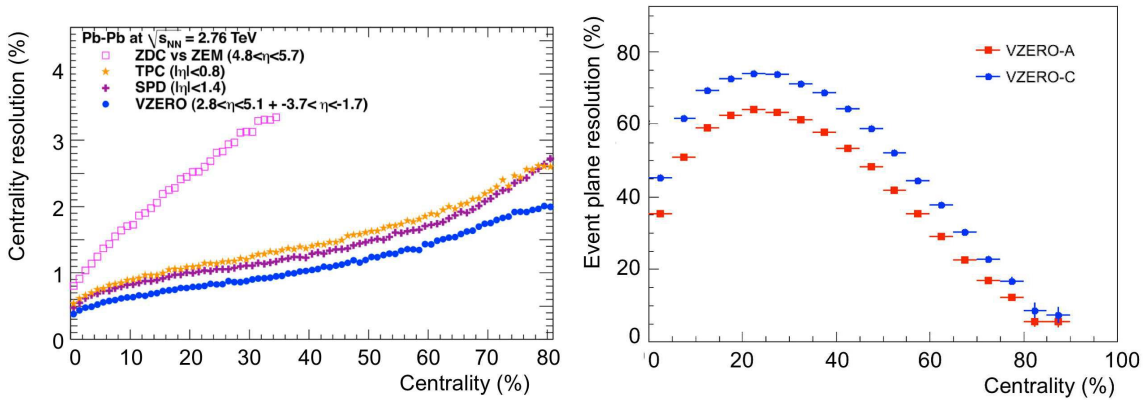


Figure 10.5: Resolution of the centrality determination by different ALICE sub-systems [62] (left). Resolution on the event plane determination with the V0 for the second harmonic as a function of the centrality percentile (right).

The V0 system also provides on-line monitoring of the luminosity and background rates using a time coincidence between the two V0 arrays.

A typical distribution of V0 amplitudes used for centrality selection is shown in Fig. 10.4 (right). Figure 10.5 (right) shows the resolution of the event plane as determined by the V0.

V0 electronics

The 32 channels of each V0 detector are received by a FEE that splits each PMT pulse into two. One is fed into charge-to-digital converters to integrate the charge. The other is amplified by a factor of 10 and provides the leading edge timing as well as the width at the discriminator threshold. The time information of both leading edge and width is digitised by time-to-digital converters.

The block diagram in Fig. 10.6 shows the concept of the present V0 read-out [63]. The shoebox in the diagram provides the wake-up signal to the TRD. It is one of the features that will disappear in the future system. The Channel Interface Unit (CIU) performs charge and time digitalisation. It contains an HPTDC that gives a precise time information for 8 channels, i.e.

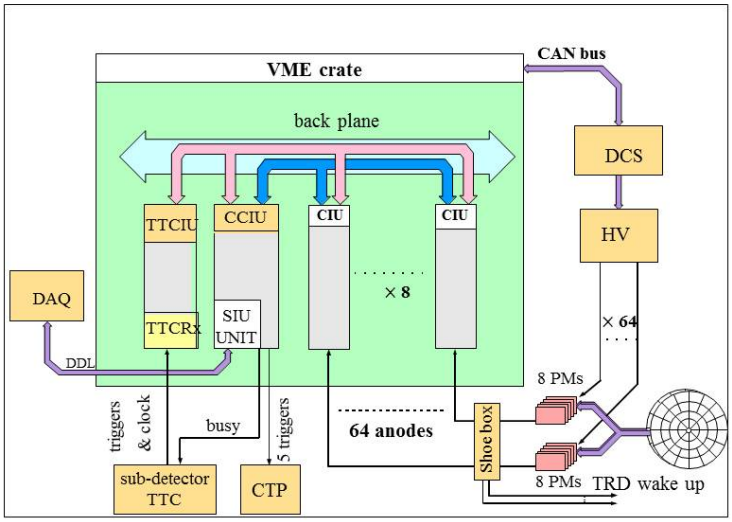


Figure 10.6: Block diagram of the present V0 read-out electronics.

one ring of V0. The CCIU performs the interface function between the DAQ and the electronics as well as the final processing of the trigger signals.

10.4 Required functionality for the FIT

The upgraded trigger detector needs to fulfil the following requirements:

- Minimum Bias trigger for pp collisions with efficiency comparable to the current V0, i.e. at least 83 % for vertex (A&C) and 93 % for the OR signal (A|C).
- Event Multiplicity determination capable of selecting and triggering on central as well as on semi-central collisions. The centrality selection should match the performance of the present V0.
- Vertex location with a performance comparable to the present T0 system.
- Evaluation and rejection of beam-induced background and in particular beam gas event sensitivity on the level of the current V0 detector.
- Time resolution better than 50 ps for pp collisions, as in the present T0 system.
- Determination of collision time for TOF with resolution better than 50 ps.
- Event plane determination with a precision similar to the present V0 system (see Fig. 10.5)
- Minimal ageing over the ALICE operation period.
- No after pulses or other spurious signals.
- Direct feedback to LHC on luminosity and beam conditions.

10.5 T0-Plus detector concept

The most natural approach to address the above requirements would be to increase the acceptance of the current T0 detector to match that of the V0. Using the present setup of a quartz+PMT is however impractical and not cost effective. Instead, a new concept with quartz radiators coupled directly to MCP-PMT-based light sensors is proposed. Figure 10.1 shows a sketch of 20 rectangular modules of such a detector at a position between the current T0 and V0.

MCP-PMT technology

An MCP-based trigger detector was considered in the 1990's, during the initial planning and construction phase of ALICE. At that time this technology was not selected, as its long-time reliability had not yet been established. Since then, rapid progress has been made, driven primarily by the demand for MCP-based night vision devices for the military. The most significant developments were:

- Atomic Layer Deposition technology [64]
- Modified photocathodes [65]
- Reduced outgassing (borosilicate glass)
- Commercially available self-contained MCP-PMT units

There are currently three producers capitalising on these developments: Hamamatsu (Japan), Photonis (USA), and BINP (Novosibirsk in Russia). According to our market survey (June 2013), the most suitable module for the trigger upgrade is XP85012 Planacon from Photonis.

XP85012 Planacon

The XP85012 Planacon consists of a sealed, rectangular vacuum box of about $59 \times 59 \times 28$ mm^3 housing a pair of microchannel plates in a chevron configuration [66], see Fig. 10.7. The pore size is 25 μm with the length to diameter ratio of 40:1. There are two front window options available: Schott 8337B or UVFS(-Q). The spectral range is 200-650 nm with peak sensitivity around 380 nm and an average quantum efficiency of 22 %. A gain of 10^5 is typically reached at 1800 V, with the maximum possible gain on the order of 10^7. The cathode is subdivided into 64 square sections that can be read out individually or combined into bigger blocks. Both the ambient operating temperature range and the behaviour in the magnetic field conform to the ALICE conditions inside the L3 magnet.

Planacon has the largest relative (80 %) and absolute (53 mm $\times$ 53 mm) active area and the lowest price per surface of all the commercially available MCP-PMTs, making it the prime choice for the T0 upgrade. The same product has been selected for the timing detectors for PANDA [67] at FAIR in GSI and for NICA [68] in Dubna. Both projects have already conducted significant R&D on this detector, which allows us to build on their results. Some of the test results shown in this chapter were obtained by the PANDA and NICA collaborations.

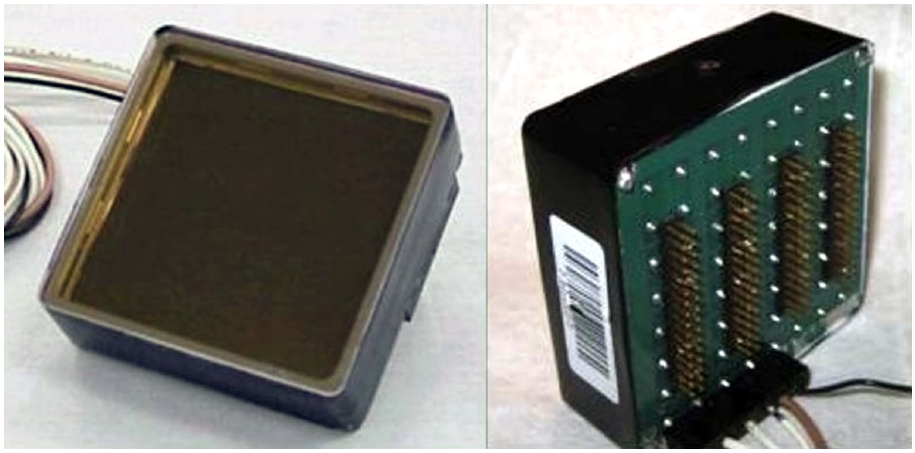


Figure 10.7: Photograph of a front (window side) and rear view of XP85012 Planacon.

Reliability and lifetime issues

Electrons multiplied by up to seven orders of magnitude in avalanches inside the microchannels inevitably degrade MCP surfaces, limiting the lifetime of the device. Likewise, the positive ions traveling in the opposite direction in the strong electric field also cause the generation of intense secondary electron showers and additional damage to the photocathode. The ageing of an MCP is typically reported by plotting the Quantum Efficiency (QE) as a function of the Integrated Anode Charge (IAC). Before the advent of Atomic Layer Deposition technology, MPCs suffered a drastic decrease in QE already after an IAC on the order of 100 $\mathrm{mC/cm^2}$. The latest tests with the Planacon XP85012 show no signs of degradation even after IAC of $\sim$5 $\mathrm{C/cm^2}$ [69], as shown in Fig. 10.8. Hamamatsu is now developing an MCP-PMT that will also push the limit beyond $\sim$5 $\mathrm{C/cm^2}$. The new product is expected on the market in 2015, that is, in time for the upgrade.

A minimum ionising particle (MIP) traversing a 20 mm thick quartz radiator generates about 1000 photons. The Quantum Efficiency (QE) of the Planacon QE is around 10 % hence 1000 photons from 1 MIP will trigger 100 avalanches. Typical gains in use are around 10^5. With such a gain there are 10^7 electrons that reach the anode per MIP, corresponding to a charge of 1.6×10^{-12} C. Referring to Sec. 3, the total number of tracks will be around 3×10^{12} on the innermost sensors and thus the total charge is close to $\sim$4.8 $\mathrm{C/cm^2}$. This value conforms to the already proven performance of PLANACON [69], giving us confidence that the new MCP-PMT units will perform well for the ALICE upgrade.

After-pulses

A serious issue complicating the use of PMT-based detectors (including the current T0 and V0) are after pulses. As can be seen in the left panel of Fig. 10.9, some 20-120 ns after the main pulse, after pulses with amplitudes of about 20% of the primary peak occur. This phenomenon is well known and is attributed to the acceleration of ions triggering secondary signals. For low-multiplicity events, that is when most of the primary pulses are generated by a single MIP traversing the radiator, this phenomenon is not a problem since the after pulses fall below the threshold of the discriminator. At higher multiplicities this is no longer the case. Since the amplitude of an after pulse scales roughly with the amplitude of the primary pulse, at higher multiplicities one gets potential problems especially when there might be an overlap with signals from the previous bunch crossing.

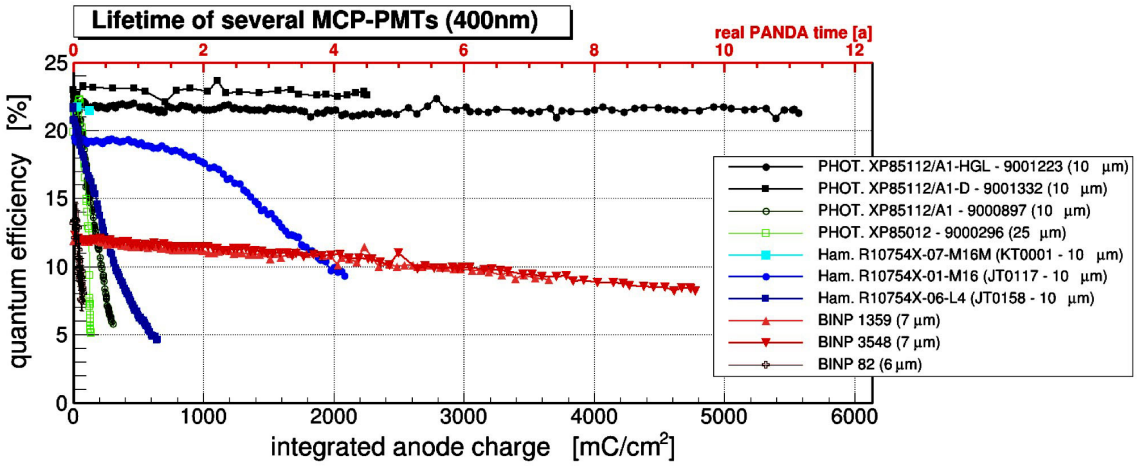


Figure 10.8: Dependence of the Quantum Efficiency on the Integrated Anode Charge for a variety of MCP-PMT sensors measured by PANDA collaboration. The performance of the ALD-treated samples from Photonis USA is shown by the top curves.

The MCP-PMT investigated has not shown any detectable after pulses, as can be seen in the right panel of Fig. 10.9.

Quartz radiators

The fragmented anode of the XP85012 makes the increase in granularity of the detector possible by dividing the quartz radiator into smaller segments (see Fig. 10.10). This is possible because the total internal reflection from the sides of the radiator segment directs all Cherenkov photons onto the photocathode directly under this segment. Such increase in granularity will improve the performance of the detector especially for high-multiplicity events.

Choice of quartz supplier

Two possible suppliers of quartz material for the radiator have been identified: Gus-Khrustalnyi from Russia, the producer of quartz KU-1, and Heraeus of Germany, which produces SUPRASIL 1. The former material is used by the current T0. The latter has a slightly wider transmission band at very short wavelengths. Both are suited for the upgrade of T0.

Surface coating

Cherenkov light cones generated by MIPs entering perpendicular to the front surface of a radiator do not lose much intensity upon reflection from the sides because the conditions for the total internal reflection are fulfilled. To take advantage of this fact, modules of the current T0C array are inclined to face the IP. When the entrance angle of charged particles increases, some of the light escapes from the sides of the quartz. It is, as yet, unclear if the space available for the upgraded T0 would be sufficient for tilting of the detector units towards the IP. If not, highly reflective coating of the radiator sides will be employed to minimise the light loss.

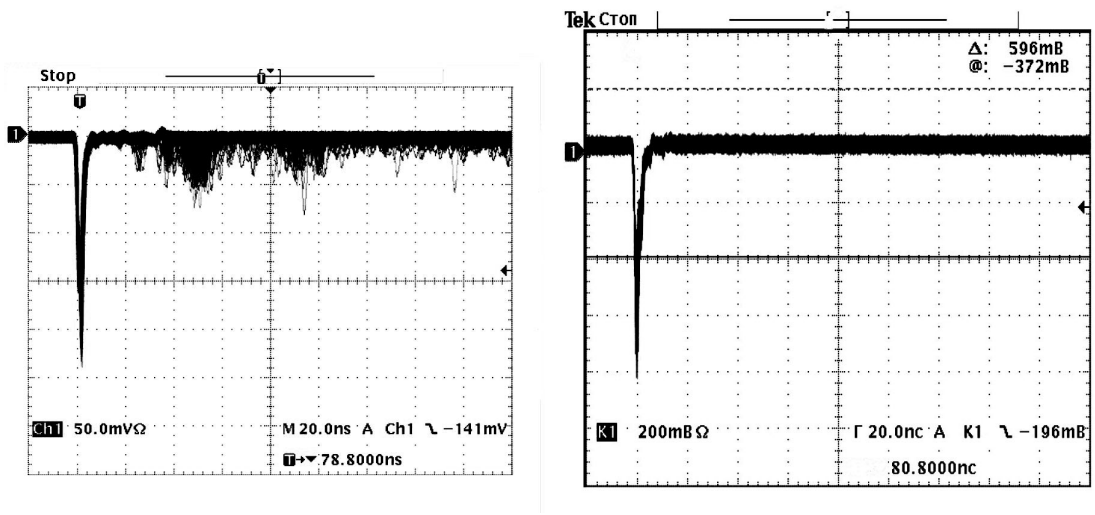


Figure 10.9: Oscillographs showing the shape of pulses from a PMT currently used by T0 detector (left) and from a XP85012 proposed for T0 upgrade (right). No after-pulses are visible in the Planacon spectrum.

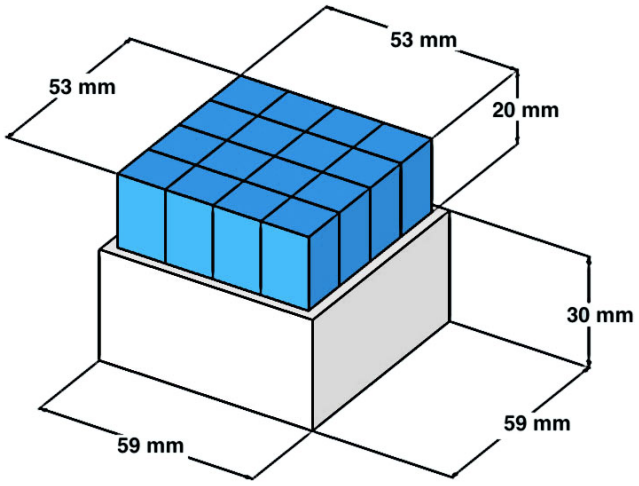


Figure 10.10: Concept of T0 module with a quartz radiator divided into 16 elements. The dimensions are approximate and do not account for detector housing and electronics.

Figure 10.11: Prototype of a detector module based on XP85012. Part of the outside cover is removed to show the rear side of the sensor with front-end electronics attached. This prototype has the quartz radiator and the anode divided into 4 equal sectors.

Also, coating of the front surface should be chosen depending on the desired performance for particles traveling in the opposite direction. Without any coating the polished front surface of the radiator would still reflect a sufficient amount of light towards the photocathode to generate a peak of roughly 50 % the normal amplitude. A properly selected light absorbing coating would remove this peak completely, while a reflective layer would bring the signal amplitude for particles traveling backwards closer to that of the normally traversing particles.

Final decisions on segmentation, angles, and optical coatings depend, of course, on the outcome of detailed simulations and the results of beam tests using various possible configurations. In any case our aim is to design T0-Plus that will be also able to monitor and measure beam-gas events. This is definitely possible but some more R&D is needed to find the optimum solution that would both be sensitive to the background events and yet be able to discriminate against them. This is a new feature of T0-Plus as compared to T0.

Detector prototyping

The results presented in here have been obtained with a prototype constructed by NICA collaboration (Fig. 10.11). Judging from the existing prototype, the minimum thickness of the fully assembled and cabled module is estimated at ∼10 cm. The sensor itself is ∼3 cm thick, the quartz would be 1.5-2 cm, the PCB with front-end electronics attached to the sensor ∼2 cm, and 1.5 cm in the front and 1.5 cm in the back to accommodate the bending angle and connector thickness of signal and electrical cables and optical fibers.

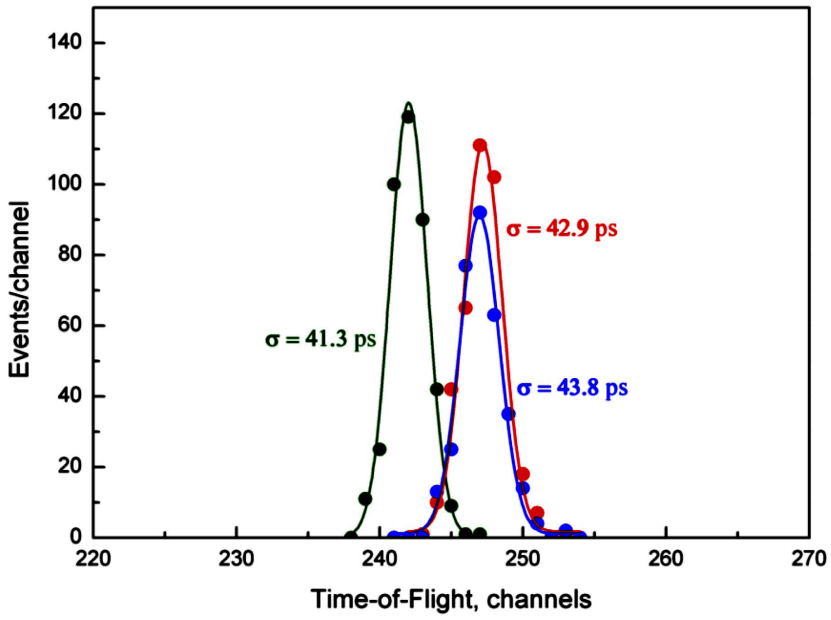


Figure 10.12: Measured TOF resolution obtained with cosmic rays for various pairs of MCP-PMT sectors obtained with the detector prototype shown in Fig. 10.11.

Time resolution

MCP-based devices are known for their very good timing properties. The tests conducted both by ALICE and the PANDA and NICA groups confirm the excellent performance of XP85012 in that respect as shown in Fig. 10.12. The Time-of-Flight resolution of 42 ps as measured with cosmic rays by a pair of MCP-based detectors corresponds to a resolution of 30 ps for a single detector element. As expected, the upgraded T0 should therefore have the same or even better time resolution than the current detector.

Efficiency

The intrinsic efficiency for a quartz radiator with an MCP-PMT detector is close to 100 %. That means that every MIP traversing a full path inside of the quartz generates a proper signal that will be registered. However, the geometric coverage of the detector unit is less than 100 %. The ratio of active surface to the physical outline of the XP85012 is 80%. When the necessary housing and mechanical support is added, this ratio will drop to about ∼75 %, depending on final design details.

Weight

According to the manufacturer, the approximate weight of XP85012 is 128 g. The weight of the $53 \times 53 \times 20$ mm^3 radiator made of fused quartz (∼2.2 g/cm^3) is approximately 124 g. The board with electronics and cable connectors together with a protective cover would bring the total weight of one module to 400-500 g. Therefore, the weight of a 20 unit array would be about 8-10 kg plus the weight of the HV cables (total of 20), signal cables (total of $4 \times 20 = 80$) and optical fibers (≤ 20).

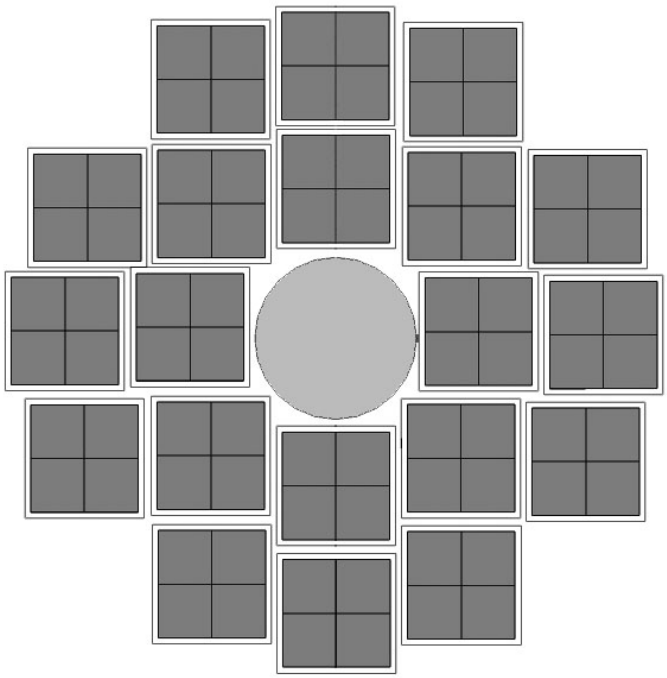


Figure 10.13: Proposed configuration and segmentation of 20 modules of T0-Plus detector around the beam pipe.

Acceptance and shape-optimisation

The demand to maximise the efficiency for Minimum Bias events requires efficient coverage of the available space with detector modules. The envelopes defined by detector integration are a minimum inner radius of 50-60 mm and a maximum outer radius of 170-200 mm. The proposed detector configuration is shown in Fig. 10.13. Each MCP-PMT module will be divided into 4 equal parts by cutting the quartz radiator into 4 and arranging the 64 anode sectors into the corresponding 4 groups. As a result, each array on the A and on the C-side will function as 20×4=80 independent detector units.

It is still to be decided whether to place the C-side T0-Plus detector on the front-absorber or on the so called cage that supports the beampipe, ITS and MFT. Fixation on the front-absorber allows an inner radius of 50 mm but has the drawback that the detector is only accessible if the TPC is moved to the parking position. Fixation on the support cage allows an inner radius of only 60 mm, but would ease the access to the detector.

For the detector optimization, a set of simulations with an ideal geometry, assuming a perfect ring detector, was performed. In these simulations, various values for R_{min}, beam pipe options, and placement along the beam axis were investigated. In addition, 15000 events generated with PHYTHIA6 for pp collisions at $\sqrt{s} = 14$ TeV were projected onto the real geometry of T0-Plus: 20 MCP-PMT sensors with $53 \times 53 \times 20$ mm^3 quartz radiators placed around beam pipe at 70 cm on the C side and 20 MCP-PMTs at 373 cm on the A side. On both sides, the distance from the center of the beam pipe to the outer edge of the sensor was $R_{\mathrm{min}} = 60$ mm. The same geometry was used for the simulation with HIJING of 8000 events of the most peripheral (b=13-20) Pb-Pb collisions at $\sqrt{s} = 5.5$ TeV. For all calculations, the standard beam pipe geometry (adopted for upgrade simulations) was used. Figure 10.14 shows the simulated T0-Plus efficiency as function of primary particle multiplicity in pp collisions, where the average is around 235 with a very

	A	C	A&C	A|C
pp @ 14 TeV				
V0*	0.88	0.88	0.83	0.93
T0-Plus*	0.89	0.89	0.84	0.94
R_{min}=50 mm				
T0-Plus*	0.88	0.88	0.83	0.93
R_{min}=60 mm				
T0-Plus	0.88	0.86	0.80	0.93
Detailed geometry				
R_{min}=60 mm				
Pb-Pb @ 5.5 TeV (b>13 fm; 70-100% centrality)				
T0-Plus	0.97	0.98	0.95	0.996
Detailed geometry				
R_{min}=60 mm				

Table 10.1: Efficiency comparison between the current V0 and the proposed T0-Plus. Asterisks indicates that the simulations were done using a simplified geometry.

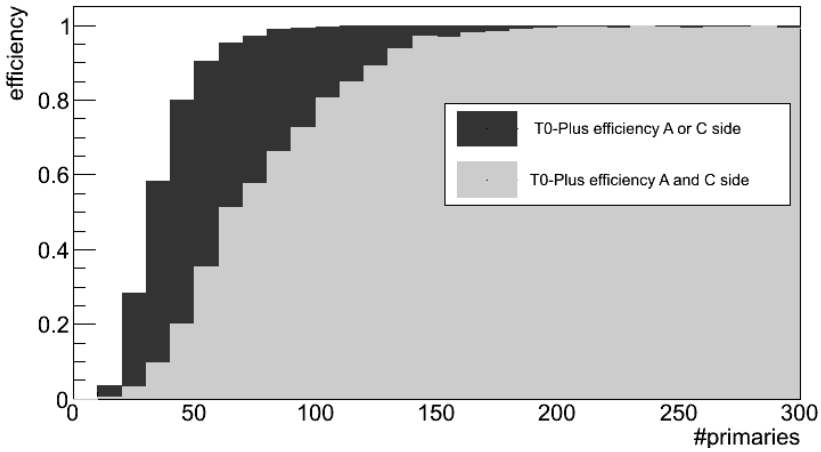


Figure 10.14: Simulated efficiency of T0-Plus detector as a function of primary particle multiplicity.

large spread around this number. Figure 10.15 shows the efficiency as a function of the impact parameter. Table 10.1 summarises the main results of the simulations. We can conclude that the performance of the T0-Plus detector is very close to the present V0 detector, as specified, and that the choice of the inner radius between 50 and 60 mm is not a critical issue.

10.6 V0-Plus detector concept

One of the advantages of the current ALICE trigger detector setup is the partial overlap in functionality between T0 and V0. It is desirable to maintain at least some of the present redundancy in the upgraded detector. A natural choice for a second detector subsystem would be V0-Plus. This would be a modified and improved V0, a plastic scintillator-based system with the frontend electronics integrated with T0-Plus and the read-out complying with the TOF standard.

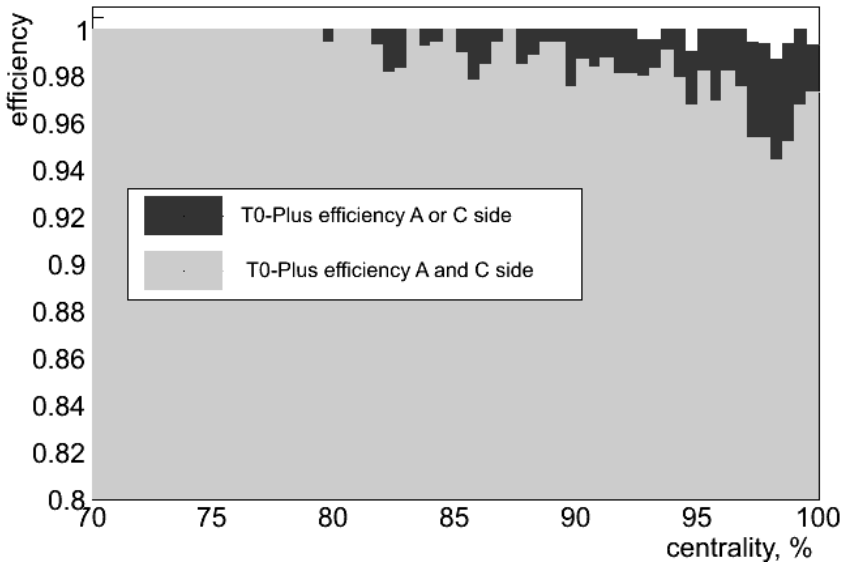


Figure 10.15: Dependence of the efficiency on the event centrality for Pb-Pb collisions at $\sqrt{s}$ = 5.5 TeV.

The existing V0 performed satisfactorily during LHC Run1, with the exception of some issues due to after-pulsing. In the following, a new V0-Plus is sketched which meets the requirements of the new run conditions, in particular the increased collision rates in pp and Pb-Pb. The severe conditions expected require a new design providing better time resolution, a larger acceptance, and much smaller after pulsing. The V0 detector assembly will be composed of a small number of independent modules which will be easy to be replaced at a minimal cost.

The new system design must continue to deliver the trigger signals provided by the current V0, including the possibility of vetoing the background due to beam-gas interactions. Because of much larger acceptance, it will both extend and complement the functionality. The final design will be developed within the Fast Interaction Trigger group to ensure the optimal functionality of the Fast Interaction Trigger detectors. Both T0 and V0 arrays are located on both sides of the interaction point [4] at a small radial distance from the beam line. A similar geometry will be used for the upgraded detectors.

V0-Plus will supply fast time signals to the CTP and, in addition, will provide an off-line multiplicity measurement and determination of the reaction plane. The design goal for V0-Plus is to improve the time resolution by an order of magnitude as compared with the current V0 and approach the level of 200 ps, while maintaining a large acceptance and high efficiency for the Minimum Bias Trigger. Better time and amplitude resolution achieved by improving the light collection from the scintillator will also improve the beam-gas background rejection capabilities of V0-Plus.

The default position of the V0-Plus arrays coincides with that of V0A and V0C. The new arrays will consist of 32 (V0C-Plus) and 32 (V0A-Plus) cells of BC408 scintillation plastic. On the A-side where the space restrictions are not critical, the light collection will be provided by fine mesh photomultiplier tubes coupled directly to the scintillator cells. On the C-side, the available volume will be restricted by the new Muon Forward Tracker (MFT).

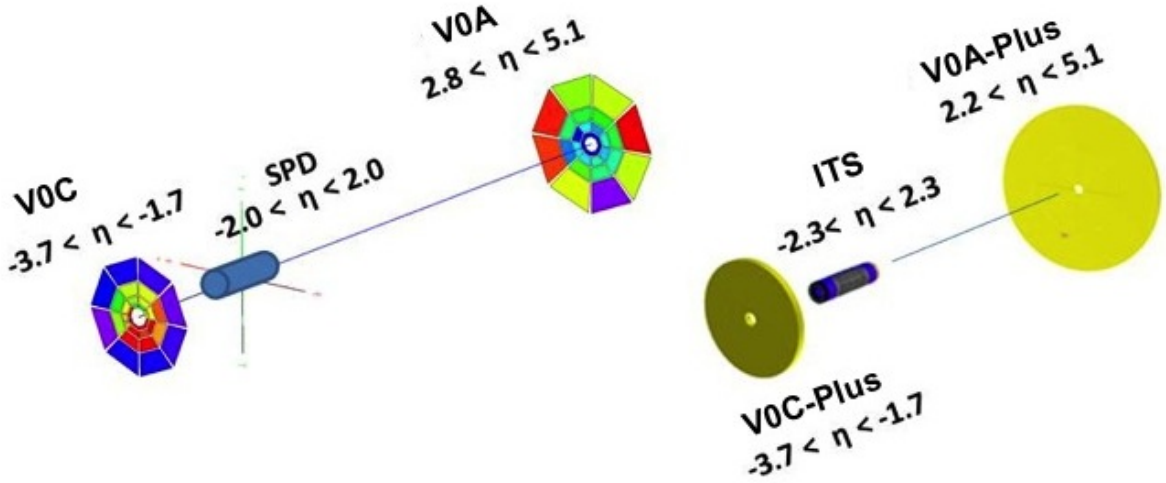


Figure 10.16: In the present system (left) there is a pseudo-rapdity gap of 0.8 units between the Silicon Pixel Detector (SPD) and V0A. Adding a ring of 0.6 units in pseudo rapidity would increase the acceptance and would even provide an overlap useful for testing and efficiency determination (right).

Ring	**V0A-Plus**		**V0C-Plus**	
	η_{max}/η_{min}	$\theta_{max}/\theta_{min}$	η_{max}/η_{min}	$\theta_{max}/\theta_{min}$
0	5.41/4.5	0.7/1.3	-3.7/-3.2	177.0/175.3
1	4.5/3.9	1.3/2.3	-3.2/-2.7	175.3/172.4
2	3.9/3.4	2.3/3.8	-2.7/-2.2	172.4/167.5
3	3.4/2.8	3.8/6.9	-2.2/-1.7	167.5/159.8
4	2.8/2.2	6.9/12.7	Additional ring only on A side	

Table 10.2: Pseudo-rapidity coverage of the new geometry. V0A-Plus may have an additional ring to cover the gap between the Inner Tracking System (ITS) and the present V0A.

V0-Plus rapidity coverage

V0A-Plus will consist of 5 rings, i.e. one more than the present V0, in order to increase the acceptance and eliminate the rapidity gap of 0.8 units between the ITS and the present V0A (Fig. 10.16). The new ITS [7] will have a wider pseudo-rapidity coverage of $-2.3 << 2.3$. Extending the coverage of V0A-Plus to $\eta = 2.2$ eliminates the gap and provides a small overlap for efficiency determination using an independent system. Such overlaps in the existing forward detectors have proven to be extremely useful.

The pseudo-rapidity coverage of V0-Plus also overlaps with the coverage of T0-Plus and the MFT, providing the ability to perform important cross checks for physics analysis. The pseudo-rapidity coverage is summarised in Tab. 10.2.

Redundancy is particularly important on the C side where access is difficult and deficiencies or failure of any of the detectors in the region should be backed up with alternative solutions. The distance to the interaction point is less than 1 m and access to the area requires a removal of the central detectors of ALICE and of the beam pipe.

Photo sensor options for V0-Plus

Both an MCP-PMT and a fine mesh PMT as possible light sensors for the upgraded V0 are considered. The former has already been described in the T0 section above. The use of the same sensor would have many advantages, as it would fully integrate the fast trigger detectors already at that level. On the other hand, the same sensor technology would increase the vulnerability of the trigger to unforeseen long-term problems with the MCP-PMT solution. If the primary goal is redundancy, one should consider the use of traditional PMTs for V0.

The R7761-70 photomultiplier from Hamamatsu [9] has been tested and will be used after LS1 at the actual V0 system. It is a fine mesh phototube with good timing properties. It has a 38 mm diameter with 27 mm diameter effective area. The spectral response of this PMT ranges from 300 nm to 650 nm, and peaks at 420 nm. With this broad range response, the WLS cookie can be avoided, thereby improving the time response of the detector. The photocathode material is bialkali and there are 19 dynode stages. It can be operated at lower voltage than the previously used 16 dynode stage PMT from Hamamatsu (R5946), reducing the after-pulsing rate for similar gains. The rise time is 2.1 ns and the transit time is 7.5 ns. The MCP from Photonis [60] PP0365G, which has a quartz window and a single anode, has been tested. It offers immunity from magnetic field, a fast response and very low time jitter.

10.7 Common front-end and read-out electronics for FIT

As discussed earlier, the T0-Plus and V0-Plus will use the same front-end and read-out electronics. The system will be based on the present T0 detector, using the upgraded TOF modules for data read-out.

Front-end electronics

FIT will use the same general scheme of front-end electronics as that used by T0 (see Fig. 10.2 and Fig. 10.3). The main new element of the front-end electronics will be the modernised amplifier. Because of the high radiation levels, it will have to be located not directly on the sensor but several meters from it. In addition to the amplifier, there will be shapers, fan-ins and discriminators to prepare the signal to be sent to the electronics racks. Functionally, the electronics sketched in Fig. 10.17 will replace that currently in the Shoe-box (see Fig. 10.2).

Read-out

Currently, T0 uses only one DRM and one TRM. As FIT will have considerably more channels, the number of TRMs must be increased. Each TOF crate has 10 slots for TRMs. Going beyond that would require additional crates and services and, as a result, considerably increase the complexity and cost of the read-out electronics. To avoid these complications, the options that would limit the read-out of FIT to one VME crate are investigated. This work is done in close collaboration with the TOF group, who is also working on increasing the VME transfer rate.

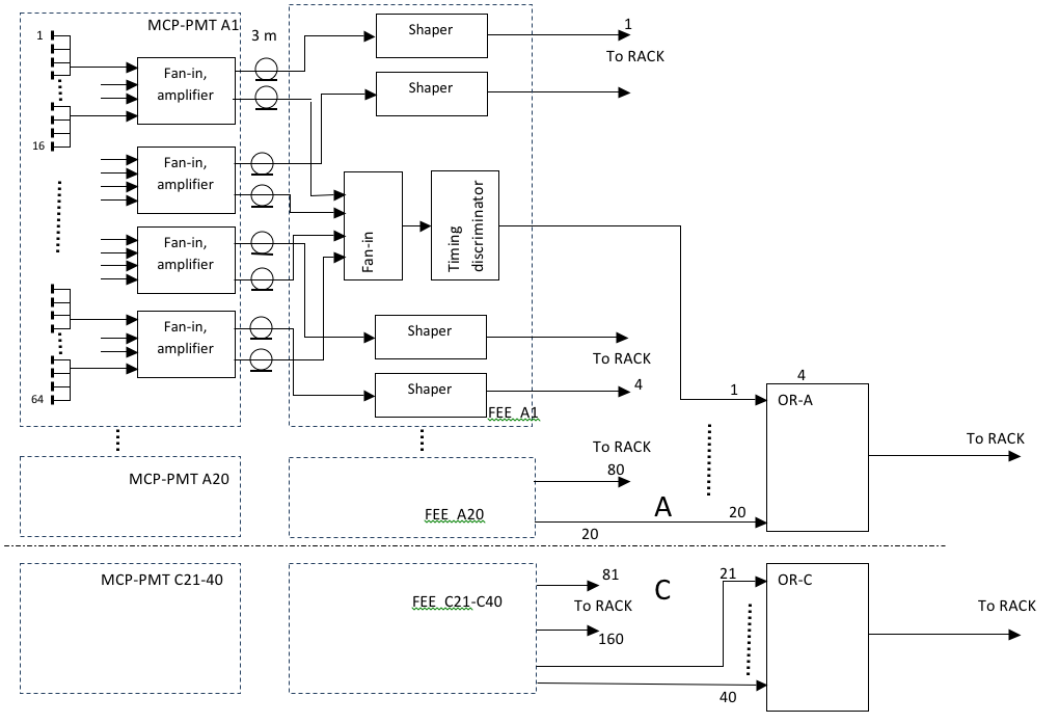


Figure 10.17: Conceptual diagram of the new first stage of the front-end electronics for the FIT. This part will replace the current electronics depicted on Fig. 10.3 by the diagram labeled shoe-box.

10.8 Schedule, funding and institutes

The most expensive items needed for the upgrade of the T0 detector are the new MCP-PMT units, currently valued at $8500 each. Including the housing, quartz etc. will result in ∼10 kCHF for each assembled detector module. Therefore, for a 2 × 20 module configuration plus 10 spares, one needs 500 kCHF. The cost of the electronics and read-out will depend on the required segmentation. Since each MCP-PMT has the anode divided into 64 independent sections, the array of 2 × 20 modules could provide up to 2560 channels. Assuming a very modest segmentation of each anode into only 4 groups gives a total of 160 channels. The cost per channel for the current T0 electronics is ∼3 kCHF. The cost estimate for the FIT detector is shown in Tab. 10.3. The involved institutes in this project are summarised in Tab. 10.4. Table 10.5 shows the FIT schedule.

	Cost [kCHF]
T0-Plus	
MCP-PMT	510
Read-out electronics	427
Services and mechanics	40
Manpower	340
T0-Plus Total	1317
V0-Plus	
Scintillation plastic & Fibers	85
Photo sensors	250
Read-out electronics	335
Services and mechanics	25
V0-Plus Total	695
FIT CORE + man power	1672 + 340
FIT Total	2012

Table 10.3: FIT cost.

Institutes
California Polytechnic State University, San Luis Obispo, USA
Centro de Investigación y de Estudios Avanzados del IPN, Mexico City, Mexico
Chicago State University, Chicago, United States
Helsinki Institute of Physics (HIP) and University of Jyväskylä, Jyväskylä, Finland
Institute for Nuclear Research / Academy of Sciences, Moscow, Russia
Instituto de Ciencias Nucleares, UNAM, Mexico City, Mexico
Moscow Engineering Physics Institute, Moscow, Russia
Niels Bohr Institute, University of Copenhagen, Copenhagen, Denmark
Pontificia Universidad Católica de Peru, Lima, Peru
Russian Research Centre Kurchatov Institute, Moscow, Russia
Universidad Autónoma de Puebla, Puebla, Mexico
Universidad Autónoma de Sinaloa, Culiácan Sinaloa, Mexico
University of Helsinki, Finland

Table 10.4: FIT institutes.

Year	Activity
2013-2016	prototyping of detector modules and electronics; in-beam tests
2017	Purchase of MCP-PMT sensors and assembly of detector modules and electronics
2018	FIT installation

Table 10.5: FIT schedule.

11 Zero Degree Calorimeter - ZDC

11.1 The present ZDC read-out system

The ZDC acquisition and trigger system has been designed with a conservative approach. Since it is located in one of the ALICE control rooms outside of the cavern, i.e. in a zone without strong radiation levels during data taking and therefore of easy access, the system uses NIM and VME electronics. At present it employs a combination of commercial and custom VME modules. The commercial modules are connected to the front-end and provide the measurement of the signal charges (CAEN V965 QDC), of the arrival time of the signals (CAEN V1290 TDC) and the measurement of their rate (CAEN V830 scalers). A custom differential discriminator has been developed for the ZDC following the idea of Refs. [70, 71] in order to provide precise triggering even in presence of low frequency noise on the baseline. The discriminated signals are combined together through standard NIM modules to provide different logical combinations that can be modified when changing colliding beam types. In the future, the combinatorial logic will be implemented in an FPGA.

Two custom modules are dedicated to the interface of the ZDC front-end with the ALICE trigger and read-out systems. The ZDC Trigger Card (ZTC) aligns the ZDC trigger signals with the LHC clock and delays them in order to satisfy the timing requirements for L1 triggers. The ZDC Read-out Card (ZRC) is dedicated to data acquisition. Upon receiving a L0 trigger, it generates a gate for the QDCs and a strobe for the TDC. At the same time, a busy signal is sent to the ALICE Local Trigger Unit (LTU) and from there to the Central Trigger Processor (CTP). Correct timing of the ZDC signals has been achieved using delay lines. Details of the timing are given in Tab. 11.1. If an L1 trigger is received in the appropriate time window, the event is read out to the ZRC buffers. Otherwise, the FEE buffers are cleared. At the reception of the L2 accept signal (L2a) the event is sent to the DAQ through the DDL link, while in case of an L2 reject signal (L2r) it is discarded. The present acquisition system is able to sustain an L2a rate of ~ 8 kHz in the ZDC. This will double after LS1 thanks to the introduction of a Multi Event Buffer (MEB). For each event, all the modules are read out. Zero suppression is present only on the V1290 TDC. The event size for Pb-Pb collisions is ~ 800 B.

The system is controlled by a VME processor that interacts with the ALICE Experimental Control System (ECS) through the SMI protocol [72]. At the same time, the processor receives some portion of the events (pushed by the ZRC) to provide calorimeter hit rate information for the luminosity monitoring. This information is made available to the experiment through the DIM protocol [73]. A detailed description of the ZDC trigger and read-out system can be found in Ref. [74].

The ZDC is operated only during Pb-Pb and p-Pb runs. In this way the aging of the PMTs and of the detector can be kept to an acceptable level. During pp runs, the ZDC is turned on for short periods to prepare for the ion running.

Phase				
ZDC signal	L0 trigger	Start (ns)	Duration (ns)	End (ns)
Collision at IP		0	0	0
Time of flight to ZDC		0	376	376
Signal formation		376	60	436
Patch cables		436	10	446
	L0 decision (LTU output)	0	975	975
Cable to CR4		446	890	1336
FIFO/Cables in CR4		1336	33	1369
	L0 cable to CR4	975	440	1415
	ZRC delay +cable	1415	257	1672
Delay lines		1369	323	1692

Table 11.1: L0 timing for the ZDC in Run1/2. We follow the formation and propagation of the ZDC signals and of the L0 trigger along the different phases. The starting time for each phase, its duration and ending time is detailed in the Table. The events are ordered according to their ending time. The delays are tuned so as to provide a gate to the ADCs that opens 1672 ns after the collision (end of row "ZRC delay +cable") i.e. 20 ns before the arrival of the analog signal of the ZDC (end of row "Delay lines").

11.2 Upgrade strategy

11.2.1 Introduction

The main target of the ALICE upgrade involving the ZDC is the improvement of the read-out performance, allowing the read-out of the detector at 100 kHz without dead time. This cannot be achieved using the current QDCs because of the fixed dead time due to the charge conversion of $\approx 10\,\mu$s per event. Consequently, the ZRC has to be redesigned. The new ZRC will be read out by the Common Read-out Unit, CRU. This simplifies the design and gives greater flexibility.

11.2.2 DAQ and trigger architecture

Data rates

In normal operation, the read-out of the ZDC will be triggered by the ALICE minimum bias signal. It would be difficult to use a trigger-less approach because the ZDC is sensitive also to the electromagnetic dissociation processes (EMD) that result in neutron or proton emission from the colliding ions. For Pb-Pb collisions at LHC energies, the cross sections are ~ 25 times larger than the hadronic cross section since they increase faster with energy and scale as the square of the ion charge. This would result in an additional 5.2 MHz event rate on the ZDC that will need to be acquired and later discarded because the other detectors are not sensitive to these events. Moreover, the V1290 TDC modules and some digitisers available on the market have a limitation to 500 kHz trigger rate. The possibility to run triggerless on events where both neutron calorimeters are hit is under investigation. In this case, the contamination from EMD events is much lower. However, there is a potential loss of hadronic events.

For calibration purposes, the system will be able to run triggerless in standalone mode. In this case, a considerable dead time is induced by the saturation of the VME bandwidth because of the EMD events. However, this is not of concern because only the ZDC data will be collected.

Front-end read-out electronics

The ZDC will replace the QDCs with digitisers with 1 GSamples/s. The modern digitisers available on the market have on-board FPGAs that allow a fast pre-processing of the data. In particular, they allow integration of the signal and provide a time-stamp of arrival times. The payload of the digitiser is therefore much reduced compared to a full read-out of all the samples. Another interesting feature is the measurement and subtraction of the baseline contribution to the integral. This feature allows the elimination of the modules that are dedicated to the baseline measurement, thereby reducing the payload. It would also be possible to implement pile-up rejection codes* if the bunch spacing is reduced below 75 ns. Moreover, data are made available without the dead time due to charge integration and conversion typical of conventional QDCs. The new modules have large read-out buffers and support read-out modes faster than BLT32, up to 2eSST. The V1290 TDC modules will also be upgraded to sustain higher transfer rates with a firmware upgrade and a small hardware modification by the factory. A payload of $\sim$ 600 B per event (with respect to the present $\sim$ 800 B) is estimated resulting therefore in 60 MB/s at 100 kHz, making the use of VME possible (using protocols 2eVME or 2eSST). A detailed breakdown of the event payload is shown in Tab. 11.2.

Test of a digitiser

During the 2013 p-Pb data taking, a test of a digitiser (CAEN V1751) in parallel to the ALICE data acquisition was made. Its main features are sampling frequency of 1 Gsample/s, 10-bit resolution, 1 Vpp dynamics and 8 channels. The signal of the common photomultiplier of the neutron calorimeter on the Pb remnant side has been sent to two channels of the V1751. In the first channel, the signal has been attenuated by 4.4 dB in order to match the dynamics of the signal with the input dynamics. In the second channel, the signal has been amplified by a factor 2 to simulate the performance of a digitiser with higher resolution ($\sim$12-bit). In this case only the events with low energy deposition are treated correctly, while for the higher amplitude signals saturation occurs. The digitiser was triggered by the start of LHC orbit and for each event a full orbit was recorded. The identification of the signal, the integration and baseline subtraction were performed in the offline analysis. An example is shown in Fig. 11.1. In the left plot, the charge of the attenuated signal is shown and the resolution of the 1n peak signal is 26 % while the resolution of the right plot for the amplified signal is 21 %, closer to the value obtained with the V965 QDCs. The contribution of the 10-bit resolution is therefore significant for the attenuated signal. We will therefore need 12-bit digitisers that are just starting to be available on the market.

*The firmware of the flash ADC should be customised to detect the presence of another collision, that is most probably electromagnetic, in the preceding bunch crossing. Since electromagnetic pile-up affects mainly the ZDC and is difficult to detect using the information of other detectors, one needs to rely only on our measurement. If another collision is present, the event could be flagged as bad or alternatively one could subtract on-the fly the pile-up contribution. As a further possibility, one could write the information about the signal shape in the data to allow a more refined subtraction during reconstruction.

		Payload							
Source	Ch.	ADC ch.	ADC B	TDC ch.	TDC[a] B	ZTC ch.	ZTC B	Scaler ch.	Scaler B
ZNA/C	5	5	40	7[b]	28			3[c]	12
ZPA/C	5	5	40	4[d]	16			3[c]	12
ZEM1/2	2	2	16	3[e]	12			3[e]	12
Trigger	4			4	16	4	8	4[f]+8[g]	48
Control	4			3	12	1		3[f]+1[g]	16
Data				338 B				+124 B	
Control words				60 B				+12 B	
Multi hit				~80 B					
CDH+packing				60 B					
Average				~540 B					

[a] Assuming a single hit per event (the multi hit contribution is accounted separately)
[b] Five towers, sum of four subtowers, common && sum
[c] Common tower, sum of four subtowers, common && sum
[d] Common tower, sum of four subtowers, common && sum, most exposed tower
[e] ZEM1, ZEM2, OR of the two
[f] V830 scaler
[g] ZTC scaler

Table 11.2: Payload of the ZDC event, detailing the contributions of the neutron (ZNA, ZNC), proton (ZPA, ZPC) and electromagnetic calorimeters (ZEM1, ZEM2) and of the trigger and control signals. The ADC, TDC and ZTC information is read out for each event while the scalers are only read out when trigger is flagged as calibration, resulting therefore in an additional payload (as indicated). The event pile-up from the preceding and following bunch crossings results in additional payload on the multi-hit TDC. This contribution has been estimated from the Pb-Pb data taking of 2011. Space for the common data header (CDH) in case it will be added by the ZRC and not by the CRU will be allocated.

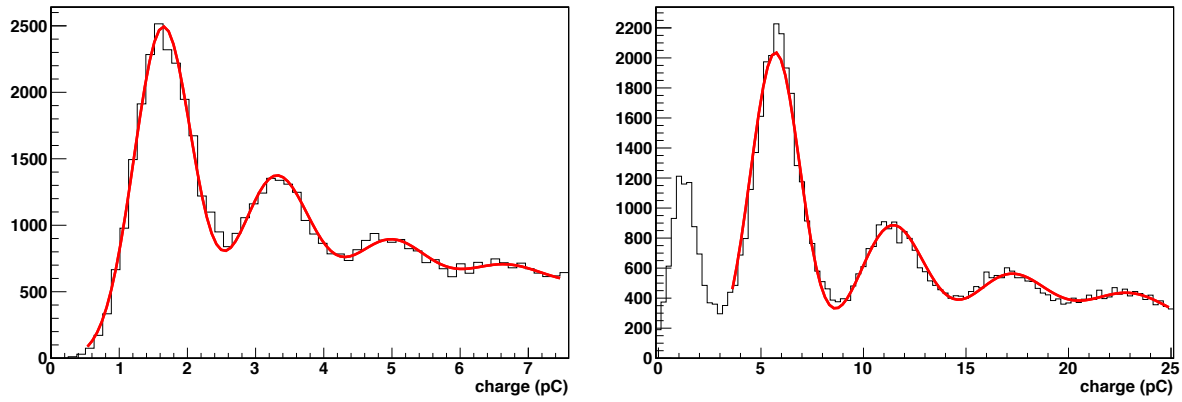


Figure 11.1: Spectra of the ZDC neutron calorimeter on the Pb-remnant side during p-Pb 2013 data taking at $\sqrt{s} = 5.02\,\text{TeV}$, obtained with a V1751 digitiser. The spectra are zoomed in the low part where the contribution of small neutron multiplicities (1n, 2n, 3n, 4n) are visible. The left figure concerns the signal attenuated by 4.4 dB, while the right figure is for the signal amplified by a factor 2. Despite that some optimization of the trigger algorithm is needed to reject noise, the spectrum for the amplified signal has better resolution.

Read-out board

The ZRC board will be upgraded to support the new trigger and DAQ framework. Its functionality will be similar to the present module: it will receive and dispatch L0 trigger and busy, will read out the front-end modules and send the data to the ALICE DAQ system via the CRU. The new board will implement faster VME cycles like VME64 or 2eSST in order to have spare bandwidth on the VME bus to allow for a future increase of the luminosity and of the trigger rate. As opposed to the present ZRC that directly receives triggers on LVDS and TTC links and sends data through DDL, the new board will interface with the ALICE Common Read-out Unit (CRU) that is being developed. This will simplify the design and make a future upgrade of the system easier. The connection with the CRU will be provided by one single bidirectional GBT connection. A scheme of the new ZRC board is shown in Fig. 11.2.

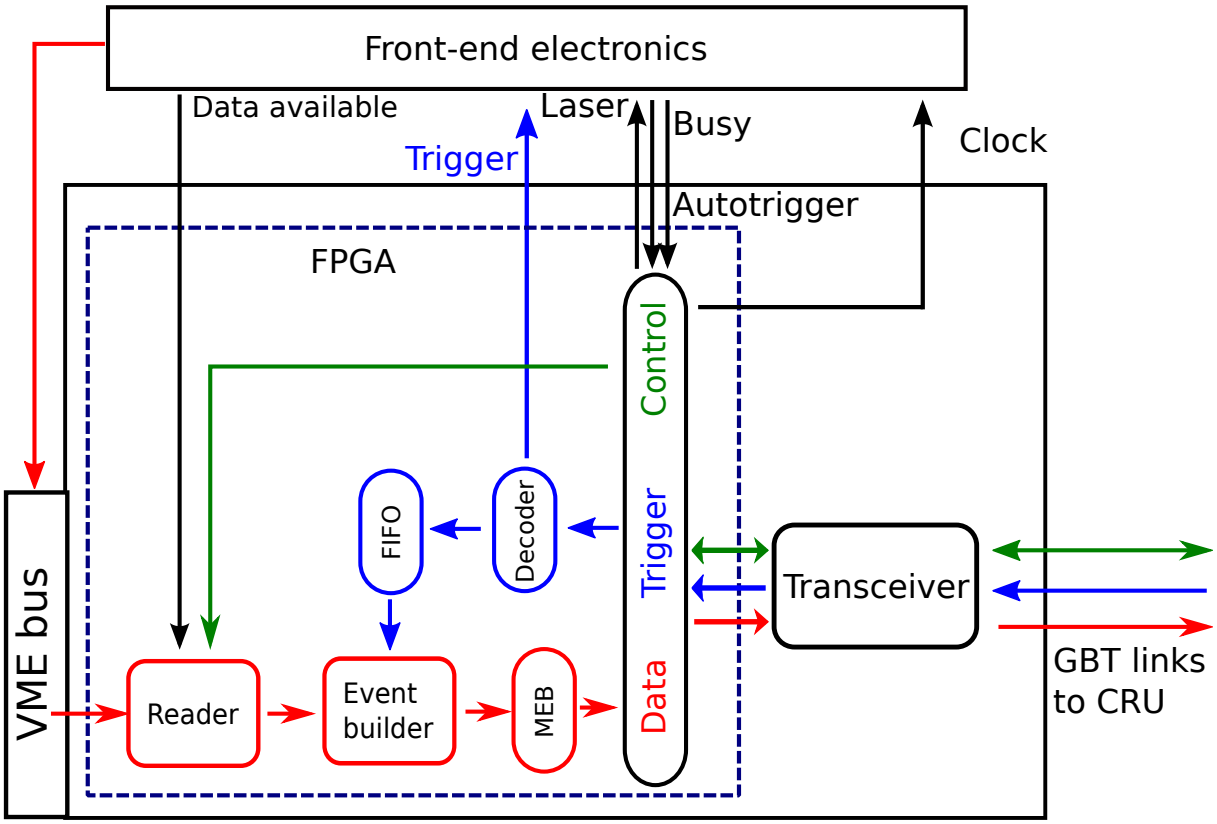


Figure 11.2: Scheme of the new ZDC read-out card.

Trigger and busy handling

The ZRC will receive the L0 trigger from the CRU and distribute it to the modules through NIM and ECL ports on the front panel. The trigger signal will be delayed using on-board delay chips in order to satisfy the timing requirements at the level of the front-end boards. Upon reception of an L0 physics trigger, an event will be acquired on the digitisers and on the TDC. When a calibration (software) trigger is received, the scaler modules will be read out in addition. The events will be transferred to the ZRC and then sent to the CRU.

In case the trigger rate is as high as to saturate the transfer capability, the buffers on the front-end modules will start to fill up and the modules will raise an “almost full” busy signal. The ZRC will receive these signals via dedicated inputs on the front panel and will OR them in a

busy that is sent to the CRU. The busy is likely to occur only when the ZDC is self-triggered for calibration.

Concerning the allowed latency of the trigger signals, the time of flight of the spectator nucleons, the signal formation time, the cable length and the delay lines have to be considered. The V1290 TDC and the digitisers employ circular memory to store temporary data that are then copied to the main buffers when a trigger is received. Since the modern digitisers have large on-board buffers, the limitation will be given by the V1290 TDC with its 256 word deep memory shared by each group of 8 channels. With conservative assumptions about the signal rates, one can accept a L0 latency up to $\sim 2\,\mu s$ at the ZDC FEE (that translates into $\sim 1.6\,\mu s$ at the CTP level) without danger of data loss.

Self-triggering operation

For calibration purposes, the ZDC has to be read out also in self-triggering mode. The calibration run modes are:

- pedestal: to measure the baseline of the signals. This is strictly not necessary since the digitiser will offer the possibility to subtract automatically the baseline, however it will be useful as a monitoring tool to check the evolution of the baseline oscillations in different run conditions.
- laser: a light pulse is sent to the photomultipliers to measure the stability of the gain.
- cosmic ray trigger: when beam is not present, pairs of scintillators are placed above and below each calorimeter to allow triggering on the passage of cosmic rays. The light output for a minimum ionising particle is ~ 1 photo electron and this allows the stability of the gain of the photo-multipliers to be checked.
- energy calibration: a minimum bias ZDC trigger signal is used to collect a significant sample of ZDC events in a short time interval. This sample is dominated by EMD events that involve the emission of a single nucleon and therefore the calibration of the detector.
- L1 calibration: the ZDC L1 trigger inputs are used to collect a sample of self-triggered events to carefully check offline the implemented trigger logic.

For this purpose, the ZRC will have NIM or ECL trigger inputs and additional trigger outputs to drive the laser pulses. Each trigger input will have a delay line to allow precise alignment with the LHC clock. Upon reception of a signal in one of the trigger inputs, if the front-end is ready and the CRU link is operational, the ZRC will dispatch the trigger signal to the front-end and forward the event data to the CRU.

In the self-triggering operation mode, depending on the beam conditions, the ZDC can saturate the VME bandwidth and therefore have dead time. Moreover, for the pedestal, laser and cosmic runs it will collect events that are completely uncorrelated to the rest of the experiment. Therefore, for the moment, this operation mode is intended for standalone operation.

Interface to CRU

The interface with the CRU will be handled by one GBT link. The maximum theoretical VME bandwidth (320 MB/s i.e. 2.56 Gbit/s) can be read by one GBT link.

ZDC triggers

The ZDC provides an L0 trigger given by the coincidence of the signals of the central towers of ZNA and ZNC. This reduces the background from electromagnetic dissociation processes that is present in minimum bias triggers. This selection is routinely used in data analysis and, in this way, will be made available at L0 trigger level. The system will be based on two fast cables (one of which is already in place) connecting directly ZNA and ZNC with a trigger logic that will be placed close to the CTP.

The ZDC L1 trigger ouput is given by logical combinations of the signals of the 6 calorimeters. For each neutron and proton calorimeter, the information has a redundancy that allows elimination of the photomultiplier noise. In the present implementation, the L1 trigger logics are synchronised by the ZTC and then forwarded to the CTP using LVDS cables. The minimum latency for the ZDC L1 triggers (at the CTP input) is around 2.0 - 2.2 μs depending on the trigger logic. The use of the present approach to dispatch the L1 trigger signals will be continued.

11.3 Schedule, funding and institutes

Tables 11.3 and 11.4 show the schedule and funding of the project. The institutes shown in Tab. 11.5 will participate in the upgrade.

2014
Purchase and test in laboratory of a 12-bit ADC (R&D⇒15 kEUR)
Definition of the architecture of the new ZDC Read-out Card
Firmware development on “evaluation board” (R&D⇒5 kEUR)
2015-2016
Firmware development on “evaluation board”
Design and construction of the ZRC prototype (R&D⇒30 kEUR)
2017-2018
Purchase of 12-bit, 1GSample/s flash ADCs (70 kEUR),
rough estimate assuming that the price will be half of the actual one)
Refinement of the firmware on the ZRC prototype
Test of the ZDC read-out card prototype
Design and construction of two final ZDC Read-out Cards (30 kEUR)
V1290 TDC firmware upgrade and hardware modification to allow for 2eSST cycles (5 kEUR)

Table 11.3: ZDC schedule

2014	20 kEUR for R&D
2015-2016	30 kEUR for R&D
2017-2018	105 kEUR for the upgrade
Total	155 kEUR / 194 kCHF

Table 11.4: ZDC funding.

Institutes
Sezione INFN and Dipartimento di Fisica dell'Università, Turin, Italy
Sezione INFN and Dipartimento di Fisica dell'Università, Cagliari,Italy
Gruppo Collegato INFN and Dipartimento di Scienze e Innovazione Tecnologica dell'Università del Piemonte Orientale, Alessandria, Italy

Table 11.5: ZDC Institutes.

12 Electro Magnetic Calorimeter - EMC

12.1 The EMCal detector

The ALICE EMCal [75] is a shashlik-type sampling calorimeter that consists of ten full size super-modules (SMs) and two 1/3-size SMs, providing 107 degrees of azimuthal coverage, already installed and operated in the ALICE experiment. The EMCal coverage will be extended with six 2/3-size and two 1/3-size EMCal SMs to be installed during the 2013-2014 long shutdown of the LHC (LS1) to provide an additional 67 degrees of azimuthal coverage. A full size SM consists of 1,152 read-out towers. An individual EMCal tower is read out with an avalanche photodiode and preamplifier mounted on the tower. The preamplifier signal is split into energy and trigger shaper channels on the Front End Electronics (FEE) [76] boards. The energy shaper signals are sampled at 10 MHz with 10-bit resolution using the ALTRO chips [8] designed for the ALICE TPC (Time Projection Chamber) [77]. Prior to digitisation, each energy signal is split into a High Gain (HG) and Low Gain (LG) channel, each shaped separately, with a gain ratio of 16 to provide an effective dynamic range of 14 bit. Each FEE board provides read-out of 32 towers (HG and LG).

The trigger signals of 2×2 towers are summed and transmitted to a Trigger Region Unit (TRU) module [78] where the 2×2 tower sums are digitised and processed in an FPGA [79]. The local high energy shower trigger decisions from each TRU are transmitted to an EMCal Summary Trigger Unit (STU) where they are ORed together to form the EMCal L0 trigger. The trigger primitive data from all TRUs are transmitted to the STU upon receipt of the ALICE L0 trigger decision where the EMCal L1 single shower and jet trigger algorithms are performed. With respect to the read-out system, the TRU may optionally include the trigger primitive data in the data stream, using the same format as the FEE boards. Each full EMCal SM requires 3 TRUs and 37 FEE boards, where one FEE board is used to read out reference channels of the EMCal LED-based monitoring system.

The EMCal read-out has been upgraded during LS1 to provide more than an order of magnitude decrease in the read-out time per event, bringing the EMCal close to the ALICE post-LS2 goal of 50 kHz read-out for minimum bias Pb-Pb collisions. This was achieved with a modification of the EMCal read-out architecture using newly developed read-out concentrator modules and minor modification of the existing FEE boards, and no modification of the TRU boards or trigger system.

12.2 The EMCal read-out system

12.2.1 Point to point links and SRU

In the read-out system used before LS1, the read-out of 640 ALTRO channels within 10 FEE boards on a single GTL bus took place sequentially, resulting in a minimum read-out time of about 270 μs for EMCal. After the replacement of the GTL bus with point-to-point links between

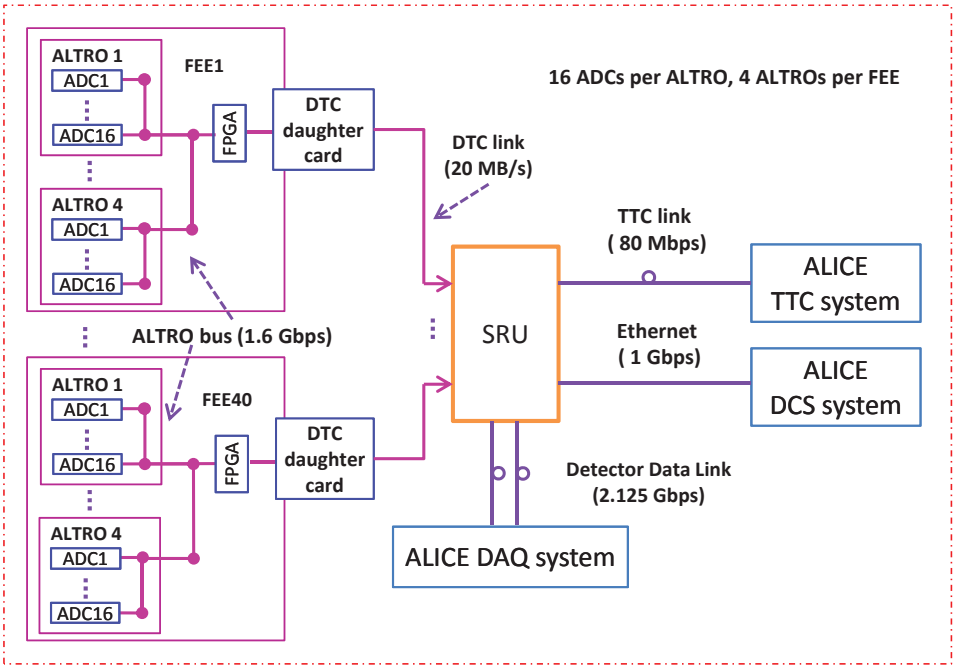


Figure 12.1: The topology of the SRU-based point-to-point read-out system.

the FEE boards and the read-out concentrator, the FEE read-out time is reduced by reading out all of the FEE boards concurrently [80]. This solution is based on the Scalable Read-out Unit (SRU) developed in collaboration with the Scalable Read-out System project [81] of CERN RD51. The SRU interconnects with each FEE board through a custom daughter card which was designed for the EMCal FEE board. It provides interface compatibility between the SRU and the existing EMCal FEE board to provide the Data, Trigger, Clock, and Control (DTC) links. The DTC daughter card mainly consists of an RJ45 port, an LVDS driver, and a power switching circuit. It mounts on the FEE board by making use of existing test-point holes into which pins and sockets have been inserted, allowing the DTC daughter card to be plugged onto the FEE without soldering.

In order to retain compatibility with the existing ALICE online system and the off-line decoding software, and since the bandwidth of the ALICE DAQ system is not a limiting factor for the EMCal read-out (see Sec. 12.2.3), the EMCal read-out partition organisation and its interfaces to the ALICE online system are unchanged, as illustrated in Fig. 12.1. Each SRU provides the two read-out partitions of a full size EMCal SM. As described in [82], the SRU board integrates a TTCrx (LHC Trigger, Timing, and Control receiver) [83] which can receive trigger and timing information from the ALICE Trigger system. It also has three SFP+ ports directly connected to the FPGA's high speed serial transceivers for serial data transport at up to 5 Gbps. One additional SFP+ port provides a 10 GbE link. For the EMCal application, one of these transceivers is used for the Ethernet connection to the ALICE DCS system, the other two transceivers are used for the two DDL links to the ALICE DAQ system. The functionalities of the DCS and SIU boards in the previous system are implemented in the FPGA firmware of the SRU.

Each SRU has 40 point-to-point links for the 40 (37 FEE + 3 TRU) boards of the two read-out partitions of a full size EMCal SM. Event data, triggers, clock, and commands are transmitted over the DTC link between the SRU and each FEE board. The maximum bandwidth of a DTC link on the SRU is 2 Gbps. In the EMCal application, the bandwidth of the DTC link is conservatively limited to 20 MB/s due to the hardware capability of the rather outdated FEE

	pp	Min. Bias Pb-Pb	Central Pb-Pb	Pedestal
N_{event}(Bytes)	1000	2500	5000	35900
N_{ch}	80	220	420	1152

Table 12.1: The measured average size in bytes (N_{event}) of various types of events, and the associated number of hit channels (N_{ch}), per read-out partition of the EMCal detector. The number of hit channels is $N_{ch} \approx (N_{event} - 68) \div 12$, where 68 is the number of bytes of the event header and trailer; 12 is the minimum number of data bytes per hit channel.

FPGA (Altera ACEX 1K Family EP1k100QC208-3) and because it is sufficient to ensure that the DTC link does not limit the EMCal data throughput (see Sec. 12.2.3).

12.2.2 Suppression of low gain read-out

Each EMCal tower energy signal is split into HG and LG channel, and shaped separately with a gain ratio of 16. The LG channel data is used in the offline analysis only when the associated HG channel has saturated. The concept of the LG read-out suppression algorithm is to check the HG signals in real time in the FEE FPGA and then omit the ALTRO read-out of the associated LG channel if the HG signal is not saturated. For low energy signals, the HG channel information is sufficient. The EMCal offline analysis experience shows that it is very rare that the LG channels are needed. Therefore, the LG suppression read-out algorithm can save read-out time by eliminating entirely the read-out of nearly half of the read-out channels.

12.2.3 Implementation and test results

The above solutions have been implemented for the EMCal read-out using the SRU of the CERN RD51 project, the EMCal specific DTC adapter card, and custom FPGA firmware for the FEE and SRU for the EMCal application.

Table 12.1 lists the measured average EMCal event sizes and the estimated maximum number of occupied channels in pp and Pb-Pb collisions per read-out partition. The average size of the EMCal physics events are typically less than 15 % of the N_{max} and less than 20 % of channels have hits in minimum bias Pb-Pb collisions.

The estimated times for each of the steps in the EMCal read-out as a function of the data volume are shown in Fig. 12.2. It is seen that the ALTRO read-out time ($t_{ALTRO_32} = \sim 19.3\ \mu$s) limits the read-out rate to 42 kHz for the anticipated EMCal event sizes (see Tab. 12.1). Further improvement in the EMCal read-out speed would require redesign and replacement of the EMCal FEE, at significant cost and effort. For event sizes larger than 3.6 kBytes, the transmit times over the existing DDL links, t_{DDL}, will limit the maximum event read-out rate (see Fig. 12.2). For the upgrade, it is therefore planned to use DDL2 links (5 Gb/s) with a new version of the SRU firmware. If necessary, the DDL3 could also be implemented using the available 10 GbE link (shown as solid circles).

A plug-in DTC daughter card has been designed to preserve the compatibility with the existing EMCal hardware. During LS1, the DTC daughter cards have been mounted on all of the FEE boards and the SRU read-out has been implemented and tested on all of the installed EMCal SMs. The additional EMCal SMs being installed during LS1 will be commissioned with the SRU read-out.

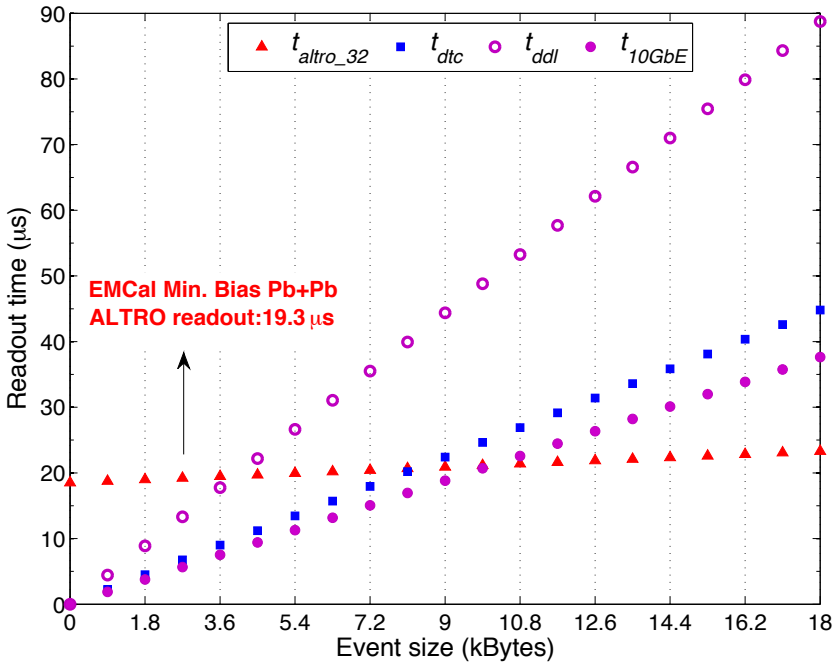


Figure 12.2: The correlation between the read-out time and the event size for the various read-out steps as discussed in the text.

The Low Gain read-out suppression algorithm ALTRO read-out function and the custom DTC protocol have been implemented through a FEE (and TRU) FPGA firmware upgrade. The function of the ALICE Detector Control System and DAQ Data Link boards of the previous read-out system have been implemented in the FPGA firmware of the EMCal SRU to provide full compatibility with the present ALICE online system.

Full read-out chain tests of the new system demonstrate a read-out time of 21.4 μs for EMCal event sizes expected for minimum bias Pb-Pb collisions, which may be reduced with further fine-tuning of the firmware. While this is more than an order of magnitude improvement over the previous read-out system, it is ultimately limited by the minimal read-out time of the ALTRO chips (19.3 μs) on the FEE boards. The new SRU-based read-out system has already been installed on the EMCal during LS1. It nearly attains the ALICE goal for the period following the 2018 shutdown to be able to record data at the anticipated 50 kHz minimum bias Pb-Pb interaction rate. The importance of multi-event buffering to keep up with the full incoming (non-uniform) event rate is shown in Fig. 12.3. With the SRU read-out, the EMCal can be read out either upon the receipt of the ALICE minimum bias trigger, up to almost 50 kHz, or upon rare triggers, such as the high energy shower or jet triggers provided by EMCal, which remain available unchanged with the new EMCal read-out.

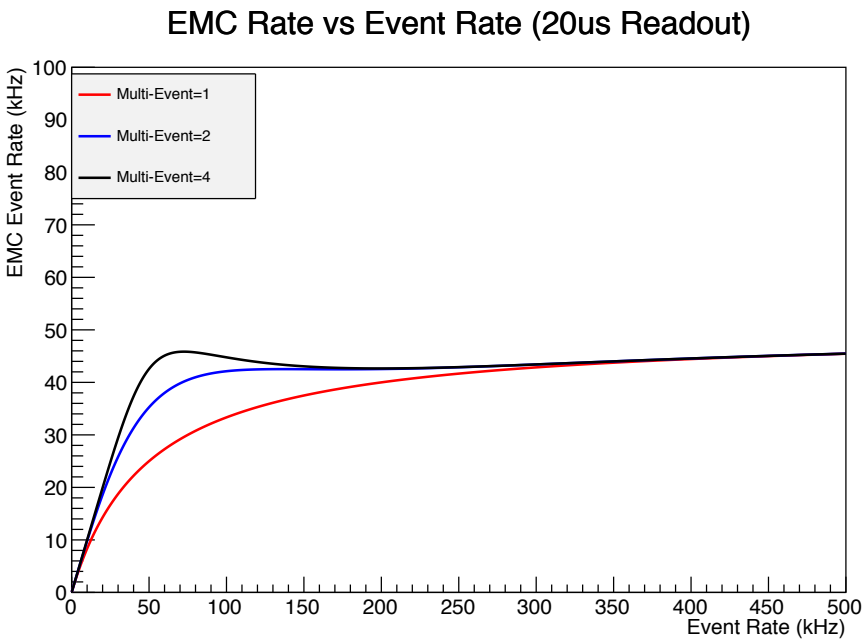


Figure 12.3: EMCal Event rate vs Event rate for different Multi-Event Buffering values.

13 Photon Spectrometer - PHO

13.1 Overview

The photon spectrometer PHO is designed to detect, identify and measure with high resolution the 4-momenta of photons. Photon studies in heavy ion collisions require from the detector a high discrimination power between photons and any other kind of particles, charged and neutral hadrons or electrons.

After LS1, PHO will have four modules, three with a full population of $56 \times 64 = 3584$ $PbWO_4$ crystals, and a fourth module with ≈ 1750 crystals. The PHO acceptance in pseudorapidity is $|\eta| < 0.13$ and each module covers 17.8° in azimuth angle.

The $PbWO_4$ crystal is 18 cm long with a squared cross-section of 22×22 mm^2. It provides 20 units of radiation length ($X_0 = 0.89$ cm). Its cross section is chosen to be comparable with the Molière radius of $PbWO_4$, $r_M = 20$ mm. The scintillation light, in the visible near UV-wavelength range, is read out by a 5×5mm^2 avalanche photo-diode (APD) integrated with a low-noise pre-amplifier. The calorimeter is operated at low temperature, -25°C, stabilised to $\pm$ 0.3°C. This operation mode on one hand enhances the scintillation light output by a threefold factor and provides the required high and constant energy resolution even for the less energetic photons. On the other hand, it keeps the noise of the APD low enough to provide a high signal to noise ratio.

The PHO read-out electronics resembles very closely those from EMCal. In fact, the EMCal FE boards were originally derived from PHO. The basic unit in the read-out chain is a FEE card (FEC) that processes and digitises data from 32 crystals. The electronics chain for a crystal comprises the avalanche photo diode (APD), a charged sensitive preamplifier (CSP) and an analog shaper with a band-pass filter and amplifier. The shaper delivers two semi-Gaussian energy signals with peaking time 2 μs, one with low gain (LG) and one with high ($\times$16) gain (HG). In addition, a short energy pulse with peaking time ≈ 100 ns is generated for the Trigger Region Unit (TRU). The LG and HG energy signals are digitised in four ALTRO 16-channels 10-bit ADCs, giving a 14-bit dynamic range up to 100 GeV. The 32 short pulses are analog summed 2×2 to eight signals and transmitted to the TRU.

A Read Out Branch (ROB) comprises 14 FECs and one TRU. The PHO module with 3584 crystals includes eight ROBs with a total of 112 FECs and 8 TRUs. The module is read out by four Read-out Controller Units (RCUs), each RCU controls two ROBs. Originally, the RCU was developed for the TPC detector. The FECs and TRU of a ROB are interconnected to one of the two RCU ports by a GTL cable bus. The read-out over a single GTL bus takes place sequentially.

The TRU delivers L0 triggers by searching for energy clusters in a ROB mapped to a 14×8 matrix (14 FECs $\times$ 8 signals). The PHO TRU digitises the quad analog sums in 20 MHz ADCs. A parallel search over all 112 of the 4×4 windows are carried out by the the FPGA firmware. The L0 energy threshold is programmable. The trigger outputs from all TRUs are ORed in a Trigger OR (TOR) device. The TOR can also be programmed to deliver L1.

Event type	pp	Pb-Pb min.bias	Pb-Pb central	pedestal
Event size, kB	1.2	8	25	160
N_{hits}	8	70	220	1792

Table 13.1: Event size and the number of hits per events in one PHO partition in different types of events during Run1.

The PHO electronics, with the exception of the read-out units, are contained inside a gas tight volume. The FEC and TRU boards are mounted inside water cooled copper boxes. To prevent condensation of humidity inside the electronics compartment, the volume is filled with nitrogen. The RCUs are mounted on the bottom shield of the module.

The average event size and the number of hits per event for pp, minimum bias Pb-Pb and central Pb-Pb collisions, as well as for pedestal runs without zero suppression, were obtained from data taken during Run1. These values for one read-out partition and the maximum of 64 time samples are collected in the Tab. 13.1. Note that data of pedestal runs contains all 64 time samples in all high- and low-gain channels, while in physics runs with zero suppression the high-gain channels dominate.

13.2 The PHO read-out system

The target for the upgrade is a PHO read-out time of ≈ 20 μs to match a 50 kHz interaction rate in Pb-Pb collisions. This requires a point-to-point read-out topology such that all FECs can be read out in parallel. PHO has therefore adopted the SRU DTC point-to-point links installed for EMCal and DCal, as described in the previous chapter. In [84] EMCal quotes a read-out time of 21.4 μs measured for event sizes expected for minimum bias Pb-Pb collisions. However, the data volume per ALTRO channel for PHO is currently 64 time samples at 10 MHz, compared with 15 time samples for EMCal.

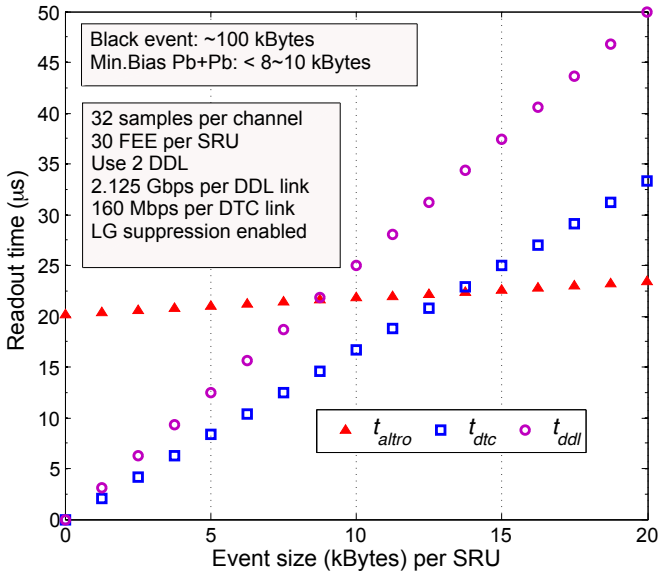


Figure 13.1: Calculated read-out times for PHO SRU configuration. Up to 9 kB/SRU the time is dominated by the ALTRO protocol. Note that the individual contributions from ALTRO, DTC and DDL are not additive.

For the SRU system, the effective read-out time for a given event size is determined by the largest transaction delay from i) ALTRO bus, ii) DTC link between FEC and SRU, and iii) the detector data link (DDL) between SRU and the DAQ system. This is illustrated in Fig. 13.1. The read-out time can be minimised by 1) reducing the number of time bins, 2) limiting the data volume from SRU to DAQ by using fewer DTC links and 3) using two DDLs instead of one.

Calculations [85] show that the minimum ALTRO read-out time with 64 time bins is around 25 μs. This value is reduced to $\approx$ 20 μs and $\approx$ 18 μs for 32 and 16 time bins, respectively. However, the current 64 time samples can safely be reduced to 32 because it is sufficient to sample the first $\approx$ 3.2 μs of the pulse, which will cover both its rising edge and the maximum amplitude.

To switch to 16 time samples would require a shorter pulse from the analog shaper by changing the shaping time constant from 2 μs to 1 μs. This will have a negligible effect on the energy resolution. However, it would require a major intervention by changing a very large number of capacitors on the FECs.

Shortening the pulse length will reduce the probability of pileup in a channel. However, as shown in [86], the mean time between hits in a cell for an average Pb-Pb event is $\approx$ 400 μs. With proper timing calibration, all cells can be aligned within 3 ns. It will therefore not be a problem to identify data from BCs with 25 ns spacing. Pileup effects can therefore be neglected also with the current pulse length.

The event size after the change to 32 time samples will be roughly half of that shown in Tab. 13.1.

The performance of the chosen topology is shown in Fig. 13.1, with 4 SRUs per PHO module and using 30 out of the 40 DTC SRU links. The SRU and FEC firmware are optimised for 32 time samples per channel with Low Gain read-out suppression algorithm [85]. For an event size of 8 kB/SRU, corresponding to $\approx$ 110 kB for the full PHO detector, the theoretical read-out time is 22 μs giving a maximum rate of around 42 kHz. The read-out topology of one PHO module is schematically shown in Fig. 13.2.

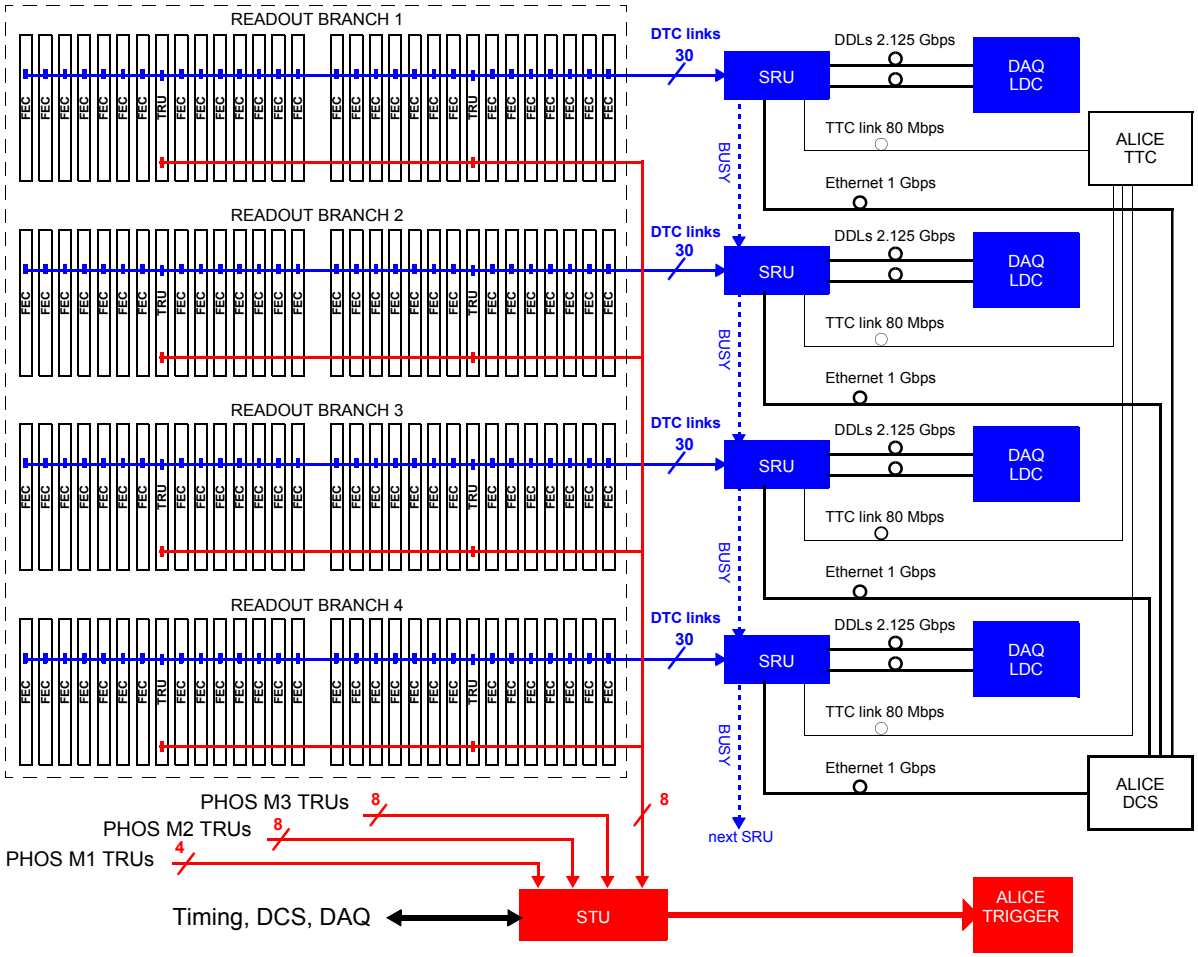


Figure 13.2: Read-out and trigger topology of the PHO modules M2, M3 and M4. The dashed rectangle contains the FE electronics inside the module.

14 High Momentum Particle Identification Detector - HMP

14.1 Introduction

The ALICE High Momentum Particle Identification Detector (HMP) performs charged particle identification by means of the measurement of the Cherenkov angle, exploiting the momentum information provided by the tracking devices. It consists of seven identical proximity-focusing Ring Imaging Cherenkov (RICH) counters. The HMP is able to provide 3 sigma separation for π/K in the momentum range 1 GeV/c < p < 3 GeV/c and in the range 1.5 GeV/c < p < 5 GeV/c for K/p that, at 2 sigma, can be pushed up to 6 GeV/c. The radiator used is C_6F_{14} (n = 1.2989 @ 175 nm, $\beta_{th} = 0.77$), 15 mm thick. The photon detection is provided by multiwire chambers equipped with pad-segmented CsI photo-cathodes (CsI Q.E. $\approx$ 25% @ 175 nm, pads size 0.8x0.84 cm^2). The amplification gas is CH4 at atmospheric pressure, the anode-cathode gap is 2 mm and the operational voltage is 2050 V (gain $\approx 4\times10^4$). The 42 photo-cathodes are segmented in 3840 pads each with individual analogue read-out. The front-end electronics (FEE) and read-out (RO) are based on GASSIPLEX and DILOGIC chips, respectively, both developed within the HMP project. The noise level is 1 ADC channel (1000 e-) whereas a single photon signal amplitude is of the order of 30 ADC channels on average. Less than 200 out of 161280 channels are dead or noisy. A detailed description of the detector can be found in [87]. HMP has successfully collected pp, p-Pb and Pb-Pb data during the LHC operation period Run1 and it has contributed as expected to the physics program, measuring charged hadron spectra and ratios. The same conditions of operation are planned for the HMP during the Run2 period, when the LHC will increase the collision energy.

After the ALICE upgrade, the HMP will be able to exploit its maximum event read-out rate of 2.5 kHz in central Pb-Pb collisions, with an increasing factor of 4 with respect to the Run1 and Run2 periods, when the drift time and the TPC read-out rate imposed lower rates. No CsI Q.E. degradation is expected for the upgrade operation since the estimated charge dose of 0.16 mC/cm^2 will be less than 0.2 mC/cm^2, which is the threshold considered where possible ageing effects of CsI could be observed [88, 89]. With the increase of the read-out rate, the HMP will have event statistics higher with respect to Run1 and Run2. The HMP read-out rate of 2.5 kHz will result in a sample of more than 10^9 minimum-bias Pb-Pb events per month with an interaction rate of 50 kHz and delivered luminosity of about 3 nb^{-1} [1]). With this sample, the production of pions, kaons and protons can be measured with a statistical uncertainty on the percent level up to p_T of 3 - 4 GeV/c for pions and kaons and of 6 GeV/c for protons.

14.2 Implementation architecture

The full exploitation of the HMP read-out rate at 2.5 kHz for central Pb-Pb collisions ensures the PID for the defined upgrade physics program. No upgrade of the electronics is planned. The

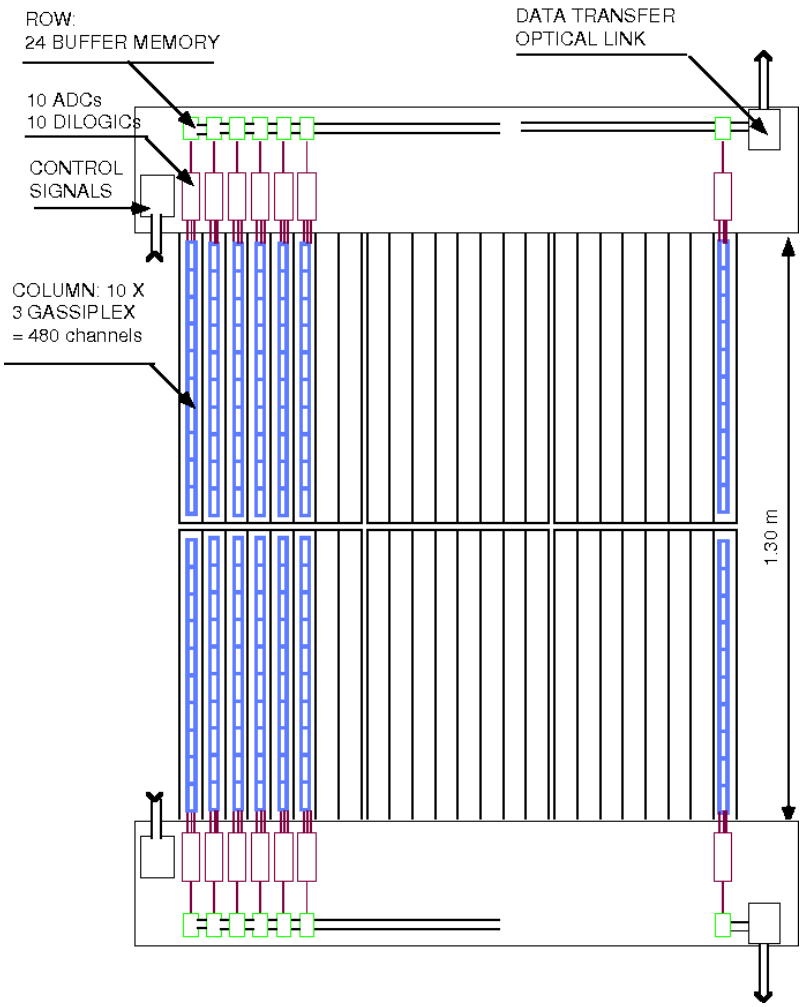


Figure 14.1: Schematics of the implementation of the FE and read-out electronics on one HMP module.

detector can be easily integrated in the ALICE read-out architecture, as the upgraded ALICE system provides backward compatibility.

Each HMP module is read out by two optical links, one for each module side (Fig. 14.1). On each side the electronics is organised in 24 columns, with 10 front-end Gassiplex cards per column. Each Gassiplex card is equipped with 3 Gassiplex chips and the DILOGIC chip for a total of 48 channels and connected to a Multi-Chip-Module that provides channel multiplexing, ADC conversion and zero suppression. Upon L0 arrival, the 24 columns are read out in parallel and the content is transferred to the column memory buffers. The L0 latency that optimises the peaking time is 1.2 μs.

Due to the relatively smooth bell shape of the shaping preamplifier signal, an increase of latency of 0.3 μs would result in a signal loss of 22 % with a reduction of the single photoelectron detection efficiency of 3 %. This result comes from the good ratio S/N $\approx$ 30 and a digitalisation threshold set at 4 ADC channels. Applying such efficiency reduction to the present experimental data set, shows no evident degradation of Cherenkov angle resolution [90]. Therefore, 1.5 μs latency for L0 should not have a relevant impact on the HMP PID performance.

Upon the trigger signal, the 24 columns are sequentially read out and the data are sent via DDL1 to the DAQ. Extrapolating the results from Run1 in central Pb-Pb collisions at 5.5 TeV

$\sqrt{s_{\mathrm{NN}}}$ at the full read-out rate, 56 MB/s data rate is expected. The trigger signal management is ensured by cables and the standard TTCrx card, connected to the LTU via optical fibres. The full detector operation is ensured by 14 DDL1 optical links, 14 RORC1 cards, 14 TTCrx cards, 14 L0 cables and 14 busy cables. For the debugging of trigger timing, one TTCit board is planned to be added. In conclusion, the HMP can take data in the upgraded system, maintaining its read-out and trigger electronics unchanged.

15 ALICE Cosmic Ray Detector - ACO

The ALICE Cosmic Ray Detector (ACO) produces an L0 input trigger signal to the ALICE CTP and provides precise information on cosmic rays.

ACO consist of an array of scintillator plastic counters placed on the top sides of the ALICE magnet. The current layout of the cosmic trigger on the top face of the ALICE magnet consists of 60 scintillator modules arranged in a doublet configuration. Each doublet consists of two superimposed scintillator counters and contains one front-end electronics (FEE). The signal of each of the two scintillators contained in one ACO module is applied to a leading edge discriminator and the FEE provides the coincidence signal of one ACO module from the two signals coming from the two scintillators. All the modules are connected to the main electronics card which processes the information to generate a single muon and multi-muon trigger signals. The ACO main card receives the 120 differential signals coming from the 60 FEE cards. These signals are translated to CMOS levels and sent an ALTERA FPGA. The Cosmic trigger signal is generated by combinational logic. The TTS interface is a TTC protocol. ACO is read out via a DDL1 interface (see Fig. 15.1).

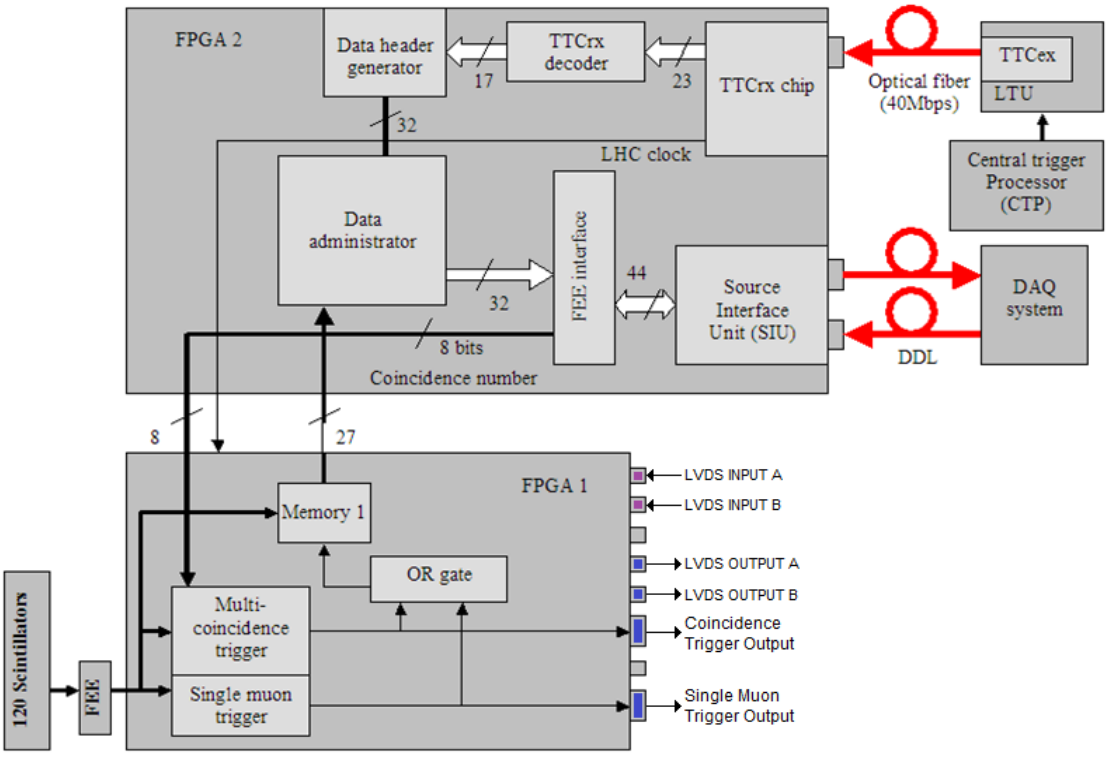


Figure 15.1: Block diagram of the ACO main card.

16 Summary of milestones and resources

16.1 Upgrade Organisation

This paragraph summarizes the organisation of the upgrade consisting of the following ALICE sub-projects. After LS2 the inner tracking system (ITS) is completely renewed. The muon forward tracker (MFT) will be added as new silicon detector. For the time projection chamber (TPC) the read-out chambers and the entire electronics system is replaced. The muon chamber system (MCH) and the muon identifier detector (MID) will keep the detectors but replace the entire read-out electronics chain. The ALICE fast interaction trigger system (FIT) will replace the present assembly of T0/V0/FMD. The zero degree calorimeter (ZDC) will change the front-end electronics and data concentrator electronics. For the time-of-flight detector (TOF) and the transition radiation detector (TRD) the detector and the front-end electronics will remain in place, but the off-detector electronics acting as data concentrator will be upgraded. The online and offline system (O^2) will be fully replaced. The electromagnetic calorimeter (EMC), the photon spectrometer (PHO) and the high multiplicity particle identification detector (HMP) have already been upgraded.

In this document the ALICE upgrade trigger and electronics read-out strategy is described together with the upgrade of the MCH, MID, FIT, TOF and TRD. The upgrade of the ITS, MFT, TPC and O^2 are described in separate technical design reports.

The upgrade of the ALICE trigger and read-out system is coordinated by ALICE system upgrade coordination. The ALICE sub-detectors are organised as individual projects with their own organisation. Common items and cross project dependencies are treated by the system upgrade coordination. Fig 16.1 shows the system upgrade programme structure, a summary of milestones and available man power. Interfaces between common developments, such as the CRU, CTP, TTS, SAMPA or O^2 are defined in collaboration between the developing projects and the user-projects during the initial project phase, allowing the user-projects to continue the development and construction of the system independently. The definition phase is coordinated and closely followed by the system upgrade coordination.

16.2 Schedule

Figures 16.2 to 16.5 show an overview of the sub-project time scales and available man power. Figure 16.7 to 16.13 show the schedule and milestones of the upgrade programme in form of a Gantt chart by sub-project. The individual sub-projects are operating independently. Cross-project developments and common items used by several sub-projects need to be available in time to proceed with sub-detector system design, construction and commissioning. Section 16.2.1 explains how these inter-dependencies are resolved.

After the development phase for a specific item, the schedule considers a prototype phase and a second iteration, the pre-series phase, to correct for errors before production. Considering

that many items to be produced are state-of-the-art products and do not require a research phase where time scales are difficult to estimate, this approach introduces contingency in the planning, as the pre-series phase might not be needed at all. The following paragraphs highlight the development and construction phases:

Development Performance is validated in development test stands. One example is the development of the MCH/TPC/SAMPA test stand which qualifies the SAMPA performance interfaced to the detector chambers and the interface to the GBTx ASIC.

Prototype The development of a prototype takes into account the final electrical and mechanical specifications. Prototype system tests validate all interfaces and performance emulating realistic environments in detail. In this phase common components are emulated.

Pre-series The prototype design is optimised and a small number of items is produced. The pre-series tests involve pre-series common components, already identical in performance to the final components.

Production The full production quantity is produced and validated in system tests involving final common components.

The duration of the individual tasks has been scheduled with margin compared to the shortest practical execution time. Nevertheless, the Gantt chart shows comfortable margin for the individual sub-project developments until the installation date. This can be explained by the fact that for most tasks no research is needed and the design and construction can start immediately.

16.2.1 Common items

The individual sub-detector projects are operating independently. Common items serve several user-projects and need to be available in time to proceed with sub-detector system design, construction and commissioning. The following paragraphs outline this approach in more detail. The delivery of the common items is adapted to the user-project needs.

For each of the common items, CTP, CRU, SAMPA, GBT and versatile link optical components, a three-phase scenario is planned where the user-projects are supplied initially with emulator or prototype objects, later on with pre-series objects and finally with production objects. This approach decouples the user-projects from the common item development and avoids idle times before the final common projects are delivered.

Common read-out unit - CRU The CRU is used by MCH, TPC, ITS, MID, TRD and ZDC. Once the front-end board and front-end link design of the sub-detector project has advanced sufficiently, prototype system tests will be conducted to demonstrate the system feasibility. In this phase the final CRU will not yet be available in production quantity, as the final production is foreseen at a later stage in order to profit from the decrease in price of FPGA and optical components. However, the interface towards the front-end is strictly defined and functional equivalent prototypes are available already at present, allowing the sub-detector projects to evaluate their system design already in the initial design phase. During the sub-detector construction phase the sub-detector projects will be provided with pre-series versions of the CRU. The CRU

project provides a common firmware frame-work which contains the interfaces to the O^2 via the DDL3, the interface to the CTP system via the TTS and an internal application independent front-end data interface. The sub-detector firmware designers will develop the application specific code providing the data path between the front-end links and the CRU internal front-end data interface.

Central Trigger Processor - CTP The CTP and timing and trigger distribution system (TTS) naturally interfaces to all sub-detector systems. The sub-detector systems need to qualify the TTS interface in their read-out and front-end systems. In case of detectors using the CRU to distribute the timing and trigger information, the hardware interface to the CTP is ensured by the CRU. For early development phases, when the CTP and local trigger units (LTU) do not yet exist, FPGA emulator firmware will be installed in the CRU emulators. For those detectors receiving the TTS directly from the CTP system via fast trigger links (FTL) FPGA cards will emulate the TTS protocol. Detectors using the TTS system still based on TTC will be using the Run1/2 version of the LTU in the early development phase. During the pre-series phase all detectors use the upgraded LTU pre-series which act as CTP emulator either connected to the CRU or to the detector front-end electronics directly. The CTP pre-series will be available for commissioning phase.

SAMPA The common TPC/MCH read-out ASIC, SAMPA, is integral part of the TPC and MCH upgrade. The SAMPA project is organised as a sub-project where TPC and MCH teams contribute to the specification, to the testing and the qualification of the ASIC with the chamber systems. For the development of the front-end boards the SAMPA project delivers the first evaluation ASIC (MPW1) allowing the detector teams to qualify the analog performance. The subsequent ASIC submission foresees a full scale ASIC with final dimension and package, allowing the detector teams to build final scale and functionally front-end prototypes and pre-series. The final production delivery is foreseen for the final front-end card production.

GBT and versatile link optical components The GBTx ASIC is needed for front-end card design and tests for TPC, MCH, MID and TOF. Presently GBTx ASICs are already available in small quantities and pre-series quantities will be available in time for the prototype electronics design. Furthermore, FPGA firmware emulators are available to the development teams already now. The versatile link optical components are already available in pre-series quantities. The final production for the versatile link components and GBTx ASIC is planned much earlier in time than for the front-end electronics production. For the SCA the first samples will be available together with the final GBTx production.

Online/offline system - O^2 The O^2 system reads the detector data from the CRUs or the detector specific read-out systems, serves as interface to the detector control system (DCS) and for MCH, TPC and MID provides the interface to the CTP system. Initially during the sub-detector design phase the O^2 system will be emulated by personal computers acting as first level processor prototypes. As the DDL3 which is the interface to the common read-out unit (CRU), is fully based on a commercial interface no hardware development effort is needed. The software layer is based on the present DDL1/2 interfaces which is already available to the sub-detector projects for the design and construction of prototypes.

16.2.2 Installation & Commissioning

Installation coordination between the detectors described in this document is not critical as the installation and commissioning can be done in parallel. Commissioning and installation is organised in three phases. The Gantt diagram shows for each sub system the time scheduled for these tests.

Commissioning on surface During commissioning on surface vertical slice system tests are performed where full chain setups are built reflecting the final installation scenario comprising all elements including the CTP, TTS, CRU, O^2 emulator and services such as cooling and power supplies. This phase will follow the system test phase during development and production. That means that the components and the interfaces between them already have been verified. Thus, the commissioning at surface phase is dedicated to the final verification of the systems with the ALICE common components.

This phase is of particular importance for the detectors upgrading their on-detector electronics, ITS, MCH, MID and TPC as it allows the verification of the full system functionality with the final components. These system will build up a full sector of their systems on surface. The surface tests allow decoupling the functional commissioning from the commissioning in ALICE. It is foreseen that optimisations are performed via FPGA firmware optimisations or control software. Applying the final functional modules of the common items, LTU, CRU and TTS, allows the verification of the full control loop and data read-out chain as shown in 2.10. The automatic calibration routines can be exercised and optimised.

Installation Only the MCH and MID involve a high number of electronics cards to be installed, whereas the other detectors described in this document install a low number of electronics cards. The MCH installs 16500 front-end cards and 500 GBT read-out cards. The MID replaces 2384 front-end cards and 250 local/regional cards. This work is planned during several months, however, the physical infrastructure in ALICE allows installation with other system at the same time and thus does not need overall coordination. Both the MCH and MID front-end cards feature self testing circuitry which allow the verification of correct connectivity once connected to the respective read-out cards. The MCH/MID CRUs sit in a control room and can be installed at any time. The MID local and regional cards sit in easily accessible crates. Once partitions of the system are installed full chain connectivity tests are performed and faulty connections will be immediately identified. The FIT detector needs installation coordination with the ALICE tracker system. The ZDC will change front-end and off-detector electronics but consists only of 22 channels. The other detectors (TRD, TOF) will replace only their off-detector read-out and do not replace the front-end cards. Thus, the number of modules to install is low and this will be done within days.

Commissioning in ALICE The system commissioning phase in ALICE repeats the surface tests, however, now for the full system, involving the final ALICE systems components with the optical fiber network from the cavern to the counting room, the first level processors (FLP) and CRUs already in place, connected to each other and verified. In this phase the correct detector component installation is verified and issues which could not be emulated during the surface tests will be highlighted. The commissioning phase for the detectors will go hand in hand with the installation. Especially for the detectors where many modules are installed, as MCH, the commissioning phase immediately starts when already some partitions of the detector have been installed in parallel to the installation of the remaining modules. These verification procedures

make use of the detector self testing circuitry together with the ALICE system control loop (see section 2.8) and allows an immediate control of the correct detector and network installation. In the example of the MCH, as soon as one on-detector GBT read-out card and its corresponding front-end cards have been installed and connected via the fiber network to the LTU and FLP, immediate verification of the correct connectivity can be performed. From the LTU, test trigger sequences are sent via the CRU to the front-end electronics. These test triggers initiate the self testing circuitry in the front-end ASIC, SAMPA, and the transmission of predefined data patterns via the GBT front-end links and the CRU to the FLP, where they are verified. This procedure allows within seconds to verify several transmission interfaces and functional blocks in the control and data loop: TTS and front-end link to detector (LTU - CRU - GBT card - SAMPA ASIC), front-end link from detector (SAMPA - GBT card - CRU) and the DDL3 (CRU - FLP). In case an error has been identified portable modules, which emulate the ALICE trigger and read-out systems, can be connected to the module under investigation instead of connecting the full ALICE system via the fiber network. It should be noted that the final tuning of trigger and clock delays will be done with the beam, see section 2.8.

16.3 Cost

Table 16.6 summarises the cost of the described detector upgrades. A majority of the upgrade effort involves the production of standard electronics boards, where no research is needed and the cost of these items has been estimated from previous experience and actual cost offers. The SAMPA ASIC development is not a standard effort and thus involves larger uncertainties. For this reason an additional multi-project wafer submission has been included in the cost estimate, a conservative production yield has been assumed and an additional contingency factor of 20 % has been applied. The cost estimate of the CRU is based on actual built prototypes and thus the uncertainty is small. Nevertheless, a 15 % overall margin has been applied. The installation and purchase of fibers has been evaluated for the most complicated installation scenario of the TPC by two individual enterprises. The cost of common items CRU are accounted for in the sub-detector projects using them. For detailed cost information, refer to the individual chapters.

Figures 16.2, 16.3, 16.4, 16.5, and 16.6 show a summary of milestones and resources for the detectors described in this technical design report and a total cost summary.

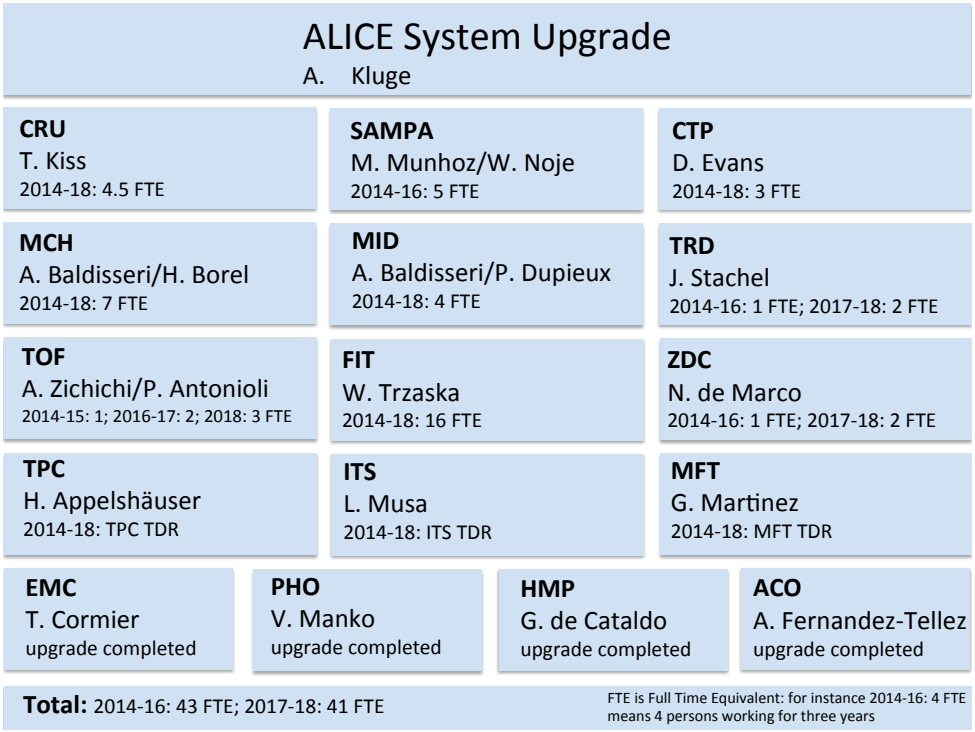


Figure 16.1: Structure of read-out and trigger upgrade.

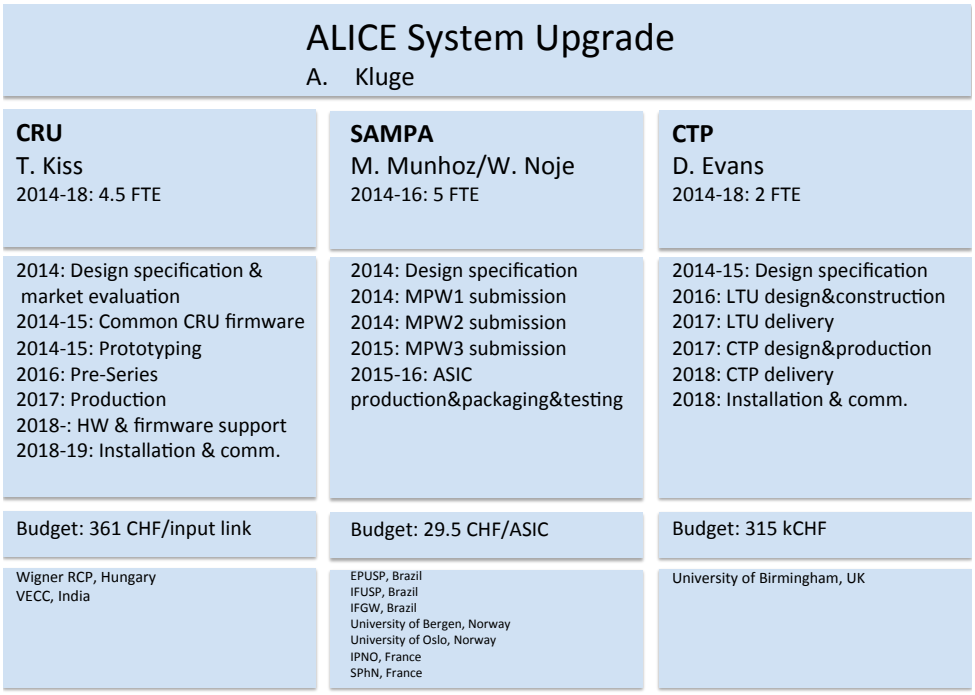


Figure 16.2: Summary of CRU, SAMPA and CTP.

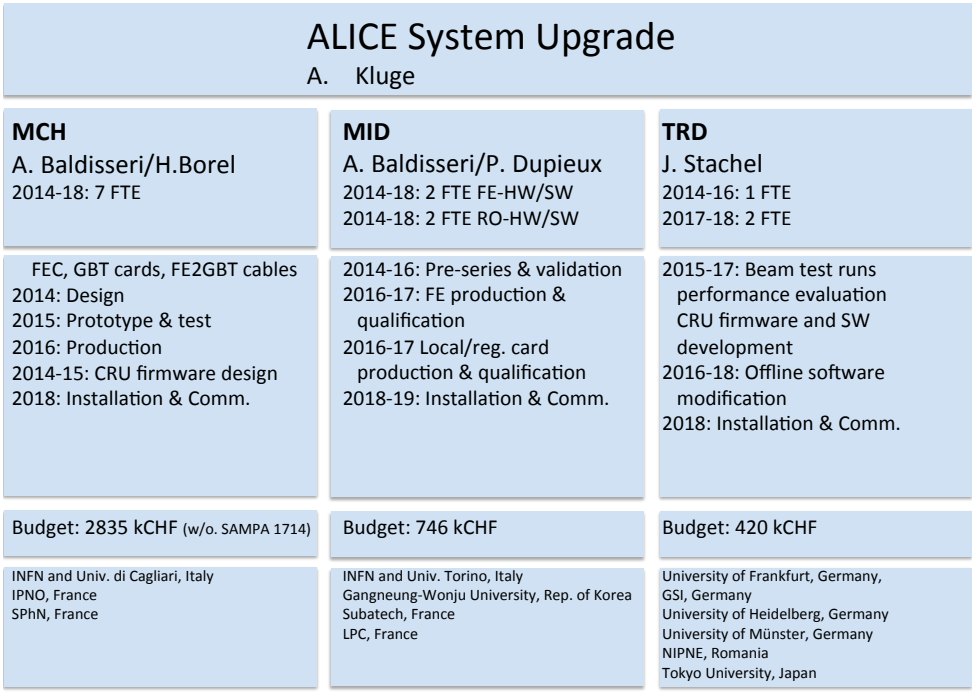


Figure 16.3: Summary of MCH, MID and TRD.

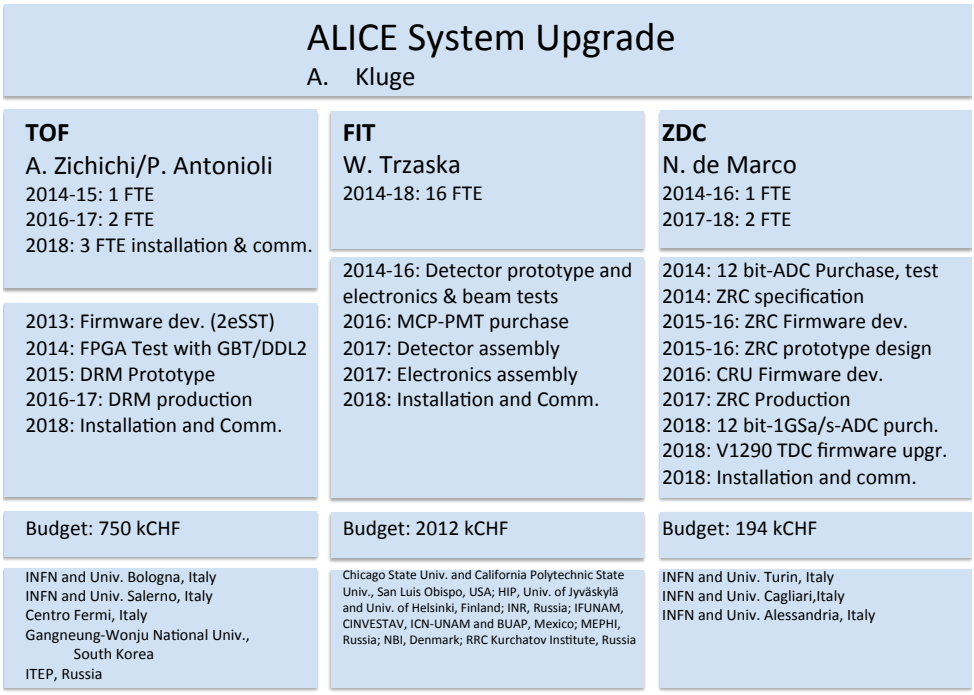


Figure 16.4: Summary of TOF, FIT and ZDC.

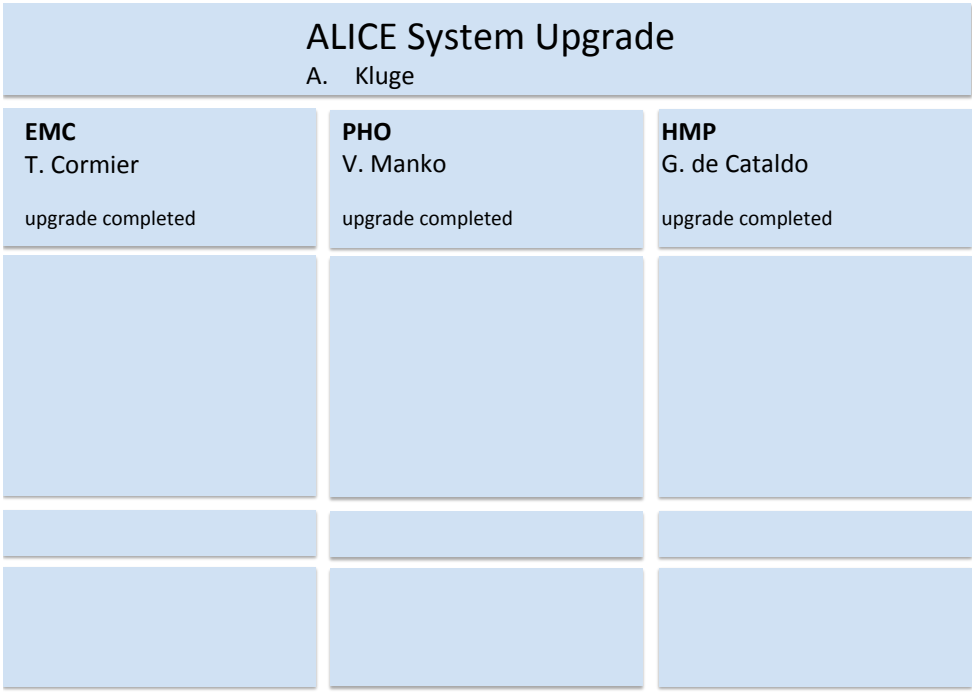


Figure 16.5: Summary of EMC, PHO and EMC.

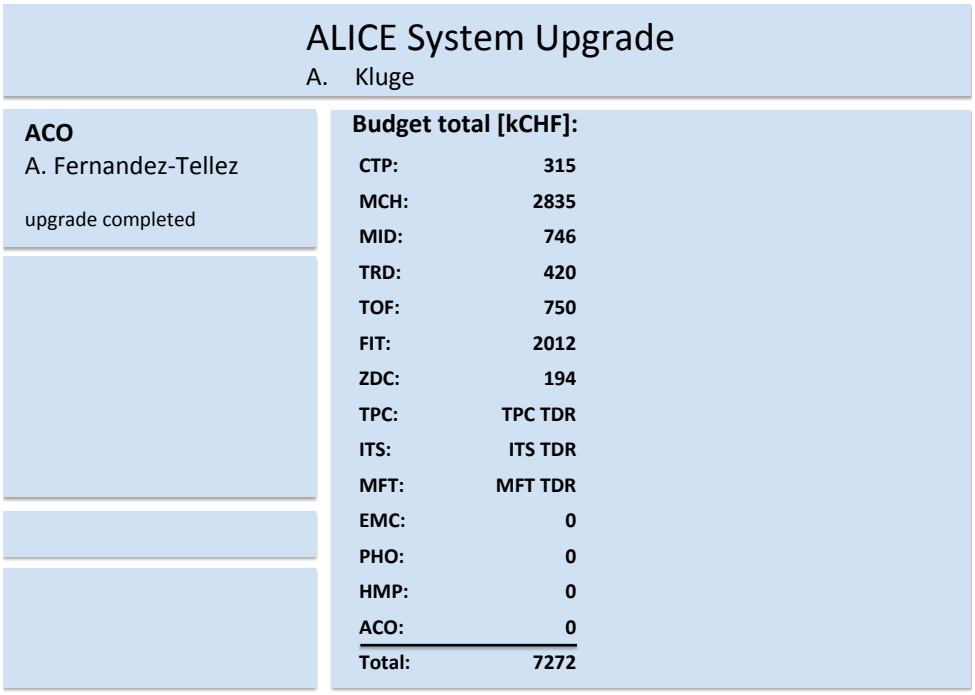


Figure 16.6: Summary of ACO and total cost overview.

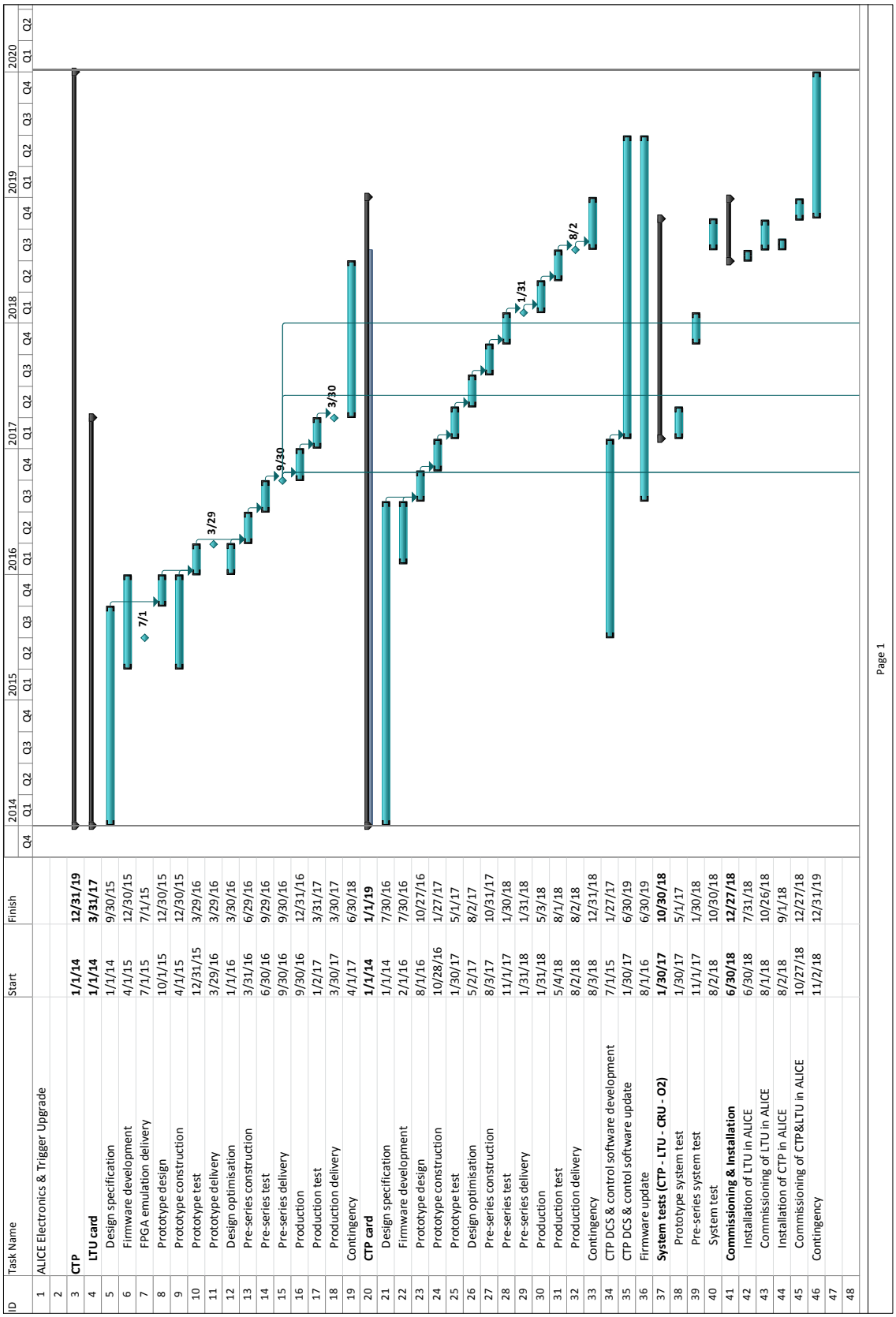


Figure 16.7: Gantt chart, page 1.

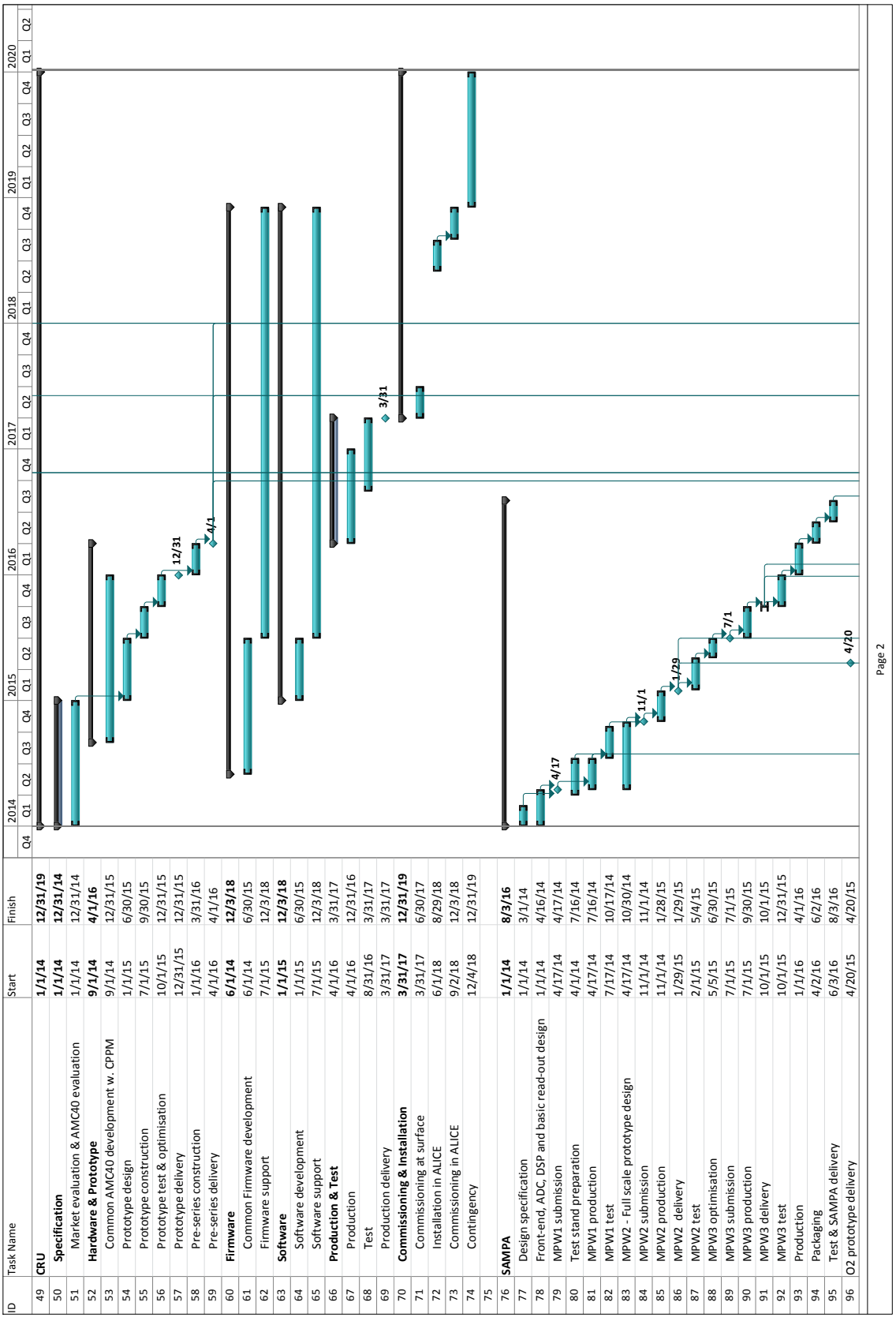
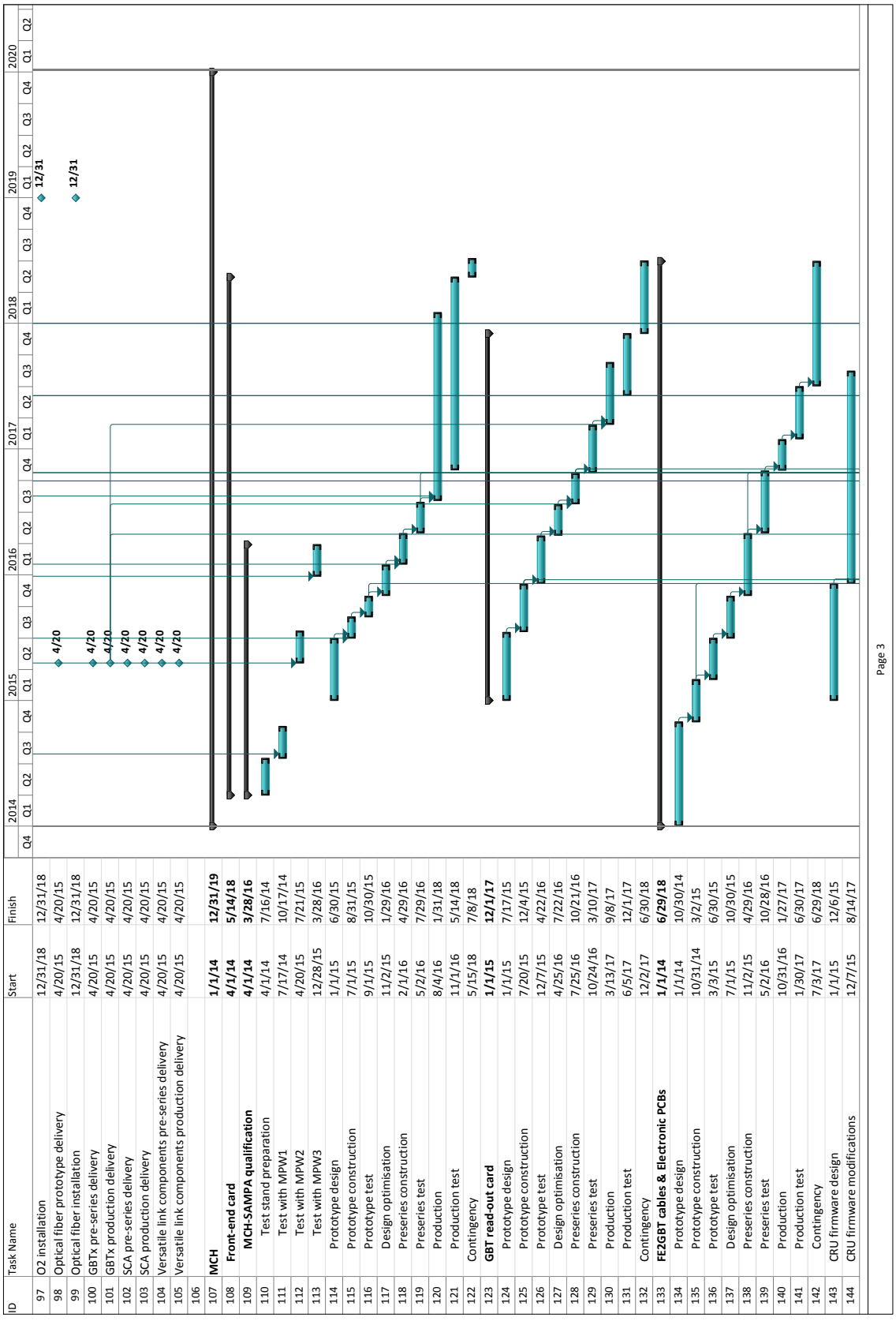


Figure 16.8: Gantt chart, page 2.



ID	Task Name	Start	Finish
97	O2 installation	12/31/18	12/31/18
98	Optical fiber prototype delivery	4/20/15	4/20/15
99	Optical fiber installation	12/31/18	12/31/18
100	GBTx pre-series delivery	4/20/15	4/20/15
101	GBTx production delivery	4/20/15	4/20/15
102	SCA pre-series delivery	4/20/15	4/20/15
103	SCA production delivery	4/20/15	4/20/15
104	Versatile link components pre-series delivery	4/20/15	4/20/15
105	Versatile link components production delivery	4/20/15	4/20/15
106			
107	**MCH**	**1/1/14**	**12/31/19**
108	**Front-end card**	**4/1/14**	**5/14/18**
109	**MCH-SAMPA qualification**	**4/1/14**	**3/28/16**
110	Test stand preparation	4/1/14	7/16/14
111	Test with MPW1	7/17/14	10/17/14
112	Test with MPW2	4/20/15	7/21/15
113	Test with MPW3	12/28/15	3/28/16
114	Prototype design	1/1/15	6/30/15
115	Prototype construction	7/1/15	8/31/15
116	Prototype test	9/1/15	10/30/15
117	Design optimisation	11/2/15	1/29/16
118	Preseries construction	2/1/16	4/29/16
119	Preseries test	5/2/16	7/29/16
120	Production	8/4/16	1/31/18
121	Production test	11/1/16	5/14/18
122	Contingency	5/15/18	7/8/18
123	**GBT read-out card**	**1/1/15**	**12/1/17**
124	Prototype design	1/1/15	7/17/15
125	Prototype construction	7/20/15	12/4/15
126	Prototype test	12/7/15	4/22/16
127	Design optimisation	4/25/16	7/22/16
128	Preseries construction	7/25/16	10/21/16
129	Preseries test	10/24/16	3/10/17
130	Production	3/13/17	9/8/17
131	Production test	6/5/17	12/1/17
132	Contingency	12/2/17	6/30/18
133	**FE2GBT cables & Electronic PCBs**	**1/1/14**	**6/29/18**
134	Prototype design	1/1/14	10/30/14
135	Prototype construction	10/31/14	3/2/15
136	Prototype test	3/3/15	6/30/15
137	Design optimisation	7/1/15	10/30/15
138	Preseries construction	11/2/15	4/29/16
139	Preseries test	5/2/16	10/28/16
140	Production	10/31/16	1/27/17
141	Production test	1/30/17	6/30/17
142	Contingency	7/3/17	6/29/18
143	CRU firmware design	1/1/15	12/6/15
144	CRU firmware modifications	12/7/15	8/14/17

Figure 16.9: Gantt chart, page 3.

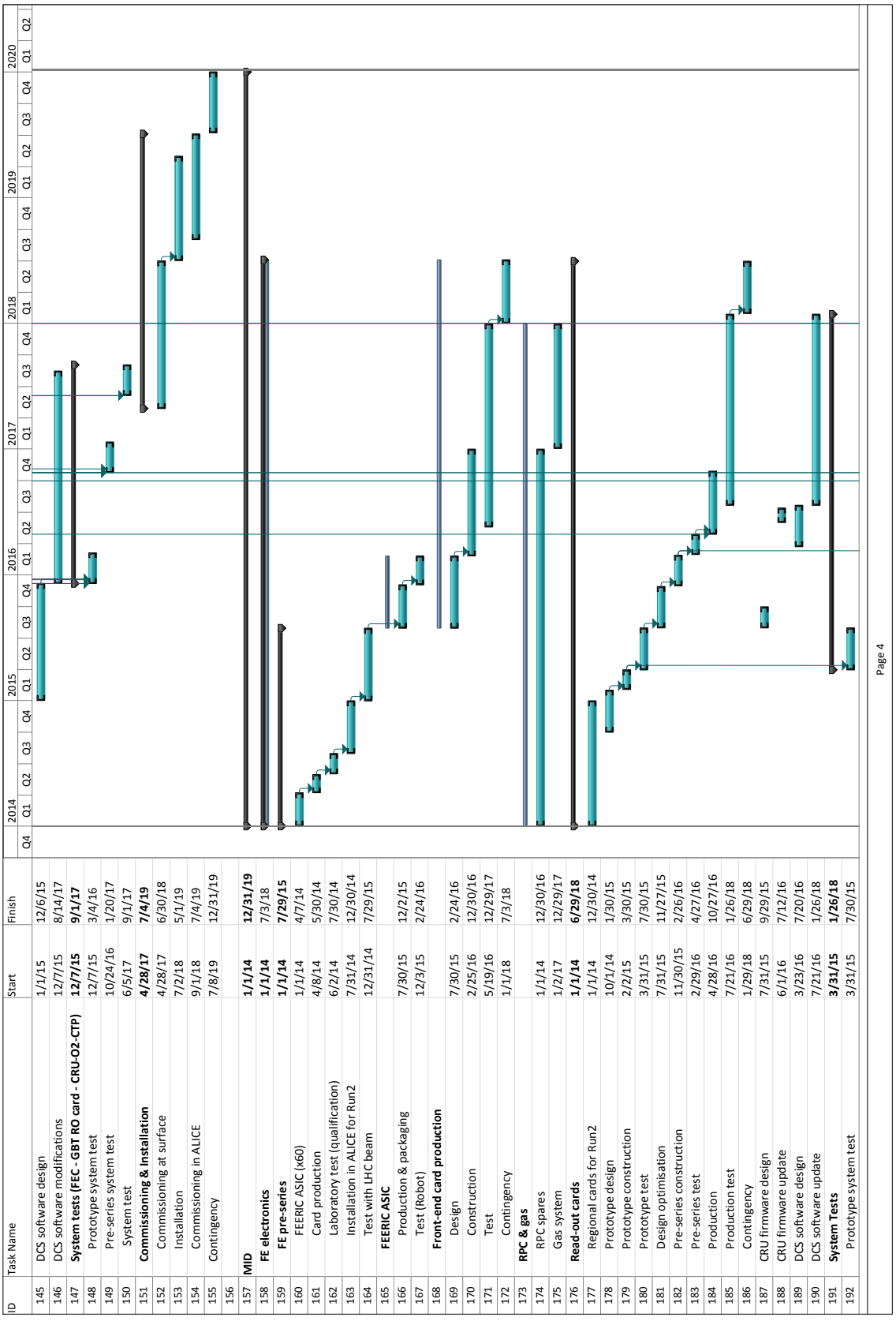


Figure 16.10: Gantt chart, page 4.

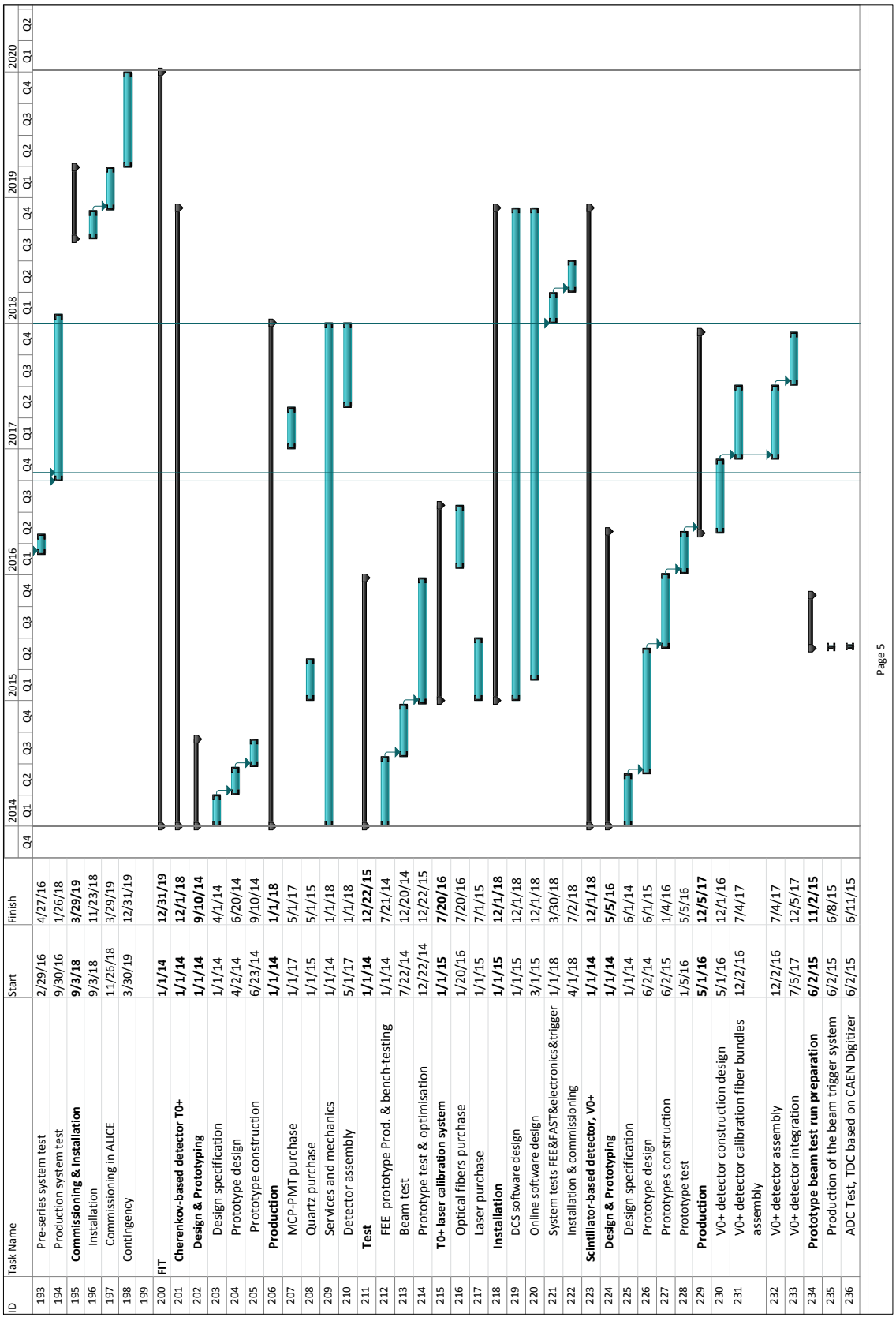


Figure 16.11: Gantt chart, page 5.

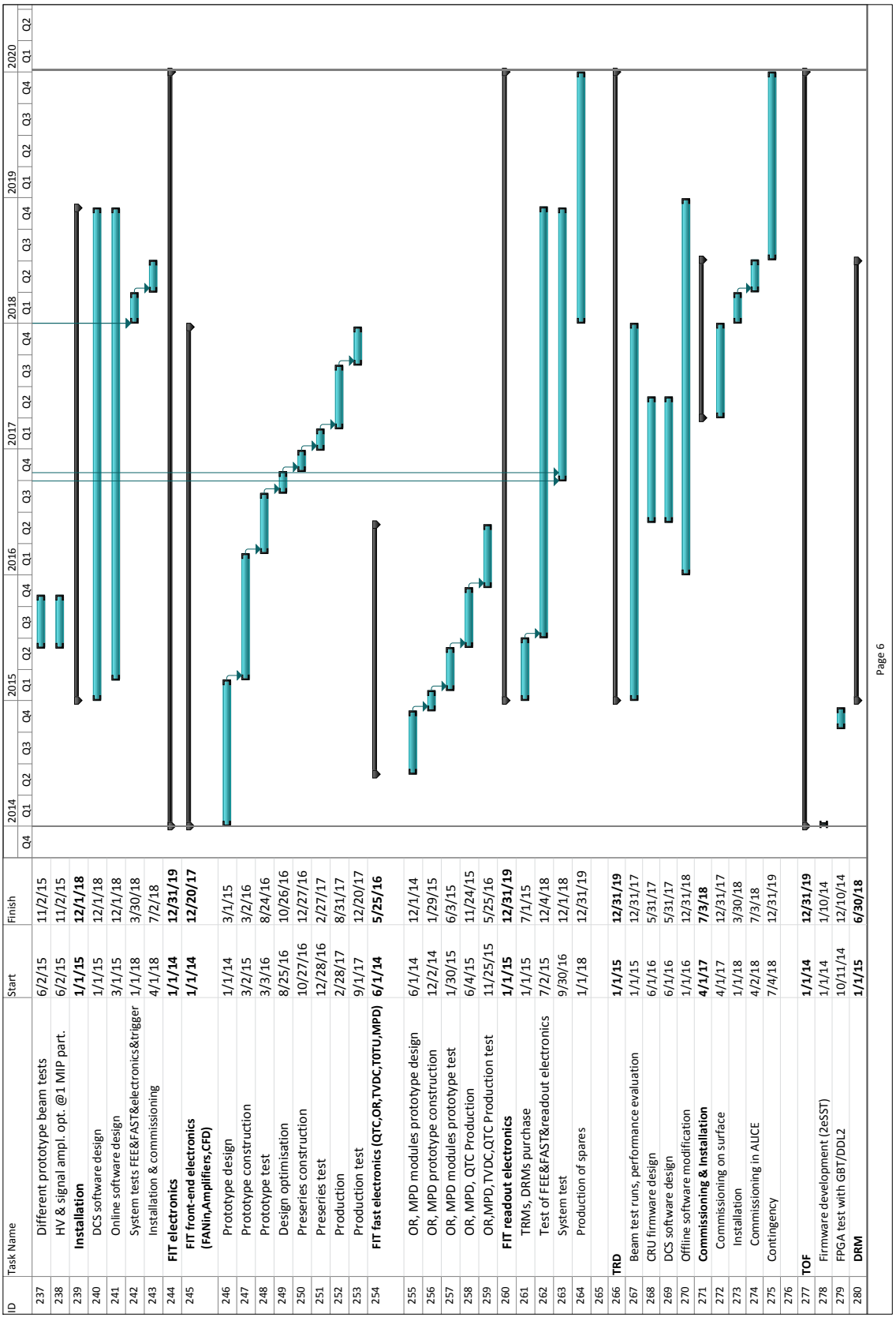


Figure 16.12: Gantt chart, page 6.

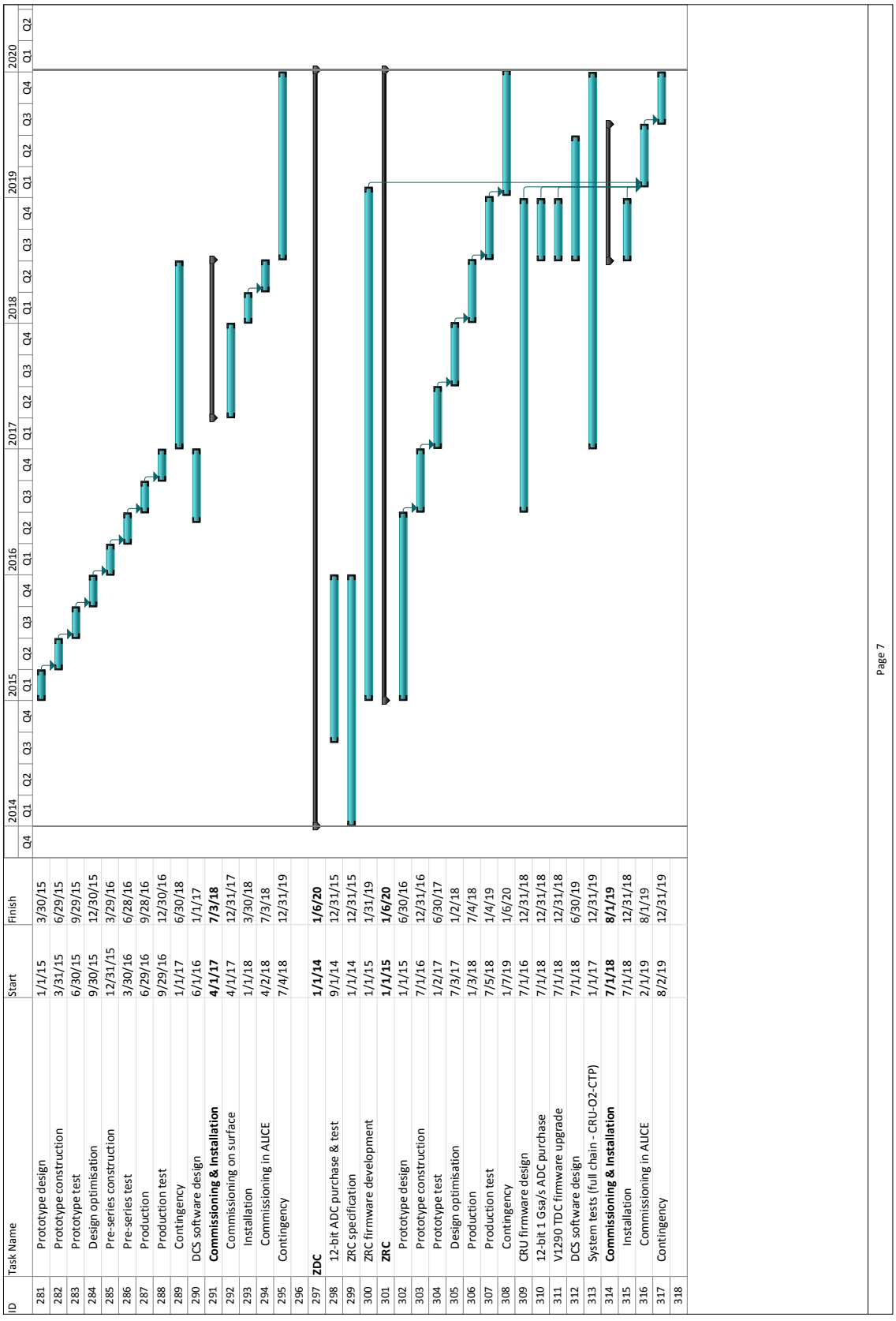


Figure 16.13: Gantt chart, page 7.

17 The ALICE collaboration

B. Abelev[74], J. Adam[38], D. Adamová[82], M.M. Aggarwal[86], G. Aglieri Rinella[34], M. Agnello[92,109], A. Agostinelli[26], N. Agrawal[45], Z. Ahammed[128], N. Ahmad[18], A. Ahmad Masoodi[18], I. Ahmed[15], S.U. Ahn[67], S.A. Ahn[67], I. Aimo[92,109], S. Aiola[133], M. Ajaz[15], A. Akindinov[57], D. Aleksandrov[98], B. Alessandro[109], D. Alexandre[100], A. Alici[103,12], A. Alkin[3], J. Alme[36], T. Alt[40], V. Altini[31], S. Altinpinar[17], I. Altsybeev[127], C. Alves Garcia Prado[117], C. Andrei[77], A. Andronic[95], V. Anguelov[91], J. Anielski[52], T. Antičić[96], F. Antinori[106], P. Antonioli[103], L. Aphecetche[110], H. Appelshäuser[50], M. Arba[104], N. Arbor[70], S. Arcelli[26], N. Armesto[16], R. Arnaldi[109], T. Aronsson[133], I.C. Arsene[21,95], M. Arslandok[50], A. Augustinus[34], R. Averbeck[95], T.C. Awes[83], M.D. Azmi[18,88], M. Bach[40], A. Badalà[105], Y.W. Baek[41,69], S. Bagnasco[109], R. Bailhache[50], V. Bairathi[90], R. Bala[89], A. Baldisseri[14], F. Baltasar Dos Santos Pedrosa[34], J. Bán[58], R.C. Baral[60], R. Barbera[27], F. Barile[31], G.G. Barnaföldi[132], L.S. Barnby[100], V. Barret[69], J. Bartke[114], M. Basile[26], N. Bastid[69], J. Basu[99], S. Basu[128], B. Bathen[52], G. Batigne[110], B. Batyunya[65], P.C. Batzing[21], C. Baumann[50], I.G. Bearden[79], H. Beck[50], C. Bedda[92], N.K. Behera[45], I. Belikov[53], F. Bellini[26], R. Bellwied[119], E. Belmont-Moreno[63], Gy. Bencédi[132], J.L. Beney[110], S. Beole[25], I. Berceanu[77], A. Bercuci[77], Y. Berdnikov[II,84], D. Berényi[132], M.E. Berger[113], A.A.E. Bergognon[110], R.A. Bertens[56], D. Berzano[25], L. Betev[34], A. Bhasin[89], A.K. Bhati[86], B. Bhattacharjee[42], J. Bhom[124], L. Bianchi[25], N. Bianchi[71], J. Bielčík[38], J. Bielčíková[82], A. Bilandzic[79], S. Bjelogrlic[56], F. Blanco[10], D. Blau[98], C. Blume[50], F. Bock[73,91], F.V. Boehmer[113], A. Bogdanov[75], H. Bøggild[79], M. Bogolyubsky[54], M. Bombara[39], J. Book[50], H. Borel[14], A. Borissov[94,131], J. Bornschein[40], F. Bossú[64], M. Botje[80], E. Botta[25], S. Böttger[49], P. Braun-Munzinger[95], M. Bregant[117,110], T. Breitner[49], T.A. Broker[50], T.A. Browning[93], M. Broz[37], E. Bruna[109], G.E. Bruno[31], D. Budnikov[97], H. Buesching[50], S. Bufalino[109], P. Buncic[34], O. Busch[91], Z. Buthelezi[64], D. Caffarri[28], X. Cai[7], H. Caines[133], A. Caliva[56], E. Calvo Villar[101], P. Camerini[24], V. Canoa Roman[34], F. Carena[34], W. Carena[34], F. Carminati[34], A. Casanova Díaz[71], J. Castillo Castellanos[14], E.A.R. Casula[23], V. Catanescu[77], C. Cavicchioli[34], C. Ceballos Sanchez[9], J. Cepila[38], P. Cerello[109], V. Chambert[48], B. Chang[120], S. Chapeland[34], J.L. Charvet[14], S. Chattopadhyay[128], S. Chattopadhyay[99], M. Cherney[85], C. Cheshkov[126], B. Cheynis[126], V. Chibante Barroso[34], D.D. Chinellato[119,118], P. Chochula[34], M. Chojnacki[79], S. Choudhury[128], P. Christakoglou[80], C.H. Christensen[79], P. Christiansen[32], T. Chujo[124], S.U. Chung[94], C. Cicalo[104], L. Cifarelli[12,26], F. Cindolo[103], J. Cleymans[88], F. Colamaria[31], D. Colella[31], A. Collu[23], M. Colocci[26], G. Conesa Balbastre[70], Z. Conesa del Valle[48,34], M.E. Connors[133], G. Contin[24], J.G. Contreras[11], T.M. Cormier[83,131], Y. Corrales Morales[25], P. Cortese[30], I. Cortés Maldonado[2], M.R. Cosentino[73,117], F. Costa[34], P. Crochet[69], R. Cruz Albino[11], E. Cuautle[62], L. Cunqueiro[71,34], A. Dainese[106], R. Dang[7], A. Danu[61], D. Das[99], I. Das[48], K. Das[99], S. Das[4], L. Das Bose[99], A. Dash[118], S. Dash[45], E. Dávid[132], S. De[128], E. Delagne[14], H. Delagrange[I,110], A. Deloff[76], E. Dénes[132], G. D'Erasmo[31], G.O.V. de Barros[117], A. De Caro[12,29], G. de Cataldo[102], J. de Cuveland[40], A. De Falco[23], D. De Gruttola[29,12], N. De Marco[109], S. De Pasquale[29], R. de Rooij[56], M.A. Diaz Corchero[10], T. Dietel[52,88], R. Divià[34], D. Di Bari[31], S. Di Liberto[107], A. Di Mauro[34], P. Di Nezza[71], Ø. Djuvsland[17], A. Dobrin[56,131], T. Dobrowolski[76], D. Domenicis Gimenez[117], B. Dönigus[50], O. Dordic[21],

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Glossary

ACO ALICE Cosmic Ray Detector.

ADC Anaolog to Digital Converter.

ALICE A Large Ion Collider Experiment.

ALTRO ALICE TPC Read Out ASIC.

ASIC Application Specific Integrated Circuit.

ATCA Advanced Telecommunications Computing Architecture.

ATLAS A Toroidal LHC Apparatus.

BC Bunch Crossing.

BC1 First Baseline Correction.

BC2 Second Baseline Correction.

BCID Bunch Crossing Identification Number.

CAEN Costruzioni Apparecchiature Elettroniche Nucleari S.p.A..

CDH Common Data Header.

CIU Channel Interface Unit.

CMFB Common-Mode Feed-Back network.

CMOS Complementary Metal Oxide Semiconductor.

CMS Compact Muon Solenoid.

CPDM Clock and Pulse Distribution Module.

CRC Cyclic redundancy check.

CROCUS Concentrator Read-Out Cluster Unit System.

CRU Common Read-out Unit.

CSA Charge Sensitive Amplifier.

CsI Caesium Iodide.

CSP Charge Sensitive Preamplifier.

CTP Central Trigger Processor.

DAQ Data Acquisition.

DC Direct Current.

DCS Detector Control System.

DDL Detector Data Link.

DNL Differential nonlinearity.

DRM Data Read-out Module.

DSP Digital Signal Processor.

DTC Data, Trigger, Clock and Control.

ECS Experimental Control System.

EMC Electro Magnetic Calorimeter.

EMD Electromagnetic Dissociation Processes .

ENC Equivalent Noise Charge.

ENOB Effective number of bits.

EOD End of Data.

FAIR Facility for Antiproton and Ion Research.

FE Front-end.

FEC Front-end Card.

FEE Front-end Electronics.

FEERIC A very-front-end ASIC for the ALICE Muon Trigger Resistive Plate Chambers.

FIFO First-In First-Out.

FIT Fast Interaction Trigger.

FLUKA Fully integrated particle physics Monte Carlo simulation software package.

FMD Forward Multiplicity Detector.

FPGA Field Programmable Gate Array.

FTL Fast Serial Trigger Link.

GbE Gigabit Ethernet.

GBT GigaBit Transceiver.

GBTx Gigabit Transceiver ASIC.

GEM Gas Electron Multiplier.

GTL Gunning transceiver logic.

GTU Global Tracking Unit.

HIJING Monte Carlo Model.

HMP High Momentum Particle Identification Detector.

HPTDC High Performance Time to Digital Converter.

HV High Voltage.

I2C Inter-Integrated Circuit.

IAC Integrated Anode Charge.

IB Infini Band.

IIR Infinite impulse response .

INL Integral nonlinearity.

IO Input-output.

IP Interaction Point.

ITS Inner Tracking System.

L0 Level 0.

LDC Local Data Concentrator.

LG Low Gain.

LHC Large Hadron Collider.

LHCC LHC Experiments Committee.

LM Level -1 TRD wake-up signal.

LoI Letter of Intent.

LS1 Long Shutdown 1.

LS2 Long Shutdown 2.

LTU Local Trigger Unit.

LV Low Voltage.

LVDS Low-voltage differential signaling.

MCH Muon Chamber.

MCM Multi Channel Module.

MCP Microchannel Plate Detector.

MEB Multi Event Buffer.

MFT Muon Forward Tracker.

microTCA Micro Telecommunications Computing Architecture.

MID Muon Identifer Detector.

MIP Minimum Ionising Particle.

MPW Multi Project Wafer.

MRPC Multi Gap Resistive Plate Chamber.

MTR Muon Trigger.

MUX Data Multiplexer.

MWPC Multi Wire Proportional Chamber.

NICA Nuclotron-based Ion Collider Facility.

NMOS N-type Metal Oxide Semiconductor Logic.

O^2 Online and Offline Computing System.

p-Pb Proton-Lead.

PANDA Anti-Proto Annihilation at Darmstadt.

Pb-Pb Lead-Lead.

PC Personal Computer.

PCB Printed Circuit Board.

PCIe Peripheral Component Interconnect Express.

PCIe Gen3 Peripheral Component Interconnect Express Generation 3.

PHO Photon Spectrometer.

PID Particle Identification.

PMOS P-type Metal Oxide Semiconductor Logic.

PMT Photomultiplier Tube.

pp Proton-Proton.

PTW Processing Time Window.

PYTHIA6 Event generator.

QDC Quarge to Digital Converter.

QE Quantum Efficiency.

QGP Quark-Gluon Plasma.

RMS Root Mean Square.

RO Read-out.

ROB Read Out Branch.

RORC Read-out Receiver Cards.

RPC Resistive Plate Chamber.

Run1 ALICE operation until Long Shutdown 1.

Run2 ALICE operation between Long Shutdown 1 and 2.

S-ALTRO Super ALICE TPC Read Out ASIC.

SAMPA TPC/MCH read-out ASIC.

SAR Successive approximation.

SCA Slow Control Adapter.

SDD Silicon Drift Detector.

SEU Single Event Upset.

SFDR Spurious-free dynamic range.

SINAD Signal-to-noise and distortion ratio.

SIU Source Interface Unit.

SOD Start of Data.

SPD Silicon Pixel Detector.

SRU Scalable Read-out Unit.

SSD Silicon Strip Detector.

TC Tail Cancellation.

TCA Telecommunications Computing Architecture.

TCFU Tail Cancellation Filter.

TDC Time to Digital Converter.

TDR Technical Design Report.

TID Total Ionising Dose.

TOF Time Of Flight detector.

TOR Trigger OR.

TPC Time Projection Chamber.

TRD Transition Radiation Detector.

TRM TDC Read-out Module.

TRU Trigger Region Unit.

TSMC Taiwan Semiconductor Manufacturing Company.

TTC Timing, Trigger and Control System.

TTCrx A Timing, Trigger and Control Receiver ASIC for LHC Detectors.

TTS Trigger and Timing Distribution System.

VME Versa Module Europa.

VTRx Versatile Transceiver.

VTTx Versatile Twin-Transmitter.

ZDC Zero Degree Calorimeter.

ZRC Zero Degree Calorimeter Read-out Card.

ZS Zero Suppression.

ZSU Zero Suppression Unit.

ZTC Zero Degree Calorimeter Trigger Card.

Bibliography

[1] ALICE Collaboration, *Letter of Intent for the Upgrade of the ALICE Experiment*, CERN-LHCC-2012-012, LHCC-I-022 (2012) (cit. on pp. 7, 11, 21, 37, 63, 64, 123).

[2] K. Aamodt et al., "The ALICE experiment at the CERN LHC", JINST 3 S08002 (2008) (cit. on pp. 7, 37, 63).

[3] K. Aamodt et al., "Performance of the ALICE Experiment at the CERN LHC", Int. J. Mod. Phys **A29**, arXiv:1402.4476, CERN-PH-EP-2014-031 (2014) (cit. on p. 7).

[4] ALICE Collaboration, *Conceptual Design Report for the Upgrade of the ALICE ITS*, CERN-LHCC-2012-013 (2012) (cit. on p. 9).

[5] ALICE Collaboration, *Technical Design Report for the Upgrade of the Inner Tracking System*, CERN-LHCC-2013-024, ALICE-TDR-017 (2013) (cit. on pp. 9, 27).

[6] ALICE Collaboration, *Addendum of the Letter Of Intent for the Upgrade of the ALICE Experiment: The Muon Forward Tracker*, CERN-LHCC-2013-014 (2013) (cit. on p. 9).

[7] ALICE Collaboration, *Technical Design Report for the Upgrade of the Time Projection Chamber*, CERN-LHCC-2013-020, ALICE-TDR-016 (2013) (cit. on pp. 9, 45).

[8] R. E. Bosch, A. J. de Parga, B. Mota and L. Musa, "The ALTRO Chip: A 16-Channel A/D Converter and Digital Processor for Gas Detectors", IEEE Transactions on Nuclear Science **50**, 2460–2469 (2003) (cit. on pp. 9, 45, 113).

[9] P. Aspell, M. D. Gaspari, H. França, E. García and L. Musa, "Super-ALTRO 16: a Front-End System on Chip for DSP Based Readout of Gaseous Detectors", IEEE Transactions on Nuclear Science **60**, 1289–1295,DOI: 10.1109/TNS.2013.2250305 (2013) (cit. on pp. 9, 45).

[10] L. Betev, T. Breitner, S. Chapeland, A. Gheata, B. von Haller and M. Richter, "ALICE Computing software framework for LS2 Upgrade", ALICE-INT-2013-001 (2012) (cit. on p. 11).

[11] E. Dénes, A. Fenyvesi, E. Futó, A. Kerék, T. Kiss, J. Molnár, D. Novák, C. Soós, T. Tölyhi and P. V. Vyvre, "Radiation Tolerance Qualification Tests of the Final Source Interface Unit for the ALICE Experiment", CERN-LHCC-2007-006 (2007) (cit. on pp. 11, 16).

[12] H. Engel, "Common Read-Out Receiver Card for the ALICE Run2 Upgrade", Topical Workshop on Electronics for Particle Physics 2013, September 2013, Perugia, Italy (2013) (cit. on pp. 11, 16).

[13] B.G. Taylor, "TTC Distribution for LHC Detectors", IEEE Transactions on Nuclear Science **45** (1998) (cit. on p. 11).

[14] F. Vasey, D. Hall, T. Huffman, S. Kwan, A. Prosser, C. Soos, J. Troska, T. Weidberg, A. Xian and J. Yed, "The Versatile Link common project: feasibility report", 2012 JINST 7 C01075 doi:10.1088/1748-0221/7/01/C01075 (2011) (cit. on pp. 11, 16, 18, 45, 58).

[15] O2 Project CWG4, "Proposal of an Heartbeat trigger for ALICE Run 3", (2013) (cit. on p. 15).

[16] J. P. Cachemiche et al., "Recent developments for the Upgrade of the LHCB readout system", 2013 JINST 8 C02014 doi:10.1088/1748-0221/8/02/C02014 (2013) (cit. on p. 17).

[17] A. Gabrielli, "The GBT-SCA, a radiation tolerant ASIC for detector control applications in SLHC experiments", Topical Workshop on Electronics for Particle Physics, Paris, France, 21 - 25 Sep 2009, 557–560 (cit. on p. 18).

[18] K. McDonald, "Deadtime When Using a FIFO Buffer", Princeton/BaBar/TNDC-96-44 (1996) (cit. on p. 27).

[19] A. Ferrari, P. Sala, A. Fasso and J. Ranft, "Fluka: a multi-particle transport code", CERN-2005-10, INFN/TC-05/11, SLAC-R-773 (2005) (cit. on p. 33).

[20] D. Adamova et al., "The virtual monte carlo", arXiv:cs/0306005l (cit. on p. 33).

[21] A. Morsch and B. Pastircak, "Radiation in ALICE Detectors and Electronic Racks", ALICE Internal Note ALICE-INT-2002-028 (2005) (cit. on p. 33).

[22] M. Krivda et al., "The ALICE trigger system performance for p-p and Pb-Pb collisions", JINST **7**, C01057 (2012) (cit. on p. 39).

[23] H. Takai, M. Wirthlin and A. Harding, "Soft Error Rate Estimations of the Kintex-7 FPGA within the ATLAS Liquid Argon (LAr) Calorimeter", in Topical Workshop on Electronics for Particle Physics 2013, September 2013, Perugia, Italy (2013) (cit. on p. 39).

[24] A. Bhasin et al., "Implementation of the ALICE Trigger System", in RT2007-TDAQ-TRIG06, in proceedings of 15th IEEE Real Time Conference (RT 07), Batavia, Illinois (2007) (cit. on p. 39).

[25] ALICE Collaboration, "Trigger, Data Acquisition, High Level Trigger, Control System", ALICE-DOC-2004-001 (2004) (cit. on p. 42).

[26] H. Soltveit, J. Stachel, P. Braun-Munzinger, L. Musa, H. Gustafsson et al., "The preamplifier shaper for the ALICE TPC-Detector", Nucl. Instr. Meth. **A676**, 106–119 (2012) (cit. on pp. 45, 47).

[27] W. M. Sansen and Z. Y. Chang, "Limits of low Noise performance of detector readout ends in CMOS Technology", IEEE Transactions on circuits and systems **37**, 1375–1392 (1990) (cit. on p. 47).

[28] G. Gramegna, P. O'Connor, P. Rehak and S. Hart, "CMOS preamplier for low-capacitance detectors", Nucl. Instr. Meth. **A390**, 241–250 (1997) (cit. on p. 48).

[29] H. Spieler, *Semiconductor Detector Systems*, 2nd (Oxford University Press, 2005) (cit. on p. 48).

[30] J. Peyre, B. Genolini and J. Pouthas, "A Full-Scale Prototype for the Tracking Chambers of the ALICE Muon Spectrometer. Part I: Mechanics, Anode and Cathode Plane Design, Assembly and Construction", ALICE Internal Note, ALICE-INT-1998-28 (1998) (cit. on p. 57).

[31] C. Cicalo et al., "Assembly of a large slat chamber prototype for the ALICE Muon Spectrometer", ALICE Internal Note, ALICE-INT-2002-17 (2002) (cit. on p. 57).

[32] H. Borel et al., "The Muon Tracking FEE upgrade specifications", ALICE Internal Note, ALICE-INT-2013 (2013) (cit. on p. 58).

[33] S. Bonacini et al., "E-link : A Radiation-Hard Low-Power Electrical Link for Chip-to-Chip Communication", Topical Workshop on Electronics for Particle Physics, Paris, France, 21 - 25 Sep 2009, pp.422-425 (2009) (cit. on p. 59).

[34] P. Moreira et al., "The GBT project", Topical Workshop on Electronics for Particle Physics, Paris, France, 21 - 25 Sep 2009, pp.342-346 (2009) (cit. on p. 59).

[35] C. Finck et al., "Raw data format for the MUON Spectrometer", CERN, ALICE-INT-2005-012 (cit. on p. 63).

[36] R. Arnaldi et al., "Front-end electronics for the RPCs of the ALICE dimuon trigger", IEEE Trans. Nucl. Sci. **52**, 1176–1181 (2005) (cit. on p. 63).

[37] ATLAS Collaboration, "The ATLAS experiment at the CERN LHC", JINST **3** (2008) (cit. on p. 63).

[38] CMS Collaboration, "The CMS experiment at the CERN LHC", JINST **3** (2008) (cit. on p. 63).

[39] ALICE Collaboration, "Heavy flavour decay muon production at forward rapidity in proton-proton collisions at $\sqrt{s} = 7$ TeV", Phys. Lett. B **708**, 265 (2012) (cit. on p. 63).

[40] X. Zhang, "Study of Heavy Flavours from Muons Measured with the ALICE Detector in Proton-Proton and Heavy-Ion Collisions at the CERN-LHC", PhD thesis, section 6.3.1 (2012), http://tel.archives-ouvertes.fr/docs/00/78/62/69/PDF/XZhangPD2012.pdf (cit. on p. 63).

[41] F. Bossù et al., "Performance of the ALICE RPC-based muon trigger system in the first two years of data taking at the LHC", JINST **7** (2012) (cit. on p. 64).

[42] R. Arnaldi et al., "Beam and ageing tests with a highly-saturated avalanche gas mixture for the ALICE *pp* data taking", Nucl. Phys. Proc. Suppl. **158**, 149 (2006) (cit. on p. 64).

[43] R. Cardarelli et al., "RPC performance vs. front-end electronics", Nucl. Instr. Meth. **A661**, S198 (2012) (cit. on p. 64).

[44] M. Abbrescia et al., "New developments on front-end electronics for the CMS RPC", Nucl. Instr. Meth. **A456**, 143 (2000) (cit. on p. 64).

[45] R. Arnaldi et al., "Final results of the tests on the resistive plate chambers for the ALICE muon arm", Nucl. Instr. Meth. **A602**, 740 (2009) (cit. on p. 64).

[46] ALICE Collaboration, *ALICE Technical Design Report of the Transition Radiation Detector*, CERN/LHCC 2001-021 (2001) (cit. on p. 71).

[47] V. Angelov et al., "Design and performance of the ALICE TRD front-end electronics", Nucl. Instr. Meth. **A563**, 317–320 (2006) (cit. on p. 71).

[48] A. Bercuci et al., "Offline Performance with New TRD Data Formats", ALICE internal node (2013) (cit. on p. 74).

[49] S. Kirsch et al., "An FPGA-based high-speed, low-latency processing system for high-energy physics", Proceedings of the 2010 International Conference on Field Programmable Logic and Applications, 562–567 (2010) (cit. on p. 76).

[50] A. Akindinov et al., "Performance of the ALICE Time-Of-Flight detector at the LHC", Eur. Phys. Journal Plus **44**, 128 (2013) (cit. on p. 81).

[51] A. Akindinov et al., "A study of the multigap RPC at the gamma irradiation facility at CERN", Nucl. Instr. Meth. **A490**, 58 (2002) (cit. on p. 81).

[52] A. Akindinov et al., "Space charge limited avalanche growth in multigap resistive plate chambers", Eur. Phys. Journal C **34**, 325 (2004) (cit. on p. 81).

[53] A. Akindinov et al., "The ALICE Time-Of-Flight system: Construction, assembly and quality tests", Nuovo Cimento B **124**, 235 (2009) (cit. on p. 82).

[54] A. Akindinov et al., "Design aspects and prototype test of a very precise TDC system implemented for the multigap RPC of the ALICE-TOF", Nucl. Instr. Meth. **A553**, 178 (2004) (cit. on p. 82).

[55] M. Mota, J. Christiansen et al., "A flexible multi-channel high-resolution Time-to-Digital Converter ASIC", Nuclear Science Symposium Conference Record, 2000 IEEE **2**, 155 (2000) (cit. on p. 82).

[56] J. Christiansen, "HPTDC: High Performance Time To Digital Converter", http://tdc.web.cern.ch/TDC/hptdc/docs/hptdc_manual_ver2.2.pdf (2004) (cit. on p. 82).

[57] A. Alici et al., "A first study of the TOF upgrade at the LS2", ALICE-INT-2012-007 (2012) (cit. on p. 83).

[58] VMEbus International Trade Association (VITA), *VME 2eSST: Source Synchronous Transfer protocol specification*, ANSI/VITA 1.5-2003 (R2009) (2003) (cit. on p. 84).

[59] M.Bondila et al, "ALICE T0 detector", IEEE Trans. Nucl. Sc. **52**, 1705 (2005) (cit. on p. 87).

[60] E. Abbas et al., "Performance of the ALICE VZERO system", CERN-PH-EP-2013-082 (cit. on pp. 87, 90, 102).

[61] The ALICE Collaboration, "The ALICE experiment at the CERN LHC", JINST **3**, 125–132 (2008) (cit. on p. 87).

[62] The ALICE Collaboration, "Centrality determination of PbPb collisions at $\sqrt{s_{NN}}$=2.76 TeV with ALICE", CERN-PH-EP-2012-368, nucl-ex/1301.4361 (2012) (cit. on p. 90).

[63] Y. Zoccarato et al., "Front end electronics and first results of the ALICE V0 detector", Nucl. Instr. Meth. **A626**, 90 (2011) (cit. on p. 90).

[64] M. Wetstein et al., "Development of sub-nanosecond, high gain structures for time-of-flight ring imaging in large area detectors", Nucl.Instrum.Meth. **A639**, 148–150 (2011) (cit. on p. 92).

[65] M. Barnyakov and M. Yu. and A.V. Mironov, "Photocathode ageing in MCP PMT", JINST **6**, C12026 (2011) (cit. on p. 92).

[66] Photonis, http://www.photonis.com/en/ (cit. on p. 92).

[67] Panda collaboration, http://www-panda.gsi.de (cit. on p. 92).

[68] NICA collaboration, http://nica.jinr.ru (cit. on p. 92).

[69] A. Lehmann, "Lifetime measurements of MCP-PMTs", DIRC2013: Workshop on fast Cherenkov detectors, Giessen Sept 4, 2013 (cit. on p. 93).

[70] D. Brahy and E. Rossa, "High-rate photomultiplier-base and precise timing calibration", Nucl.Instrum.Meth. **158**, 121 (1979) (cit. on p. 105).

[71] D. Brahy and E. Rossa, "A low-level ultra-fast differential discriminator", Nucl. Instr. Meth. **A192**, CERN/SPS/81-11 (EBP), 359 (1982) (cit. on p. 105).

[72] B. Franek and C. Gaspar, *Smi++ – state management interface*, http://smi.web.cern.ch/smi/; accessed 18-October-2013, \url{http://smi.web.cern.ch/smi/} (cit. on p. 105).

[73] C. Gaspar et al., *Dim – distributed information management system*, http://dim.web.cern.ch/dim/; accessed 18-October-2013, \url{http://dim.web.cern.ch/dim/} (cit. on p. 105).

[74] S. Siddhanta et al., "The readout system for the ALICE zero degree calorimeters", IEEE Trans.Nucl.Sci. **58**, 1759–1765 (2011) (cit. on p. 105).

[75] T. C. Awes et al., "The ALICE electromagnetic calorimeter", Nucl. Instr. Meth. **A617**, 5 (2010) (cit. on p. 113).

[76] H. Muller et al., "Configurable electronics with low noise and 14-bit dynamic range for photodiode-based photon detectors", Nucl. Instr. Meth. **A565**, 768 (2006) (cit. on p. 113).

[77] L. Musa et al., "ALICE TPC Front-end electronics", EEE Trans. Nucl. Sci. **5**, 3647 (2003) (cit. on p. 113).

[78] H. Muller et al., "Hierarchical trigger of the ALICE calorimeters", Nucl. Instr. Meth. **A617**, 344 (2010) (cit. on p. 113).

[79] J. Kral et al., "L0 trigger for the EMCal detector of the ALICE experiment", Nucl. Instr. Meth. **A693**, 261 (2012) (cit. on p. 113).

[80] Fan Zhang et al., "Point-to-Point Readout Electronics for the ALICE EMCal Detector", (cit. on p. 114).

[81] S. Martoiu et al., "Front-end electronics for the Scalable Readout System of RD51", EEE Trans. Nucl. Sci., 2036 (2011) (cit. on p. 114).

[82] S. Martoiu et al., "Development of the scalable readout system for micro-pattern gas detectors and other applications", JINST, C03015 (2011) (cit. on p. 114).

[83] A. Sancho, "Receiver ASIC for timing, trigger and control distribution in LHC experiments", EEE Trans. Nucl. Sci. **43**, 1773 (1996) (cit. on p. 114).

[84] ALICE collaboration, "EMCal Technical Design Report", CERN-LHCC-2006-014 (cit. on p. 120).

[85] Fan Zhang, "Private communication", (cit. on p. 121).

[86] Y. Kharlov, "PHOS plans for switchover to SRU readout. CTF meeting 03.07.2013 (https://indico.cern.ch/conferencedisplay.py?confid=260463)", (cit. on p. 121).

[87] ALICE collaboration, *ALICE Technical Design Report*, CERN/LHCC 98-19 (1998) (cit. on p. 123).

[88] ALICE collaboration, "Results from the ageing studies of large CsI photocathodes exposed to ionizing radiation in a gaseous RICH detector", Nucl. Instr. Meth. **A 553**, 187–195 (2012) (cit. on p. 123).

[89] ALICE collaboration, "Long term performance and ageing of CsI photocathodes for the ALICE/HMPID detector", Nucl. Instr. Meth. **A 574**, 28 –38 (2007) (cit. on p. 123).

[90] G. Volpe, *Studio di caratterizzazione del rivelatore RICH dell'esperimento ALICE al CERN*, Master degree thesis, Bari University, 2003. () (cit. on p. 124).

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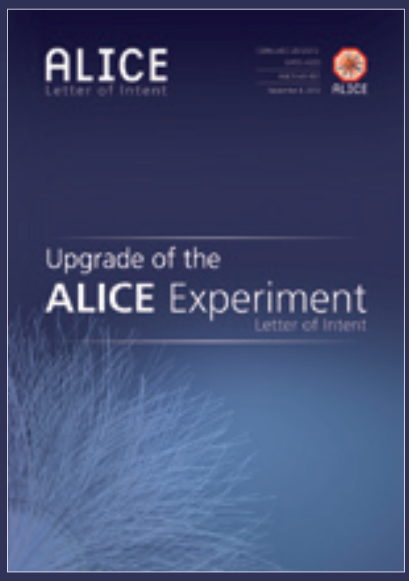

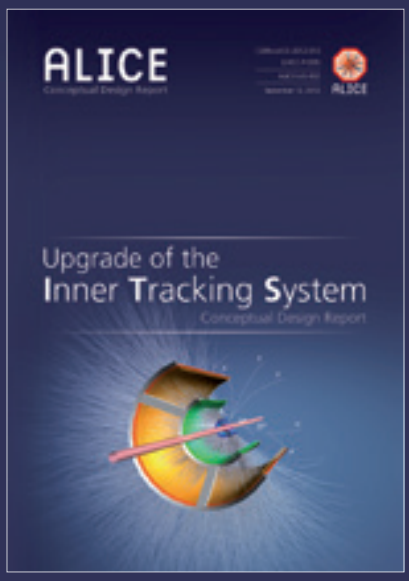

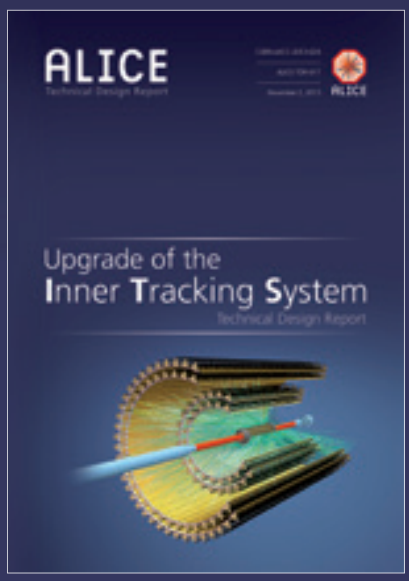

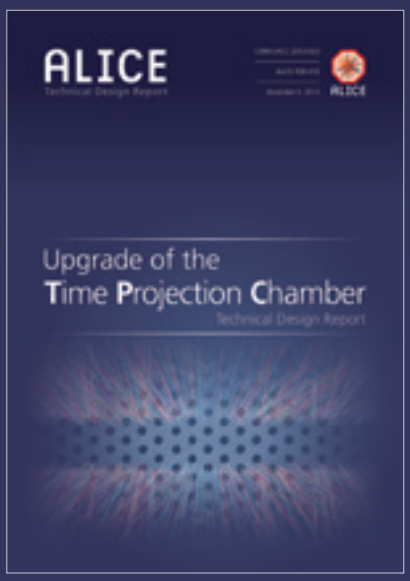

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