



Contribution to the Development of the LHCb Vertex Locator Readout Electronics

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Abstract

The LHCb experiment is being built at the future LHC accelerator at CERN. It is a forward single-arm spectrometer dedicated to precision measurements of CP violation and rare decays in the b quark sector. Presently it is finishing its R&D and final design stage. The construction already started for the magnet and calorimeters.

In the Standard Model, CP violation arises via the complex phase of the 3×3 CKM (Cabibbo-Kobayashi-Maskawa) quark mixing matrix. The LHCb experiment will test the unitarity of this matrix by measuring in several theoretically unrelated ways all angles and sides of the so-called "unitary triangle". This will allow to over-constrain the model and - hopefully - to exhibit inconsistencies which will be a signal of physics beyond the Standard Model.

The Vertex reconstruction is a fundamental requirement for the LHCb experiment. Displaced secondary vertices are a distinctive feature of b-hadron decays. This signature is used in the LHCb topology trigger. The Vertex Locator (VeLo) has to provide precise measurements of track coordinates close to the interaction region. These are used to reconstruct production and decay vertices of beauty-hadrons and to provide accurate measurements of their decay lifetimes.

The Vertex Locator electronics is an essential part of the data acquisition system and must conform to the overall LHCb electronics specification. The design of the electronics must maximize the signal to noise ratio in order to achieve the best tracking reconstruction performance in the detector. The electronics is being designed in parallel with the silicon detector development and went through several prototyping phases, which are described in this thesis.

Résumé

L'expérience LHCb sera installée sur le futur accélérateur LHC du CERN. LHCb est un spectromètre à un bras consacré aux mesures de précision de la violation CP et à l'étude des désintégrations rares des particules qui contiennent un quark b. Actuellement LHCb se trouve dans la phase finale de recherche et développement et de conception. La construction a déjà commencé pour l'aimant et les calorimètres.

Dans le Modèle Standard, la violation CP est causée par une phase complexe dans la matrice 3×3 CKM (Cabibbo-Kobayashi-Maskawa) de mélange des quarks. L'expérience LHCb compte utiliser les mesons B pour tester l'unitarité de cette matrice, en mesurant de diverses manières indépendantes tous les angles et côtés du "triangle d'unitarité". Cela permettra de surdéterminer le modèle et, peut-être, de mettre en évidence des incohérences qui seraient le signal de l'existence d'une physique au-delà du Modèle Standard.

La reconstruction du vertex de désintégration des particules est une condition fondamentale pour l'expérience LHCb. La présence d'un vertex secondaire déplacé est une signature de la désintégration de particules avec un quark b. Cette signature est utilisée dans le trigger topologique du LHCb. Le Vertex Locator (VeLo) doit fournir des mesures précises de coordonnées de passage des traces près de la région d'interaction. Ces points sont ensuite utilisés pour reconstruire les trajectoires des particules et l'identification des vertices secondaires et la mesure des temps de vie des hadrons avec quark b.

L'électronique du VeLo est une partie essentielle du système d'acquisition de données et doit se conformer aux spécifications de l'électronique de LHCb. La conception des circuits doit maximiser le rapport signal/bruit pour obtenir la meilleure performance de reconstruction des traces dans le détecteur. L'électronique, conçue en parallèle avec le développement du détecteur de silicium, a parcouru plusieurs phases de "prototyping" décrites dans cette thèse.

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1 Introduction

1.1 Matter and antimatter

It is generally believed that our World is stable and made of matter. Where all antimatter disappeared after a Big Bang that created an equal mixture of matter and antimatter?

A possible explanation [1] is that an asymmetrical behaviour of particle and antiparticle, so called symmetry violation or CP (Charge conjugation / Parity) violation - the mysterious phenomena discovered in neutral kaon decays in 1964 [2], was at the origin of the slight matter-antimatter disequilibrium, necessary for the present dominance of matter over antimatter in the World.

The present Standard Model (SM) of the world of elementary particles can naturally generate CP violation. It was firmly established in neutral kaon decays and recently in the B-meson decays - the area, where a new generation of experiments opened a new phase of CP violation research. The SM, however, does not seem to be capable of generating a sufficient amount of CP violation to explain the observed dominance of matter. This calls for new sources of CP violation beyond the Standard Model which contribute or even fully accounts for the observed phenomena. CP violation is therefore a highly interesting place to look for evidence for new physics [3].

In the Standard Model, CP violation is described in the framework of the 3x3 complex unitary mass-mixing matrix (CKM matrix), which can be described by four independent parameters. These four parameters of the CKM matrix will be well determined with a small theoretical uncertainty within the framework of the Standard Model by ongoing experiments (BABAR, BELLE, CDF)

The Large Hadron Collider (LHC) at CERN is the new scientific instrument, a gigantic microscope to study invisible. It offers the opportunity to study CP violation with sufficient precision to isolate the contribution from a possible New Physics and to understand its nature.

1.2 CERN and LHC

CERN, the European Laboratory for Particle Physics near Geneva, created in 1954, provides the experimental facilities required to advance our knowledge of the universe, matter and the fundamental laws of the nature. The scientific research done at CERN not only contributes to particle physics but also to many other fields. These include vacuum technology, superconducting magnets, computing, cryogenics and electrical, electronics civil and mechanical engineering just to mention a few.

The Large Hadron Collider - the CERN next particle accelerator - allows to explore physics up to the TeV scale [4]. This is a 27 km circumference high luminosity proton-proton collider being built in the present LEP tunnel reusing CERN accelerator complex. It will accelerate two proton beams to the total energy of 14 TeV with a design luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$.

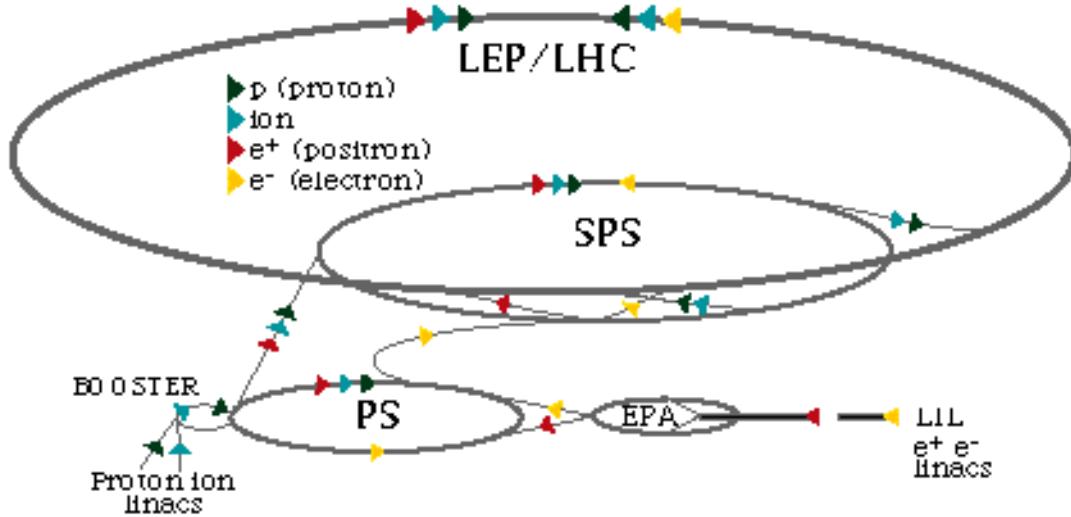
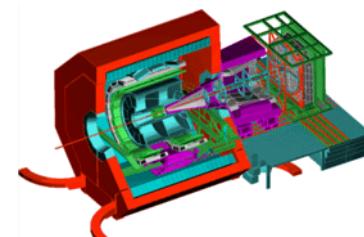


Figure 1 The CERN accelerator complex.

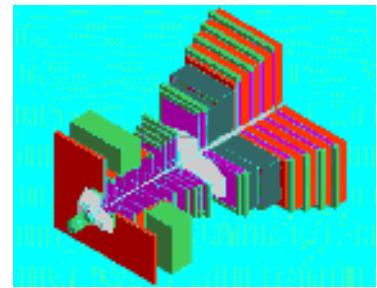
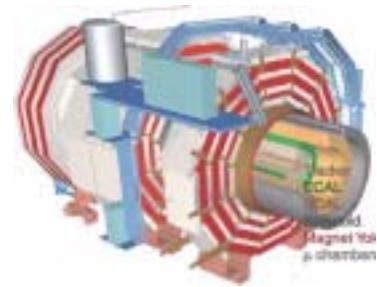
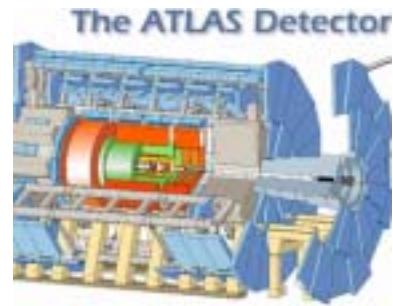
The proton beams are accelerated in a linear accelerator at the Meyrin site (*Linac*) up to 50 MeV. Then two circular accelerators boost them to 1 GeV (*Booster*) and 26 GeV (*PS*) before they enter the Super Proton Synchrotron (*SPS*). There they reach an energy of 450 GeV and enter the LHC via two new tunnels. The final energy of 7 TeV is limited by the magnetic field in the super-conducting magnets.

Four experiments have been approved for the LHC accelerator and will be installed at the intersecting points of the LHC:

- The ALICE (A Large Ion Collider Experiment) Collaboration will build a dedicated heavy-ion detector to exploit the nucleus-nucleus interactions at LHC energies [7]. The aim is to study the physics of strongly interacting matter at extreme energy densities, where the formation of a new phase of matter, the quark-gluon plasma, is expected. The existence of such a phase and its properties are a key issue in QCD for the understanding of confinement and chiral-symmetry restoration. For this purpose, the collaboration intends to carry out a comprehensive study of the hadrons, electrons, muons and photons produced in the collision of heavy nuclei. The experiment is designed to cope with the highest particle multiplicities anticipated for Pb-Pb reactions.



- The ATLAS (A Toroidal Lhc ApparatuS) Collaboration [6] proposes to build a general-purpose pp detector which is designed to exploit the full discovery potential of the LHC, among which the origin of mass at the electroweak scale. The detector optimization is therefore guided by physics issues such as sensitivity to the largest possible Higgs mass range. Other important goals are the searches for heavy W and Z-like objects, the super symmetric particles, the components of the fundamental fermions and detailed studies of the top quark. The primary goal is to operate at high luminosity, but the detector is conceived to assure performance in the full operational range of LHC. The investigation of CP violation in B-decays will be part of the addressed topics as well. ATLAS is planned to run also in heavy ion mode, searching for some rare processes.
- The CMS (Compact Muon Solenoid) detector has been designed to detect cleanly the various signatures for new physics by identifying and precisely measuring muons, electrons and photons over a large energy range and at high luminosity [5]. The key features that enable CMS detector to reach the challenges are an electromagnetic calorimeter with excellent energy resolution, efficient tracking at high luminosity for lepton momentum measurements, b-quark tagging and for electron and photon identification as well as tau and heavy-flavour vertexing, muon momentum measurement up to highest luminosity. CMS could be competitive as well for B-physics in some particular channels. The detector will also be used to detect low momentum muons produced in heavy ion collisions.
- The LHCb experiment is a forward detector which will study CP violation and other rare phenomena in the decays of Beauty particles [8]. At the LHC the produced B-mesons are correlated in rapidity and are typically forward, hence a forward spectrometer covering the angular region below 400 mrd would have all the decay product of the B-mesons in its acceptance for roughly (10-15)% of all Beauty events. LHC will operate at a luminosity much reduced compared with the maximum luminosity available to exploit only beam crossing with single interactions. Its main goal is to measure all angles of the unitary triangles in many different ways, over-constraining the CKM matrix including higher order terms and thereby searching for an inconsistency in the CKM picture that would reveal new physics. It will be described in more details in the following section.



1.3 Overview of LHCb experiment

Requirements

The production cross section of the $b\bar{b}$ quark pairs at the LHC energy is estimated to be $\sim 500 \mu b$, larger than at any existing machines. The fraction of events with b quarks, $\sigma_{b\bar{b}}/\sigma_{\text{inelastic}}$, is about 6×10^{-3} which is similar to the fraction of charm events in the present fixed-target charm experiments. Thus, LHC appears to be a very promising place to perform high precision CP violation measurements in B -meson decays. At LHC, B_s , \bar{B}_s , B_c^\pm and b -baryons are abundantly produced, in addition to B^\pm , B^0 and \bar{B}^0 .

The goal of B physics in the LHC era, is to determine the CKM parameters in a model-independent way and to isolate the effect of New Physics so that its characteristics could be identified. This calls for a high statistics experiment capable of studying CP violation with both B^0 and B_s^0 systems decaying into various final states, including those with only hadrons. In order to exploit the potential of LHC, experiments need to have the following capabilities:

- Trigger sensitive to both leptonic and hadronic final states.
- Particle identification system capable of identifying p , K , π , μ and e within the required momentum range.
- Vertex detector able to reconstruct primary and b -hadron vertices very precisely.
- Tracking system with good momentum resolution.

In addition, a capability of reconstructing π^0 would enhance the potential of the experiment further. The LHCb spectrometer [9] is designed to fulfil these requirements. It is also important to note that the detector covers a region of phase space which is not looked at by the two general purpose detectors, ATLAS and CMS.

Apparatus

The layout of the LHCb detector¹ shown in Figure 2 resembles a typical fixed target spectrometer due to its forward geometry. LHCb consists of a vertex detector at the intersection point (placed in "Roman Pots"), a tracking system, Ring Imaging Cherenkov Counters with aerogel and gas radiators, a large-gap dipole magnet, a calorimeter system, and a muon system. An existing LEP experimental area is reused to install the detector. The interaction point is shifted by 11 m from the nominal point, the centre of the experimental hall, in order to accommodate the detector elements without extra excavation.

1. A redesign of some components of the LHCb is going on and will be finalised after the end of this thesis ("LHCb light"); unless otherwise specified, in this work the LHCb layout from the Technical Proposal [8] (LHCb TP) is described.

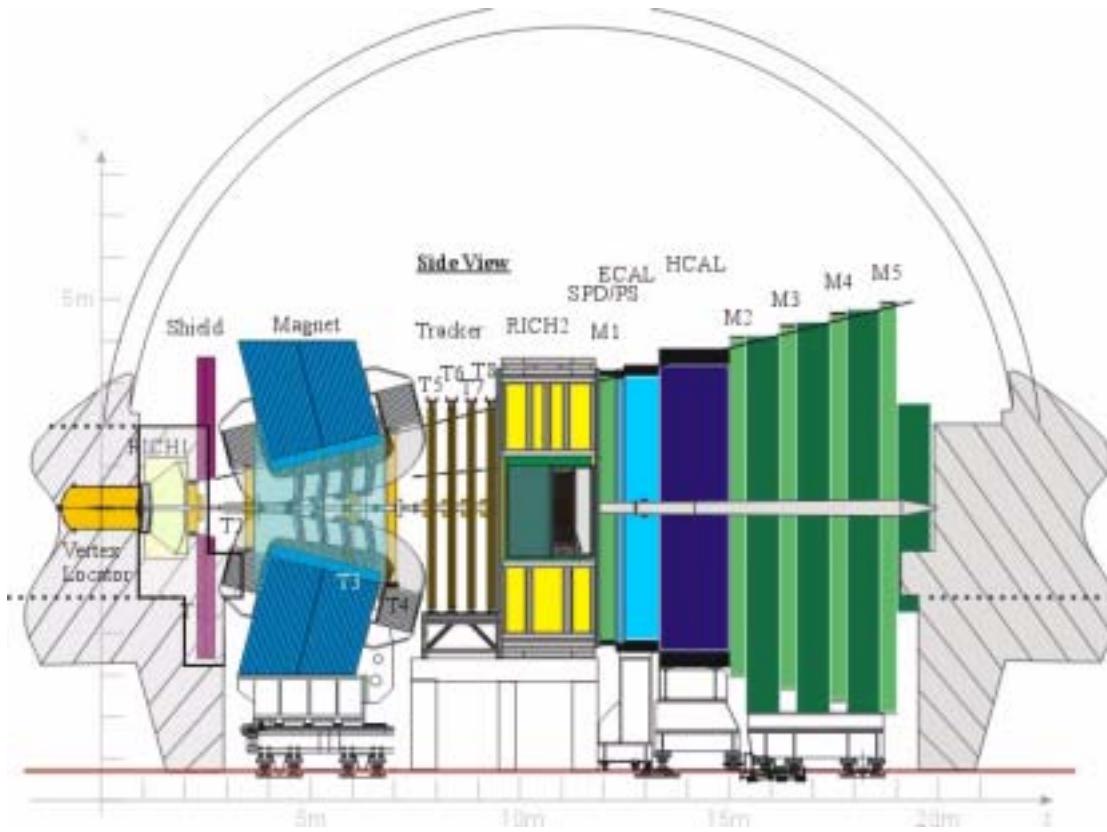


Figure 2 The LHCb spectrometer in the experimental area.

The choice of the detector geometry is based on the fact that both the b- and \bar{b} -hadrons are predominantly produced in the same forward (or backward) cone at high energies. Further advantages of the forward geometry are:

- The b-hadrons produced in the forward direction are faster than those in the central region. Their average momentum is about 80 GeV/c, corresponding to a mean decay length of 7 mm. Therefore, a good decay time resolution can be obtained for reconstructed b-hadrons.
- The spectrometer can be built in an open geometry with an interaction region which is not surrounded by all the detector elements. This allows a vertex detector system to be built with sensors which can be extracted away from the beam during the injection using Roman Pot technique. During the data taking, the sensors are positioned close to the beam in order to achieve a good vertex resolution.
- In the forward region, momenta are mainly carried by the longitudinal components. Therefore, the threshold values for the p_T triggers can be set low for electrons, muons and hadrons without being constrained by the detector requirements. This makes the p_T triggers more efficient than in the central region.

- The momentum range required for particle identification is well matched to the Ring Imaging Cherenkov (RICH) technique. The required size for the RICH counters remains affordable.
- The open geometry allows easy installation, maintenance and possible upgrade.

Beam Pipe

A large vacuum tank with a length of 1.7 m and a diameter of 1 m is placed around the interaction point to accommodate the vertex detector system with its retraction mechanics. It has a 2 mm thick Al forward exit window over the full detector acceptance. This part is followed by two conical sections: the first one is 1.4 m long with a 25 mrad opening angle, and the second part is 16 m long with a 10 mrad opening angle.

Except for bellows and flanges and the last 6.3 m of the 10 mrad cone, the beam pipe is made of Al-Be alloy in order to reduce the radiation length. This is essential for minimising the occupancies of the tracking and RICH systems, as well as for the detection of photons and electrons. Due to mechanical and safety reasons, flanges and bellows are made of Al. The beam pipe section in the region of the calorimeters and muon system is no longer important for the detection of electrons and photons. It is surrounded by shielding material, thus generating background particles is no longer an issue. Therefore, stainless steel is used for this section.

Magnet

A dipole magnet with Al conductor provides a field integral of 4 Tm. The polarity of the field can be changed to reduce systematic errors in the CP-violation measurements that could result from a left-right asymmetry of the detector. The two pole faces form a wedge shape following the spectrometer acceptance, in order to reduce the power consumption to 42 MW. The yoke of the magnet weights 1.5 kt and consists of many iron plates assembled together. The magnet assembly will take place in the experimental area.

Vertex Locator

A total of 27 stations of silicon microstrip detectors are placed perpendicular to the beam of which 25 stations are used as a vertex detector system (VErtex LOcator, VELO [10], 21 stations in the “LHCb light” layout). The remaining two stations are dedicated for detecting bunch crossings with more than one pp interaction as part of the Level-0 trigger (pile-up veto counter).

Stations are split into two halves, covering the left and right 180^0 sections. Each vertex detector station consists of two Si sensor planes with different strip layouts, one for r and the other for ϕ measurements. There are about 200'000 strips in total with varying sizes so that the occupancy remains below 1% everywhere. The pile-up veto counter has only r -measuring sensors. The closest distance between the active silicon area and the beam is 8 mm.

In order to cope with high radiation dose expected at this position so close to the beam, n-on-n silicon sensors are taken as baseline. The silicon detectors are placed in Roman Pots with $250\ \mu\text{m}$ thick aluminium foil, which acts as a shield against RF pickup of the circulating beam bunches. In order to avoid explosion, a secondary vacuum is maintained inside the Roman Pots.

During the injection and acceleration, the Roman Pot system will be moved away from the beam to avoid interference with the machine operation and accidental irradiation of the detectors.

Tracking

Because of the high particle density close to the beam pipe, the LHCb tracking detector is split into inner and outer systems. The boundary between the two was chosen so that the occupancy of the outer tracker does not exceed 15% at the highest point.

The outer tracking system uses drift chambers based on a straw cells structure. Straws are made by winding the carbon-loaded Kapton foil. The diameter of the straw is 5 mm and drift-time is sampled over 50 ns, i.e. two bunch crossings.

The inner tracking system is made from single sided p-on-n Si strip detectors with a strip pitch of $\sim 200\ \mu\text{m}$. Since the sensitive regions of the Si sensor are further away from the beam (several centimetres) compared with the sensors of the Vertex Locator, the problem of radiation damage is less severe.

RICH

The RICH system of the LHCb detector consists of two detectors with three different radiators in order to cover the required momentum range, 1-100 GeV/c. The first detector uses aerogel and C_4F_{10} gas as radiators. The second detector, design to identify high momentum particles, is placed after the magnet and uses CF_4 as radiator. The Cherenkov light is detected with planes of Hybrid Photon Detectors (HPD's) placed outside the spectrometer acceptance.

Calorimeters

The calorimeter system consists of a preshower detector followed by electromagnetic and hadronic calorimeters. The primary function of the calorimeter system is to provide single-particle energy information to the Level-0 trigger. It is also used in offline to reconstruct π^0 from B meson decays. It serves as the initial part of the muon filter system. The cells of the Preshower detector are made as two scintillator plates sandwiching a 14 mm-thick lead plate. The cell size of the preshower detector is matched to the module size of the electromagnetic calorimeter.

The hadron calorimeter is based on a scintillating tile design similar to that used in the ATLAS experiment with a reduced energy resolution of $\sim 80\%$. It is 6.8 m tall, 8.4 m wide and 165.5 cm long corresponding to $5.6\ \lambda_L$. There are only two cell sizes for the hadron calorimeter modules; $13 \times 13\ \text{cm}^2$ and $26 \times 26\ \text{cm}^2$.

For the electromagnetic part, a Shashlik calorimeter is used since a modest energy resolution of $\sim 10\%$ is needed. It is 6.3 m tall, 7.8 m wide and 83.5 cm long corresponding to $25 X_0$. The cell size of a module changes from $4 \times 4 \text{ cm}^2$ in the zone closest to the beam pipe, to $6 \times 6 \text{ cm}^2$ in the intermediate zone, and to $12 \times 12 \text{ cm}^2$ in the outer most zone, minimizing the number of modules without deteriorating the performance.

Muon

The muon system consists of four layers of hadron absorbers and five muon stations. The first station is placed in front of the first absorber layer, which is the calorimeter system. The three other absorbers are made of iron plates, each of them 80 cm thick. Three muon stations are placed between the absorbers and the fifth muon station is placed behind the last absorber, shielded with $20 \lambda_I$ of material. A smaller shielding plate behind the last station protects the chambers from the particles produced by the proton beam in the accelerator.

In the LHCb Technical Proposal Resistive Plate Chambers are used in the region where the charged particle rate is below 1 kHz/cm^2 . In the region with a charged particle rate from 1 kHz/cm^2 to 100 kHz/cm^2 , Multi Wire Proportional Chambers (MWPC's) are used. In the small region of the first muon station close to the beam pipe, where the charged particle rate exceeds 100 kHz/cm^2 , triple-GEM chambers or MWPC's with asymmetric gas gap are being considered.

Trigger system

The LHCb trigger is based on four decision levels. Due to the large mass and the transverse momentum spectrum of the B-meson, its decay products have on average higher p_T than particles produced in most of the inelastic pp interactions (minimum-bias events). Decay products of the B-meson originate from vertices that are displaced from the primary interaction point by several millimetres. The early levels of the LHCb trigger exploit those two characteristics.

Level-0 trigger decision is based on high- p_T hadrons or electrons found in the calorimeter system or muons found in the muon system. In addition, the pile-up veto counter detects bunch crossings with more than one pp interaction. Level-0 trigger provides a modest reduction of minimum-bias events by a factor of ~ 10 .

At Level-1, data from the Vertex Locator are used to select events with multiple vertices. Level-1 trigger provides a reduction factor of ~ 25 for minimum-bias events. After a positive decision of the Level-1, whole LHCb data are read out to an event buffer in the CPU farm.

At Level-2 and Level-3 (or High Level Triggers) a further enhancement of events with b-hadrons is achieved by combining data from different detector components and reconstructing the full event for the decay modes of interest.

2 LHCb electronics, trigger and data acquisition

The LHCb electronics is divided in Level-0 and Level-1 electronics. The Level-0 electronics is located in the cavern on or near the detector while the most of the Level-1 electronics is located in the counting room as well as the trigger and the Data Acquisition (DAQ) systems. A simplified diagram of the LHCb electronics, trigger and DAQ systems is shown on Figure 3.

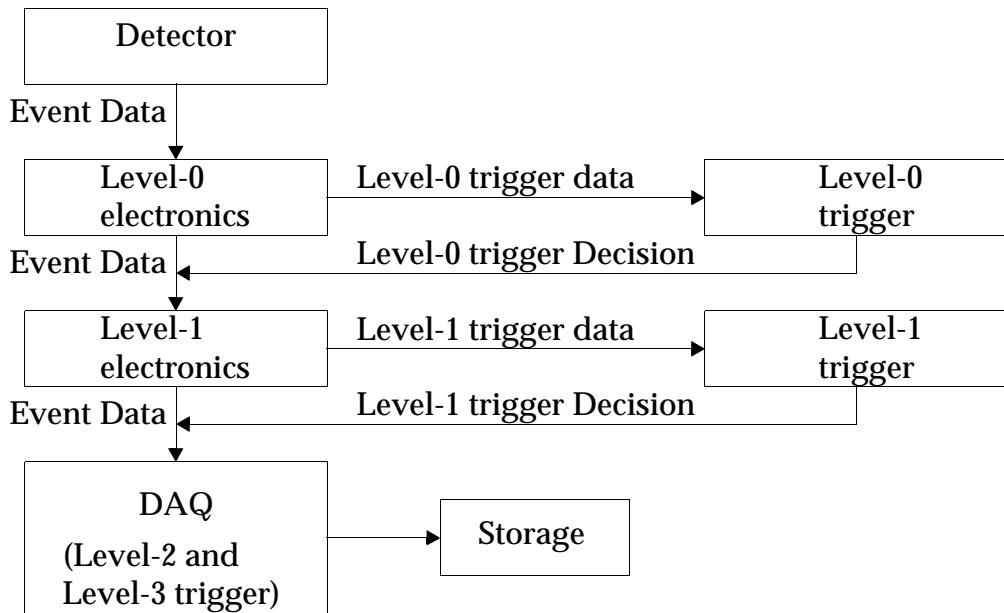


Figure 3 LHCb electronics, trigger and DAQ.

The Level-0 electronics of calorimeter and muon sub-detectors and the pile-up veto counter supplies data for the Level-0 trigger. During Level-0 trigger latency event data are kept in the pipelines of the Level-0 electronics. Data for events, accepted by the Level-0 trigger, are moved to the Level-1 electronics.

The Level-1 electronics of the Vertex Locator supplies data for the Level-1 trigger. During Level-1 trigger latency event data are kept in the Level-1 buffers of the Level-1 electronics. Upon positive trigger decision, data from the Level-1 electronics are collected by the DAQ system and made available for the Level-2 and Level-3 triggers. Finally selected events are stored for the off-line analysis.

The overall control of the LHCb electronics, trigger and DAQ system is performed by the TFC (Timing and Fast Control) system and the ECS (Experiment Control System) of the LHCb experiment.

In the following sections the individual parts of the LHCb electronics, trigger, DAQ and control systems will be described in more details.

2.1 Level-0 electronics

The Level-0 electronics [11] must correctly capture and store detector signals, from particles generated by the bunch collisions of the LHC machine on a large number (~1 million) of electronic channels. The detector signals must be captured with sufficient time resolution, to determine the exact bunch crossing from which the particles originate. Captured data (analogue or digital) must be stored in the Level-0 electronics pipeline buffer, until the Level-0 trigger decision accepts or rejects data from a given bunch crossing. Accepted data must be extracted from the pipeline buffer and temporarily stored in the Level-0 derandomizer buffer, waiting to be transferred to the Level-1 electronics

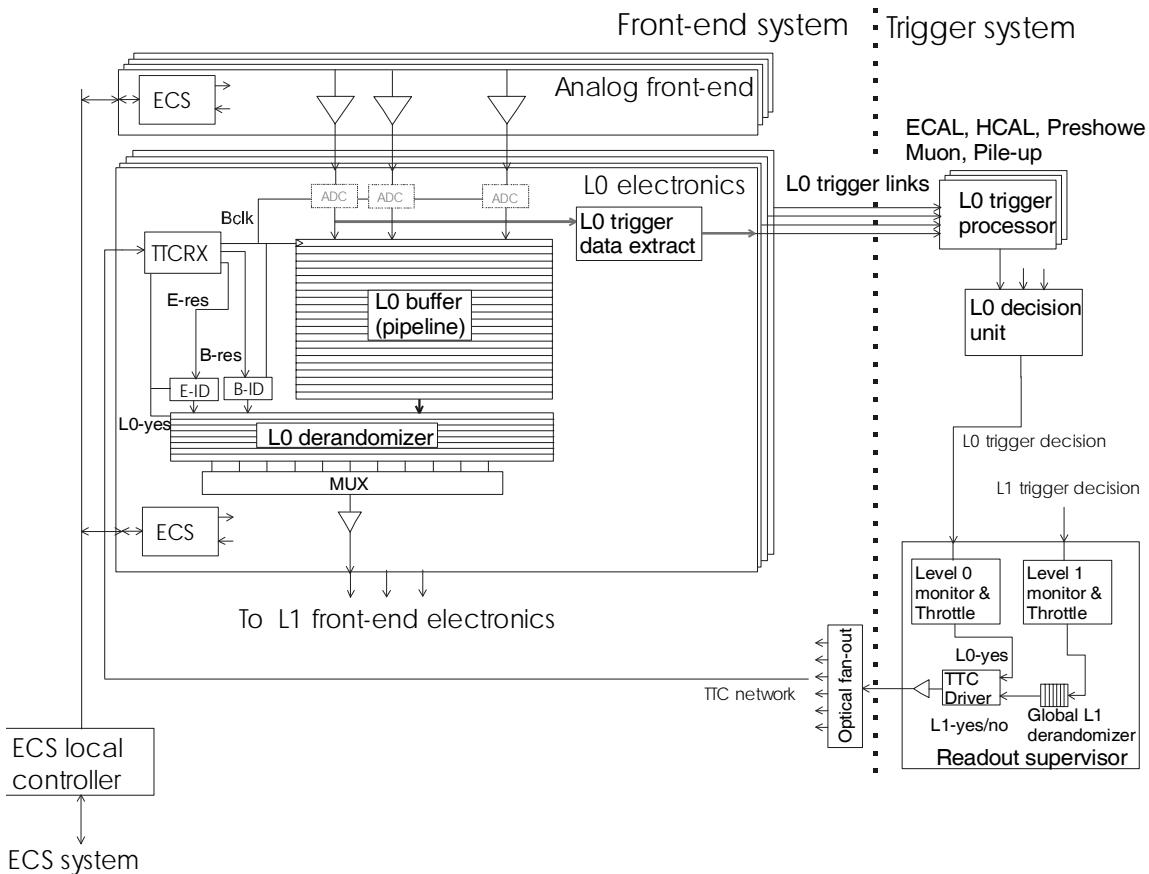


Figure 4 General architecture of the Level-0 electronics (from [11]).

A predictable behaviour of the Level-0 electronics system is of special importance in the LHCb experiment, because of the high bunch crossing rate (40 MHz) and the relatively high trigger rates. All electronics must be perfectly synchronised to the beam crossings, to insure correct capture of detector signals. The arrival of the Level-0 trigger-accept to the Level-0 electronics must also be in perfect synchronisation, to insure the extraction of correct event data from the Level-0 pipeline. Caused by the relative high Level-0 trigger accept rate, event data from the Level-0 pipeline must be temporarily stored in a derandomizer

buffer before being transferred to the Level-1 electronics. The size of this derandomizer buffer, and the speed of which data can be transferred to the Level-1 buffer, is a major bottleneck in the LHCb electronics that has a significant impact on the physics performance of the experiment. The Level-0 trigger accept rate must be limited centrally, based on an emulation of the Level-0 derandomizer buffers. For such a scheme to work in a reliable way for a large system, it is required that the Level-0 pipelines and the Level-0 derandomizers work in perfect synchronisation across the whole experiment. Otherwise one would have to reduce the Level-0 trigger rate significantly, to insure that no buffers overflow in any part of the electronics, or build a very large and fast signalling network which could throttle the Level-0 trigger, when any electronics buffer risk to overflow.

The LHCb TFC system, based on TTC (Timing and Trigger Control) system [12] is used for the distribution of all time critical signals. The use of a common system for this ensures that the control of the different sub-detector electronics implementations have a unified interface with a predictable behaviour. The Readout Supervisor, that receives trigger decisions from the trigger systems, drives the TFC system. The Readout Supervisor (RS) is responsible for preventing buffer overflows in the LHCb electronics and DAQ systems. During testing, debugging and special calibrations each sub-detector is driven from a separate Readout Supervisor via the partitioning system of the TFC. During normal physics running all sub-detectors are driven from one common central Readout Supervisor.

In the large and complex electronics system, consisting of several completely different implementations for different sub-detectors, it is also important to define a set of error checking and monitoring features. These kinds of functions are vital to insure that data collected from the experiment can be considered correct, with a sufficient confidence level, when working in a hostile environment (radiation). The control, monitoring, and verification of the LHCb electronics is performed by the LHCb ECS [13]. The global ECS system will communicate with the LHCb electronics via the ECS interfaces. The ECS interface to the electronics has been standardized, to insure a consistent control and monitoring system.

The Level-0 electronics is in general located very close to the detector, either inside the sub-detector itself or on its close periphery. Electronics located inside a sub-detector can only be accessed for service or repair during the long shutdown periods of the LHC machine once per year (may in exceptional cases be accessed to perform limited repairs). Electronics located outside the detector can be accessed on a regular basis for simple repairs and service. If standard commercial components are used in the Level-0 electronics, it must be located in places with low radiation levels (less than 10 krad total dose during 10 years) and the system must be verified to work correctly after realistic radiation doses. In locations with higher radiation levels special radiation hard/tolerant components must be used which have been qualified with appropriate procedures. Integrated circuits must be verified to be immune to single event latch-up (possibly destructive) in the given application.

The effects of Single Event Upsets (SEU) on the reliability of the electronics must be evaluated and the detection and recovery from such failures must be considered. The specific problems related to SEU effects on configuration data in FPGA's must be shown to be at an acceptable level. Especially the ECS interface of the Level-0 electronics must be shown to be immune to lockup states caused by SEU, as this interface is the only path available to recover normal functionality.

2.2 Level-1 electronics

The Level-1 electronics [14] is defined as the last stage of the sub-detector specific electronics, before data is sent to the common DAQ system. The general architecture of the Level-1 electronics is based on extensive simulation. The physical implementation of this architecture for different sub-detectors may look quite different, as long as it conforms to the defined requirements.

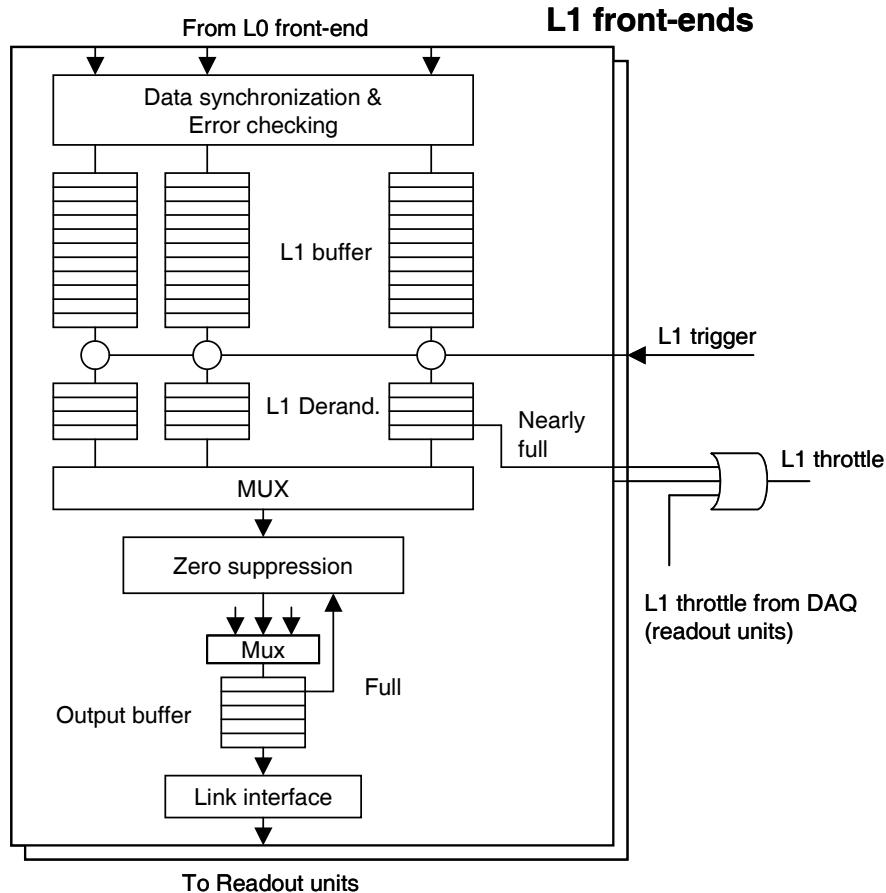


Figure 5 General architecture of the Level-1 electronics (from [14]).

Event data, accepted by the Level-0 trigger, is received from the Level-0 electronics on a set of sub-detector specific links (or internal data buses in the case the Level-0 and Level-1 electronics are housed on same board). If data have not yet been digitised, it must be converted into a proper digital format, as sensitive analogue data cannot be stored reliably during the relatively long Level-1 trigger latency. The data is stored in the Level-1 buffers, waiting for the Level-1 trigger decision to be distributed to the Level-1 electronics via the TFC system. Events accepted by the Level-1 trigger must be extracted from the Level-1 buffer, derandomized in the Level-1 derandomizer, zero-suppressed and finally formatted to be sent to the DAQ system on standardized (optical) links. In the DAQ system, event data is not assumed to be preprocessed before it arrives in the CPU's of the Level-2/Level-3 trigger processor farm, therefore, all sub-detector specific processing of detector data must be performed in the Level-1 electronics.

Buffers overflow prevention in the Level-1 electronics is made as a combination of central control and a hardwired Level-1 throttle signal. The Level-1 buffer occupancy is controlled and monitored centrally in the Readout Supervisor based on a set of strictly defined parameters. The Level-1 derandomizer overflow after the Level-1 accept are prevented by a hardwired Level-1 throttle signal, as local Level-1 derandomizer occupancies can not be predicted centrally when event data have been zero-suppressed. The Level-1 derandomizer handles the delay of the Level-1 throttle signal, and following data buffers are assumed to back-propagate their full status to the Level-1 derandomizer.

The ECS interface is needed to configure and initialize the Level-1 electronics before data taking. It is also vital for efficient monitoring of the correct function of the Level-1 electronics modules during data taking. A high level of controllability and observability of the modules will be required to perform efficient testing and debugging of the electronics during commissioning and debugging. As the ECS interface is the only path to control and monitor the Level-0 electronics it must have high reliability and it must be insured that it cannot get into a deadlock state where the control of the module is lost. The ECS interface must be capable of recovering the normal function of a module without the need of powering off and powering on the module.

2.3 Trigger system

The 25 ns bunch spacing at LHC implies that the pipeline of the Level-0 electronics will have to be clocked at 40 MHz. However, some of the bunch crossings in LHCb will involve empty bunches, reducing the bunch crossing rate to an effective average value of 30 MHz.

At high luminosity, several proton-proton interactions are expected in a single bunch crossing. However, LHCb is planning to reach its physics goal using only events with single interactions. This is motivated by radiation damage, detector occupancy, pattern recognition flavour tagging and trigger issues. The detector

will therefore be operated at a modest luminosity of $2 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$, (the beams will be defocused at the LHCb interaction point as the LHC machine gradually delivers its design luminosity of $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ to ATLAS and CMS). Under these conditions and assuming an inelastic cross section of 80 mb, 30% (10%) of the bunch crossings will have one (more than one) proton-proton interaction. In addition, a pile-up veto system is foreseen at the earliest trigger level to reject events with more than one interaction vertex, from the information provided by two dedicated silicon stations located upstream of the VELO detector. After this cut, the event rate is around 10 MHz with more than 90% single interactions.

The trigger scheme [15] will be implemented in four levels to selectively extract the B decays of interest while rejecting the non-b events. The lower level triggers (Level-0 and Level-1) will aim at rejecting non-b events. They will merely rely on two main features of the b-hadron decays: long lifetimes and significant transverse momentum release due to the high b-quark mass. The higher level triggers (Level 2 and 3) will consist of software algorithms running on farms of commercial computers and select specific $b\bar{b}$ events channels.

Level-0 Trigger

The first level of trigger, based on calorimeter and muon chamber information only, will reduce the event rate to 1 MHz by requiring a muon, an electron or a hadron with a transverse momentum (p_T) or energy (E_T) above some threshold, typically 1, 2.4 and 3.4 GeV respectively: tracks from b-hadron decays have indeed a harder p_T spectrum than tracks from non-b events. The fraction of the bandwidth attributed to the muon, electron and hadron triggers have been chosen to maximize the overall CP reach and will approximately be 20%, 10% and 60% respectively, the rest being allocated to other triggers (high E_T photon, dimuon, etc.). The Level-0 decision will take 4 μs during which the data will be kept in the pipeline of the Level-0 electronics.

Level-1 Trigger

The Level-1 trigger achieves a further reduction in rate by a factor of 25. It uses vertex detector information to identify secondary vertices produced by the b-hadron decays. Tracks are found from the hits in the VELO detector and a primary vertex is reconstructed. Secondary vertices are then formed with large impact parameter tracks. The Level-1 buffer will reside in the Level-1 electronics; its depth will allow for a maximum latency of the Level-1 trigger of 1.7 ms. After a Level-1 trigger accept, the zero-suppressed data are transferred to the data acquisition system and the full event data are available to the high level software triggers.

The overall layout of the Level-1 trigger system [16] is shown on Figure 6. It's a farm of processors connected by a low latency, shared memory network [17]. A two-dimensional torus network with distributed CPUs in the intersections is used. The torus is implemented as horizontal and vertical Scalable Coherent Interface (SCI) ringlets of 800 Mbyte/s bandwidth each [18]. The network congestion is avoided by destination address allocation and traffic scheduling.

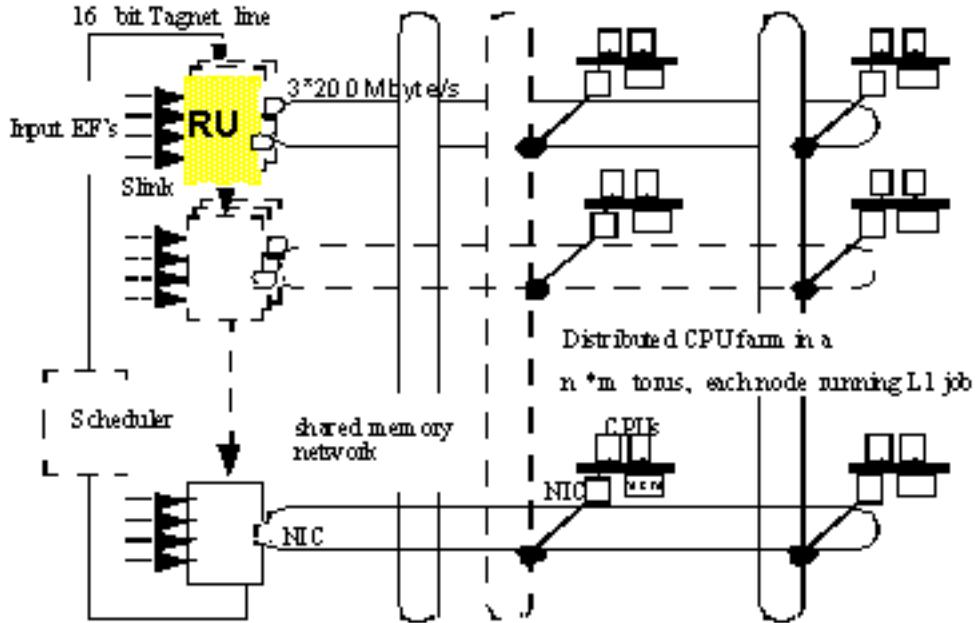


Figure 6 Level-1 trigger system layout.

High Level Triggers

Some secondary vertices found at Level-1 are fake due to low momentum tracks undergoing multiple scattering. The aim of the Level-2 trigger is to reconstruct large impact parameter tracks in the VELO and the first tracking chambers and use the momentum information to refine the secondary vertex requirement.

At Level-3, specific b-hadron decay modes will be reconstructed and selected with loose cuts using all available information. Approximately 200 events per second will be written to tape at a rate of 20 Mbytes/s.

2.4 Data acquisition system

The LHCb DAQ system [19] collects zero-suppressed data, belonging to one event, from the Level-1 electronics and assemble them in one CPU for execution of the high level trigger algorithms. It will have to cope with an average trigger rate of ~ 40 kHz, after two levels of hardware triggers, and an average event size of ~ 150 kB. Thus an event-building network which can sustain an average bandwidth of 6 GB/s is required. A powerful software trigger farm will have to be installed to reduce the rate from the 40 kHz to ~ 200 Hz of events written to permanent storage.

A overall architecture of LHCb electronics, trigger, DAQ and control systems is shown on Figure 7.

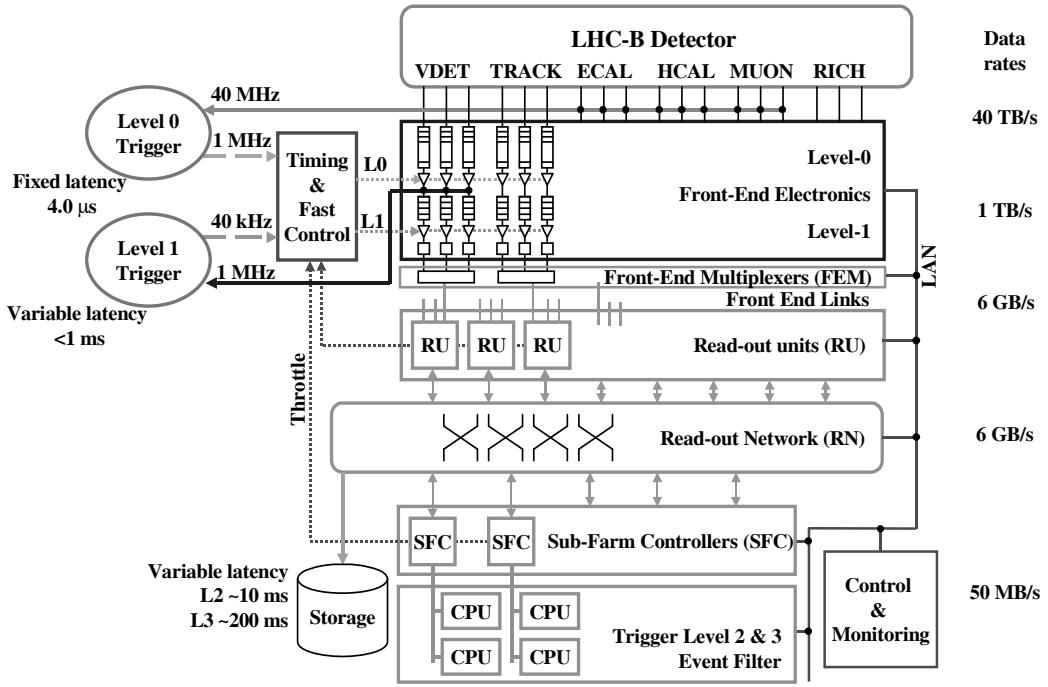


Figure 7 Trigger and DAQ architecture (from [19]).

The main functional components of the LHCb DAQ system are:

- The Readout Units (RU) acting as a multiplexer of Level-0 links and as a interface to the Readout Network (RN). The same basic module is used as interface to the Readout Network and also as a Level-0 Multiplexer,
- The Readout Network (RN) which provides support for event-building, i.e. assembling all event fragments buffered in the RUs in one place,
- Sub-Farm Controllers (SFC) which act as an interface between the RN and the processor farm, which will run the higher-level triggers (Level-2 and Level-3),
- CPU farm to execute the higher level trigger algorithms (Level-2 and Level-3).

The purpose of the Level-0 Multiplexer (FEM) is to aggregate the data fragments originating from many Level-1 electronics boards and which have very low data rates into bigger fragments with the final aim of reducing the number of links into the Readout Network and/or making better use of the single link bandwidth. The functionality of the Readout Units is in the first instance the same as that for the FEMs (Multiplexing/Data Merging). In addition the RUs are connected to the Readout Network. The Readout Network can, for certain technologies, suspend the sending of data to it, and hence block the RUs. This can lead to congestion in the RUs, which in turn entails significant buffering requirements for the RUs. Another functionality of the RUs is related to network technology choices. If the technology of the links to the RUs is different from the technology of the Readout Network, the RUs must perform the necessary

'protocol translation' between the two technologies. In the terms of network language they act as a gateway between the two technologies. A third feature required of the RUs has to do with the event-building process. Unlike the FEMs the RUs can send their data to more than one destination through the Readout Network. The fragments of a given event-number, however, should arrive at only one destination. Hence the RUs have to support the destination assignment mechanism.

There are two main functional requirements imposed on the Readout Network (RN): to provide the connectivity between the RUs and the Sub-Farm Controllers, such that each RU can communicate to any Sub-Farm Controller and to provide the necessary bandwidth, such that all data arriving in the RUs can be sent to the Sub-Farm Controllers with only minimal packet loss.

The Sub-Farm Controllers (SFC) fulfils three functionalities. Firstly they perform the final event building, i.e. the concatenation of the event-fragments originating from the RUs to form a complete event. Secondly, they are supposed to isolate the Readout Network and its technology from the network technology within the sub-farm. Again, this is a gateway like function, as for the RUs, in network terms. Finally, the SFCs are supposed to exercise a load balancing function among the CPUs connected to each sub-farm. An event can spend a very long time in a CPU if it is accepted by the trigger algorithms and has to be reconstructed. A simple minded round-robin scheduling would lead to high buffer occupancies in the SFC and uneven load in the sub-farm nodes. The SFCs are also responsible for collecting the finally accepted and reconstructed data from the CPUs connected to them and to send these data to the storage controller also connected to the Readout Network.

The protocol applied for transferring the data from one stage to the next is a push protocol, which means that any module or stage that has data available for transfer will push them to the next higher stage immediately, under the condition that the output port is able to execute the transfer. There is no synchronisation or communication neither between components of the same level or between components of different levels. This protocol assumes that there is always enough buffer space available in the destination module to receive the data. Should buffer space get scarce traffic control has to be exercised. This is done through a throttle signal to the TFC system, specifically to the Readout Supervisor, which will inhibit the sending of new data from the Level-1 Electronics, by issuing Level-1 "No" decisions until the throttle signal is de-asserted.

2.5 Timing and Fast Control system

The LHCb TFC system [20] distributes a common clock synchronous to the accelerator, the Level-0 and Level-1 decisions, resets and synchronization commands, bunch crossing number and event number to all components needing this information, such as Level-0/Level-1 electronics, trigger, etc.

Although the backbone of the timing, trigger and control distribution network is based on the CERN RD12 system (TTC), several components are specific to the LHCb experiment due to the fact that the LHCb trigger/DAQ system is different from that of the other experiments in several respects.

- The LHCb TFC system has to handle two levels of high-rate triggers: a Level-0 trigger with an accept rate of maximum 1.1 MHz and a Level-1 trigger with an accept rate of maximum 40-100 kHz.
- The TFC architecture has been designed with emphasis on partitioning. A partition is a configurable ensemble of parts of a sub-detector, an entire sub-detector or a combination of sub-detectors that can be run in parallel, independently and with a different timing, trigger and control configuration than any other partition.

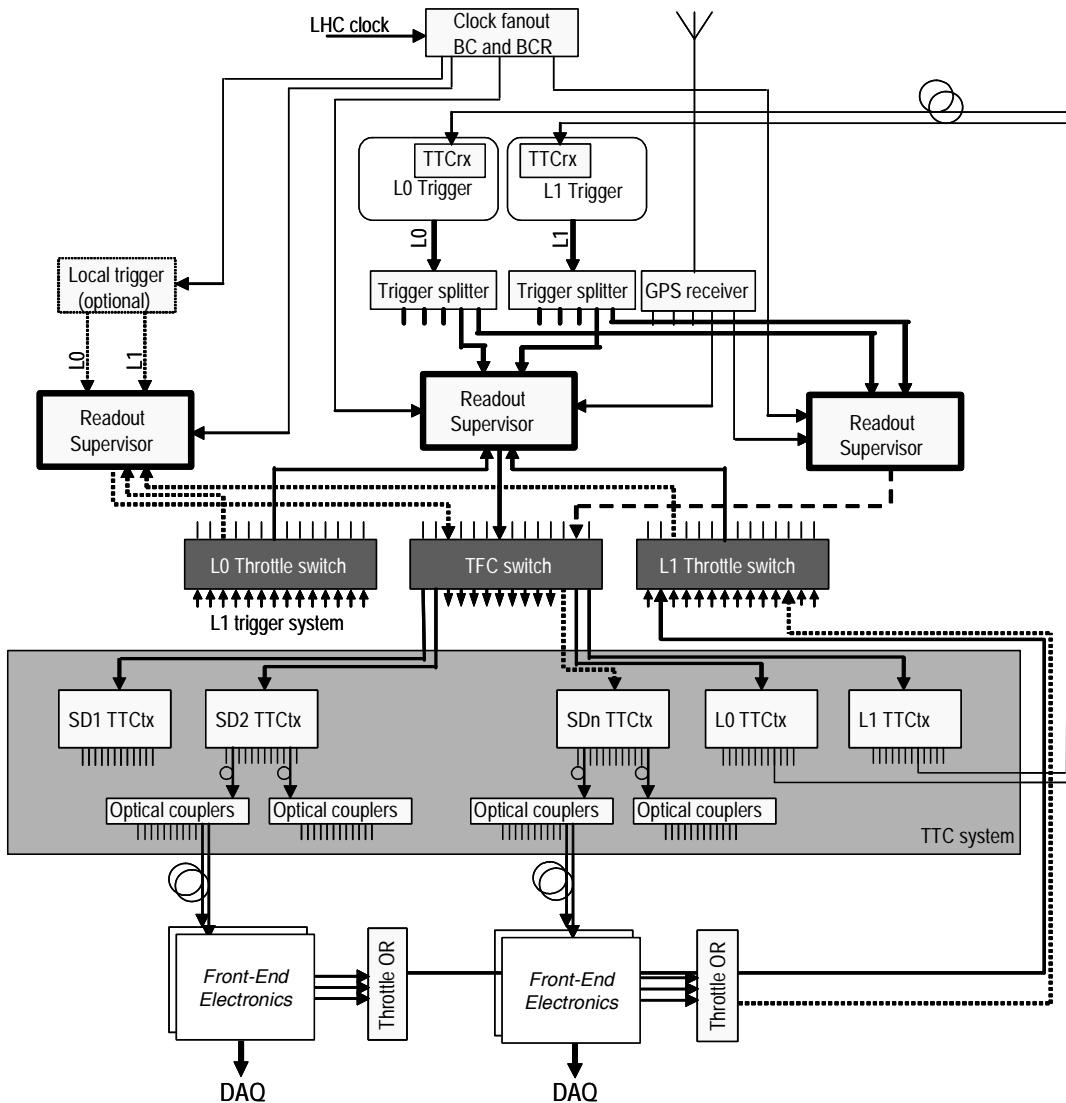


Figure 8 TFC architecture (from [20]).

Furthermore, the aim has been to locate the entire TFC mastership of a partition in a single module. The trigger decision units are also considered as sub-detectors.

The TFC architecture is shown in Figure 8. It incorporates a pool of Readout Supervisors, one of which is interfaced to the central trigger decision units and is used for normal data taking. The other Readout Supervisors are reserves and can be invoked for tests, calibrations and debugging of individual sub-detectors.

The TFC Switch distributes the TFC information to the LHCb electronics and the Throttle Switches feed back hardware throttle signals from the Level-1 trigger system, the Level-1 derandomizers and components in the data-driven part of the DAQ system, to the appropriate Readout Supervisors. The Throttle ORs form a logical OR of the throttle signals from sets of LHCb electronics. A GPS system allows time-stamping the local event information sampled in the Readout Supervisor.

2.6 Experiment Control System

The LHCb Experiment Control System, shown on Figure 9, is in charge of the control and monitoring of all experimental equipment. As such, it has to provide interfaces to all types of devices in the experiment and a framework for the integration of these various devices into a coherent complete system.

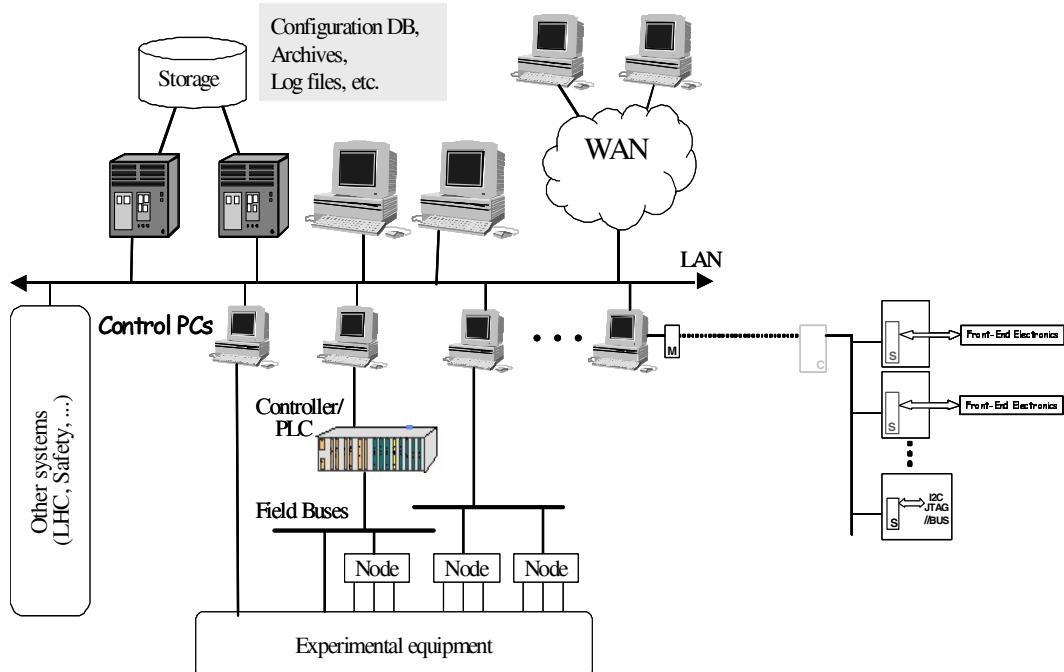


Figure 9 ECS architecture (from [13]).

Each component of the system, be it a electronics board, a high voltage channel or a physics algorithm in the PC farm, will have to be initialized, configured and monitored for different activities or running modes.

The control framework was developed following the specification provided by the Joint Control Project at CERN and based on the PVSS II SCADA system. The framework offers tools to implement a hierarchical control system.

The ECS interface is needed to configure and initialize the LHCb electronics before data taking. It is also vital for efficient monitoring of the correct function of the LHCb electronics modules during data taking. To insure a homogenous ECS system it has been agreed to limit the number of different ECS interfaces to a minimum. Three different ECS interfaces have been identified as viable solutions. For applications in areas with no radiation (underground counting room and surface buildings) a commercial Ethernet interface based on a Credit-Card PC (CC-PC, [21]) has been found to be an attractive solution. The local intelligence of this CC-PC can be used for local monitoring and verification of the correct function of an electronics or DAQ module.

The CC-PC (Figure 10) contains and Intel Pentium compatible CPU, up to 64 MB of memory and outputs directly I2C, JTAG and the PCI bus, which can be easily converted into a simpler parallel bus. These CC-PCs will probably run Linux and will be booted remotely via the network.



Figure 10 Credit-card PC.

In LHCb The CC-PCs will be used to provide the necessary local intelligence on an electronics board. They are connected to the central ECS via a conventional Ethernet and allow accessing the various components of the board.

3 VELO electronics development

3.1 VELO detector

Vertex reconstruction is a fundamental requirement for the LHCb experiment [10]. Displaced secondary vertices are a distinctive feature of b-hadron decays. The VErtex LLocator (VELO) has to provide precise measurements of track coordinates close to the interaction region. These are used to reconstruct production and decay vertices of beauty- and charm-hadrons, to provide an accurate measurement of their decay lifetimes, and to measure the impact parameter of particles used to tag their flavour. The VELO measurements are also a vital input to the Level-1 trigger, which enriches the b-decay content of the data. The VELO features a series of silicon stations placed along the beam direction. They are placed at a radial distance from the beam which is smaller than the aperture required by the LHC during injection and must therefore be retractable. This is achieved by mounting the detectors in a setup similar to Roman pot (Figure 11).

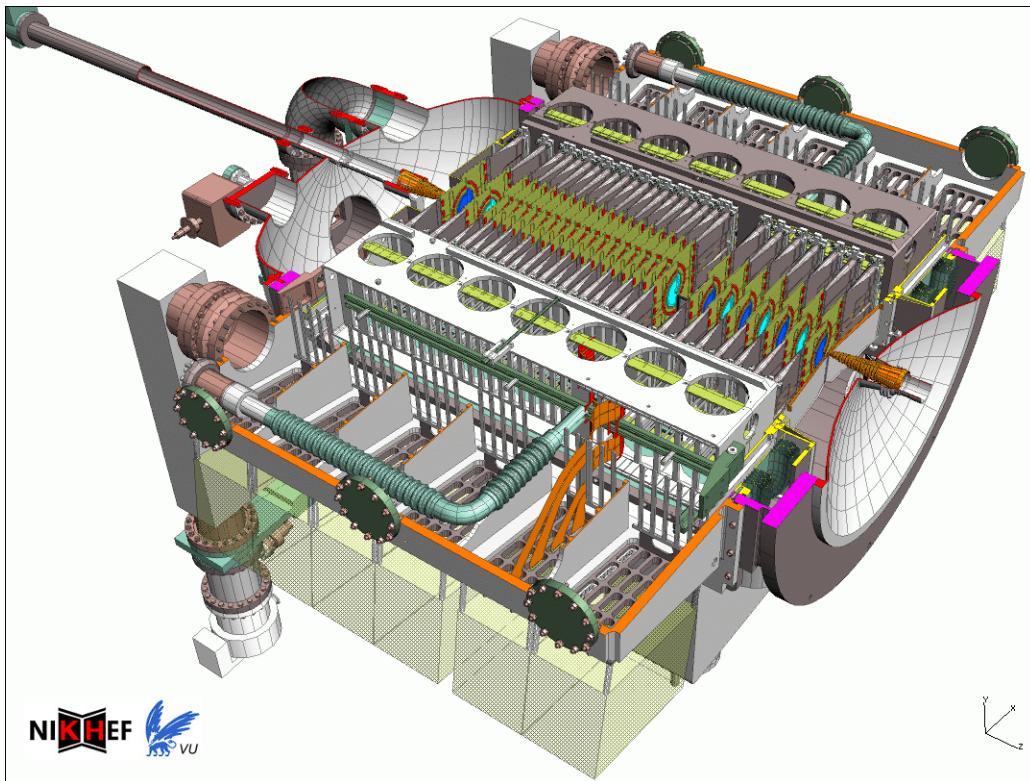


Figure 11 LHCb VELO detector.

Special requirements emerge from the use of the VELO information in the Level-1 trigger. The Level-1 algorithm requires a fast and stand-alone three-dimensional pattern recognition to distinguish b-events from those minimum bias events which are accepted by the Level-0 trigger. B-hadrons that have all their decay products within the acceptance of the spectrometer are typically produced with a polar angle below 200 mrad. Hence, the projection of the impact parameter of the decay products to the primary vertex in the rz -plane is large, while in the plane perpendicular to the beam-axis ($r\phi$) it is similar to that of tracks originating from the primary vertex. The Level-1 trigger exploits this by first reconstructing all tracks in the rz -projection, but reconstructing only tracks in three dimensions which have a significant rz -impact parameter. Hence, the strip pattern on the sensors has strips with constant radius for the rz -track reconstruction, combined with radial-strip sensors having a stereo angle of (10° - 20°) to allow the two projections to be combined.

3.1.1 VELO implementation

The VELO detector is composed of 25 (21 in “LHCb light”) parallel disk-shaped silicon strip detector stations as shown in Figure 12. To simplify the high impact parameter track search, the VELO is outside of the magnetic field (to have straight tracks) and measures the r and ϕ coordinates. This geometry allows the identification of high impact parameter tracks using only the r coordinate.

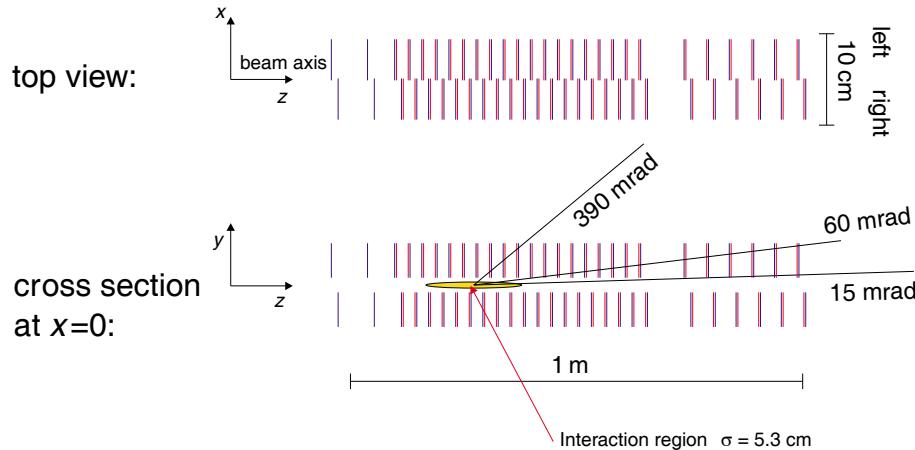


Figure 12 Arrangement of VELO sensors along beam axis.

The top figure shows the VELO setup seen from above, indicating the overlap between the left and right detector halves.

The bottom figure is a cross section of the setup at $x = 0$ along the beam axis showing also the nominal position of the interaction area. The three lines indicate the maximum and minimum angular coverage of the VELO and the average angle of tracks in minimum bias events respectively.

The silicon sensors have a circular shape, patterned with azimuthal (r measuring) or quasi-radial (ϕ measuring) strips, and span 182° . These views have been chosen in order to optimize the stand-alone tracking performance for the Level-1 trigger. By using a double metal layer, it is possible to decouple the routing of the signals from the strip geometry and to move the electronics as far as possible out of the acceptance. The innermost radius of the sensitive area is 8 mm and the outermost radius is approximately 42 mm.

The concept of the strip layout is illustrated in Figure 13. The strips in the ϕ -sensor are split into an inner and an outer region, chosen to equalize the occupancy in the two regions. The detectors are flipped from station to station, and the strips are tilted with a stereo angle, which is different in sign and magnitude for the inner and outer region. This results in a dog-leg shape, which minimizes the depth of the corrugations needed in the RF shield to accommodate the shape. The strips in the r -sensor are segmented into 4 (2) azimuthal sections in the inner (outer) regions. With this design it is possible to determine the primary vertex position in the plane perpendicular to the beam using the R -sensors alone, which is an important input to the Level-1 trigger. The pitch varies with radius, striking a balance between making the occupancy as uniform as possible, and ensuring that the first two points on the track are measured with the finest pitch available.

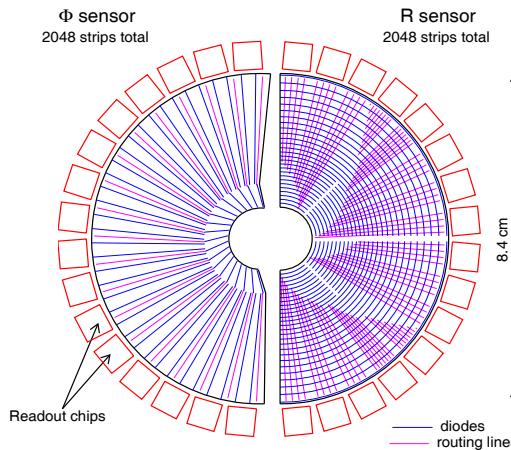


Figure 13 Schematic view of a r - and ϕ -measuring sensor.

The number of detector strips per sensor is kept as 2048. This leads to 16×128 channels Level-0 chips (see 3.2.1) per sensor which fit at a maximum sensor radius.

The VELO module provides the mechanical infrastructure to support the sensors rigidly, stably and in a known position. It acts as the base on which the electronic components for the sensor can be mounted. It also allows the removal of heat from the Level-0 chips and sensors. The key components of the module are: 2 silicon sensors, the Level-0 chips, mounted on a hybrid and the module support

with the cooling pipes. The module is designed to allow the precision alignment of the sensors relative to the platform on which all modules are mounted. A large vacuum vessel, supported by a concrete stand, encloses the complete detector array and support frames.

3.1.2 VELO experimental environment

The design of the VELO system, including VELO electronics, is constrained by its proximity to the LHC beams and its integration into the LHCb experiment. In the design of the VELO, the following boundary conditions are imposed:

- The need for shielding against RF pick-up from the LHC beams, and the need to protect the LHC vacuum from outgassing of the detector modules, requires a protection to be placed around the detector modules.
- The space, available around the VELO detector and radiation levels in the VELO location constrain the VELO Level-0 and Level-1 electronics implementation.
- Cooling of the detector modules is required since the sensors are operated in a high radiation environment. Harsh radiation environment also lead to the silicon sensor efficiency degradation and the sensors have to be replaced every three year. To allow for a replacement of the sensors in case of radiation damage, access has to be rather simple.
- The number of analog channels in the VELO is limited to about 200K channels. In particular, this is due to the limited space for the vacuum feedthroughs on the VELO vacuum vessel.

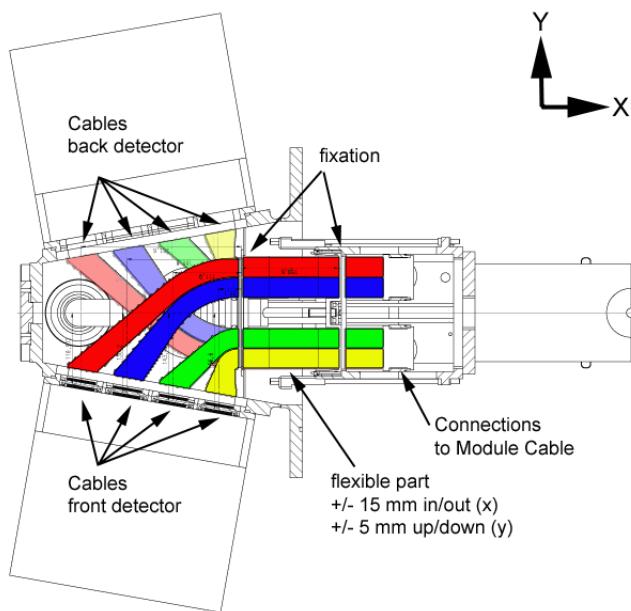


Figure 14 VELO cabling inside vacuum vessel.

Limited space around the vacuum vessel does not allow to place any Level-1 electronics close to the VELO detector. Radiation hard and flexible kapton flat cables transfer detector signals inside the vacuum vessel from the front-end chips on the VELO modules to the feedthroughs (Figure 14).

Outside of the vacuum vessel there are drivers for the signals from the front-end chips and receivers for the control signals. They are located on the repeater cards. Cables are traced from the VELO vicinity to the Level-1 electronics location.

Radiation levels in the LHCb cavern have been calculated with FLUKA99 [22]. The results are obtained for the experimental layout configuration shown in Figure 15.

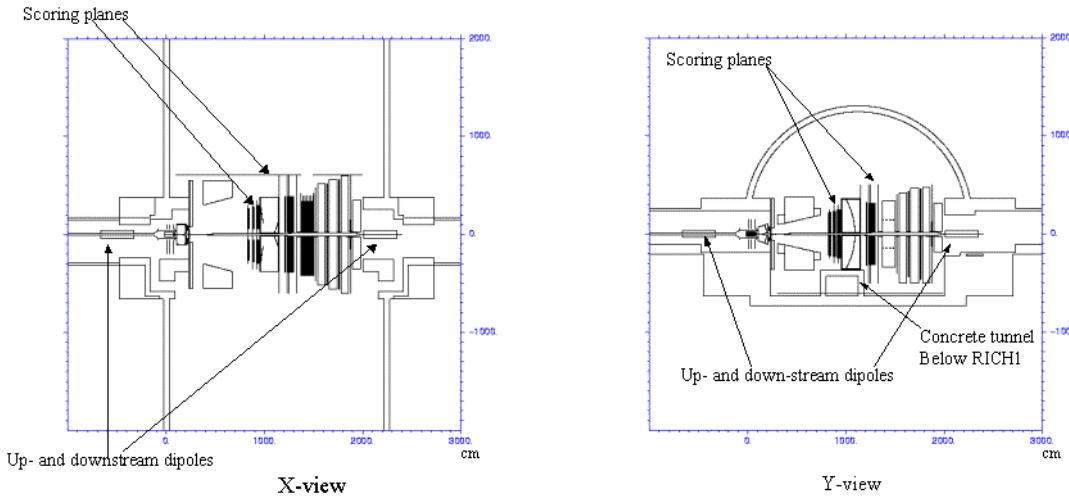


Figure 15 LHCb layout configuration for radiation levels study.

Material of all scoring volumes is silicon. In the cross-sections at $X=0$ and $X=200$ no special material is introduced. The dose is scored in the actual material of the detector present in each point of the scoring volume. The radiation level results have been divided into different categories to allow to use it to evaluate the possible effects on electronics. The three categories mentioned below is of particular use to define the radiation hardness requirements of electronics:

- Total ionizing dose is presented in units of Gy per collision.
- 1MeV neutron-equivalent fluence for silicon is used to define the level of damage to silicon lattice by hadrons (neutrons).
- High energy hadrons ($E_k > 20\text{MeV}$): Used to evaluate rate of Single Event Upset (SEU) effects.

The presented radiation levels are without any safety factors for uncertainty of the Fluka simulation and the variability of radiation resistance of electronics. A total safety factor of the order of ~ 10 must be used to define the requirements to electronics.

Results for the VELO detector area shows that radiation hard electronics must be used in the vicinity of the VELO both inside and outside of the vacuum vessel.

Location of the Level-1 electronics is constrained by the space available and the level of radiation in the experimental hall. Two possible locations are:

- In the experimental hall at the distance of about 10-15 m from the VELO vacuum vessel. Radiation level at this location may require radiation tolerant component for the Level-1 electronics (total dose effects are for most locations below 10 krad over the life time of the experiment, the effects of Single Event Upsets (SEU) must be considered seriously for complex electronics with large memory structures). However shorter cables may be used to transfer detector signals. Access to the electronics is also excluded during accelerator run and limited in time during the interruption (accessibility for an hour is expected to be granted with a 24 hour notice).
- In the underground counting room behind the massive concrete wall at the distance of about 40 m from the VELO. Radiation level in the counting room allows standard components to be used in the Level-1 electronics. This implementation requires longer cables which shall transport detector signals with losses under control. Access can be given at any time which simplifies maintenance during accelerator run.

In order to make a qualified decision about location of the Level-1 electronics for the VELO detector, several conditions have to be taken into account. They include, among others:

- feasibility to transfer detector signals over long cables without signal quality degradation at reasonable cost,
- qualification of the electronics components for the radiation levels and experience with the radiation tolerant electronics design techniques.

The positive result of the feasibility study of detector signals transfer gives a possibility to locate the VELO Level-1 electronics in the underground counting room and avoid the necessity of the radiation tolerant Level-1 electronics design and implementation. Otherwise a considerable efforts have to be put into qualification of the electronics components for the radiation levels and implementation of the Level-1 electronics using special radiation tolerant design techniques. Maintenance of the VELO Level-1 electronics also becomes more complicated.

3.2 VELO Level-0 electronics

The VELO detector is located in the vacuum tank around LHCb interaction point. In the LHCb Technical Proposal it is divided in 25 stations, each station has 4 silicon sensors with 2K strips, 200K detector strips in total.

Each sensor is attached to the hybrid with 16 Level-0 chips, 1600 Level-0 chips in total. Detector strips are bonded to the pads on the Level-0 chips. Each Level-0 chip has 4 multiplexed analog outputs and timing/control interface.

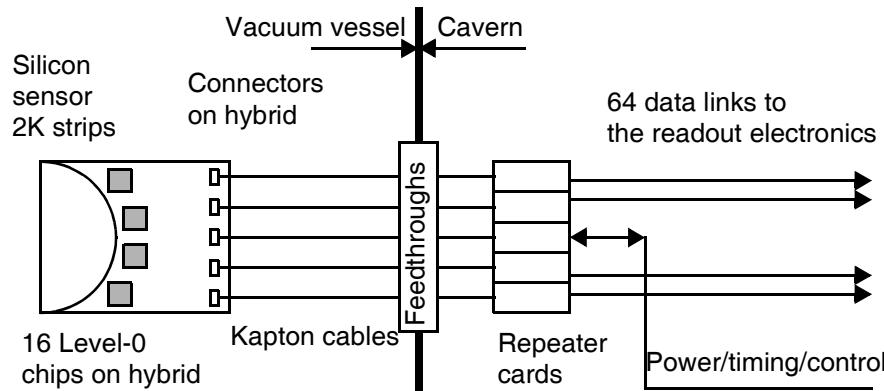


Figure 16 VELO Level-0 electronics layout.

Signals from connectors on the hybrid are transported via flexible kapton flat cables inside the vacuum vessel to the to the feedthroughs on the flanges of the vacuum vessel. Kapton cables are also used to distribute the low and high voltage power to the Level-0 chips on hybrids and to the silicon sensors.

Short cables between feedthroughs and connectors on the repeater cards isolates feedthroughs from mechanical stress during inserting and removal of the repeater cards.

“Digital” repeater cards (one card per hybrid, 100 cards in total) provide connection to the power supplies and to the timing and control systems. “Analog” repeater cards (4 cards per hybrid, 400 cards in total), located in the vicinity of the vacuum vessel contain drivers for the analog data links to the Level-1 electronics.

The analog data from the Level-0 chips has to be transmitted via electrical analog links (6400 links in total) to the read-out boards where they are converted to the digital data.

Therefore the main components of the VELO Level-0 electronics may be enumerated as following:

- 128-channel front-ens chips on the hybrid,
- Timing and control system interface for the VELO Level-0 electronics,
- Analog data links for the detector signals.

Following paragraphs describes in details individual components of the VELO Level-0 electronics.

3.2.1 Level-0 chips

VELO detector Level-0 electronics must conform to the overall LHCb Level-0 electronics and has to be radiation hard. Data from the VELO detector are used in the Level-1 trigger and in the data acquisition system.

Analog rather than binary front-end chip readout has been chosen since it provides a better hit resolution [23] and allows for better monitoring and control of effects due to the very non-uniform radiation damage to the silicon detectors. Detector readout lines are bonded to a front end chip which samples detector signals with the LHC bunch crossing frequency. The analog data have to be stored in the chip until a Level-0 trigger decision arrives and then are transferred to the VELO Level-1 electronics.

Requirements

Requirements to the VELO Level-0 chip are specified in [24]. The dynamic range was chosen to correspond to 10 times the charge deposited by a minimum ionizing particle in 150 μm silicon. The peaking time and sampling frequency is determined by the LHC bunch crossing rate of 40 MHz, the readout speed must match the Level-0 accept rate of 1 MHz. A signal to noise ratio (S/N) > 14 is required for reliable operation of the silicon detector even after the irradiation. The radiation hardness must be such, that the chip withstand 5 years of operation at an estimated load of around 2 Mrad per year. The length of the pipeline is given by the 4 μs latency of the Level-0 trigger decision plus the size of the derandomizing buffer, which has to be large enough to have negligible dead time at nominal operating conditions. A buffer depth of 16 events ensure that at readout speed of 900 ns per event and a Level-1 trigger rate of 1 MHz the remaining deadtime is below 1%.

The requirement about the tolerable signal left over after 25 ns (pulse spill-over) is derived from a study of the Level-1 trigger efficiency [23]. If the signals left over are too high, the Level-1 trigger starts to reconstruct tracks from the previous bunch crossing and assign them a large impact parameter. The output of the Level-1 trigger will then be saturated by fake b-events.

A single chip has 128 analog inputs. The data are brought off-chip at a clock frequency of 40 MHz, multiplexed to 4 lines. In addition every line transmits two samples of control information which code the pipeline location of the data that follows and thus allow to check the internal consistency of the data and the operation of the Level-0 electronics. With 34 bits of information per line and 40 MHz clock frequency the readout of one event is done in 850 ns. Additional functionalities of the chip are a programming via I²C-interface and internal pulse generation.

Level-0 chip design

Since a fast front-end readout chip satisfying the LHCb requirement was not available, it was decided to develop one within the collaboration.

Possible candidates to start from were the SCTA128 chip (built in the radiation hard silicon-on-insulator process [25]) developed for ATLAS and the HELIX chip (realized in a standard 0.8 μm CMOS process with a radiation tolerant design) developed for the HERA-B experiment.

Both chips are based on the RD20 architecture [26] shown in Figure 17, which contains a low-noise charge-sensitive RC-CR preamplifier/shaper stage, an analog pipeline, a derandomizing buffer for triggered events and an output multiplexer.

In the meantime access became available to the 0.25 μm CMOS technology, which can be made at least as radiation hard as the DMILL technology. To minimize the risk related to switching to a new technology, it was decided to pursue a dual approach:

- develop a new chip in 0.25 μm CMOS technology (Beetle [27]),
- modify the existing SCTA128 chip such that it fulfils the requirements for the readout of LHCb (SCTA_VEL0 [28]),

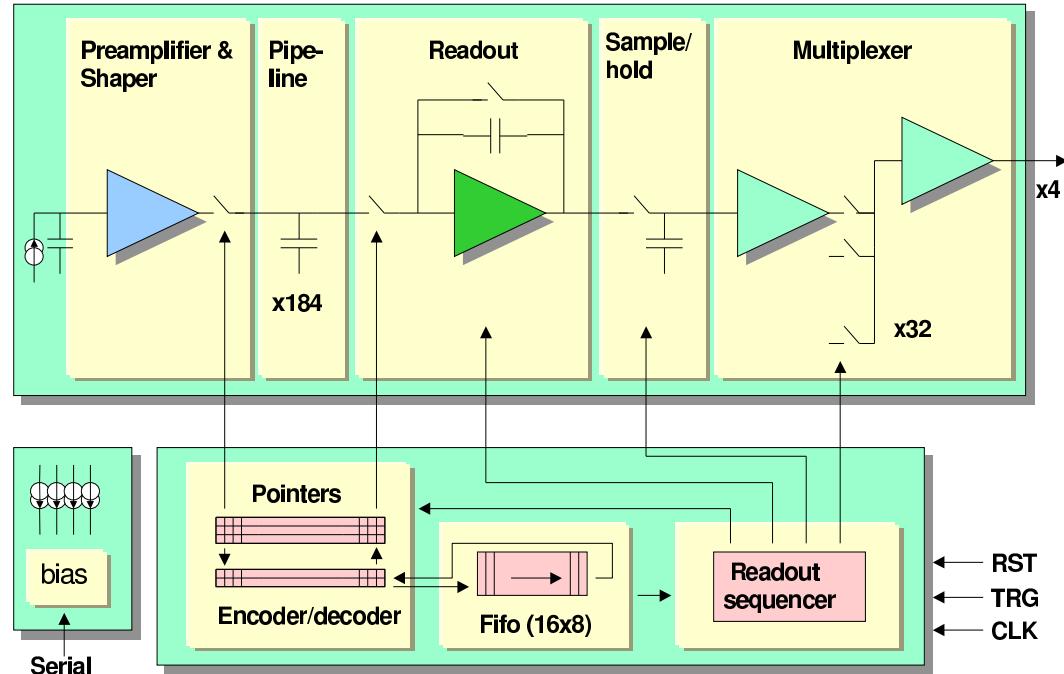


Figure 17 RD20 chip architecture.

R&D work towards the final Level-0 chip encompasses measurements with the existing SCTA128 chip, the predecessor of the SCTA_VEL0, studies of test chips with components of the Beetle and results from the first prototype of the complete chip, the Beetle1.0.

3.2.2 Level-0 electronics control

Each silicon sensor of the VELO detector will be equipped with 16 analog Level-0 chips (Beetle or SCTA_VEL0) residing on the hybrids inside the vacuum vessel. Radiation hard and flexible kapton flat cables transfer signals inside the vacuum vessel from/to the Level-0 chips to the feedthroughs. Outside of the vacuum vessel there are drivers for the analog signals from the Level-0 chips which are located on the “analog” repeater cards in the vicinity of the vacuum vessel.

For the proper operation, the Level-0 chips must be controlled by two LHCb systems - TFC and ECS. Receivers for the control signals are located on the separate repeater card (“digital”) in the vicinity of the vacuum vessel. “Digital” repeater cards also provides a connection to the low and high voltage power for the Level-0 chips on hybrids and for the silicon sensors.

All repeater cards are located on the flanges of the vacuum vessel using custom made mechanical support with short cables between feedthroughs and connectors on the repeater cards in order to isolate feedthroughs from mechanical stress during inserting and removal of the repeater cards.

3.2.2.1 Timing and Fast Control system interface

The TFC system is used for the distribution of all time critical signals to the Level-0 (a common clock synchronous to the accelerator, the Level-0 and Level-1 decisions, resets and synchronization commands, bunch crossing number and event number to all components needing this information, such as Level-0/Level-1 electronics, trigger, etc.) via optical distribution network tree (see Figure 8).

For their operation, Level-0 chips require three signals: 40 MHz clock, Level-0 decision and reset. They are delivered by the TTCrx receiver ASIC [29], developed by the CERN Microelectronics Group. It recovers 40.08 MHz LHC reference clock from the input optical signal and provides the Level-0 trigger decision (L1Accept output of the TTCrx chip), which can be delayed in steps of 25 ns (one clock cycle) up to 15 clock cycles. In the LHCb environment TTCrx 8-bit broadcast command is used to distribute reset to the Level-0 electronics.

Access to the internal registers of the TTCrx chip is provided by the I2C interface on the chip. The TTCrx chip contains a total of 20 user-accessible 8-bit registers.

TTCrx chip is located on the “digital” repeater card and is connected via optical fibre to the optical coupler (optical splitter). The TTCrx chip will be controlled in the same way as the Level-0 chips on the hybrid from the VELO Level-0 control system using I2C interface on the TTCrx chip.

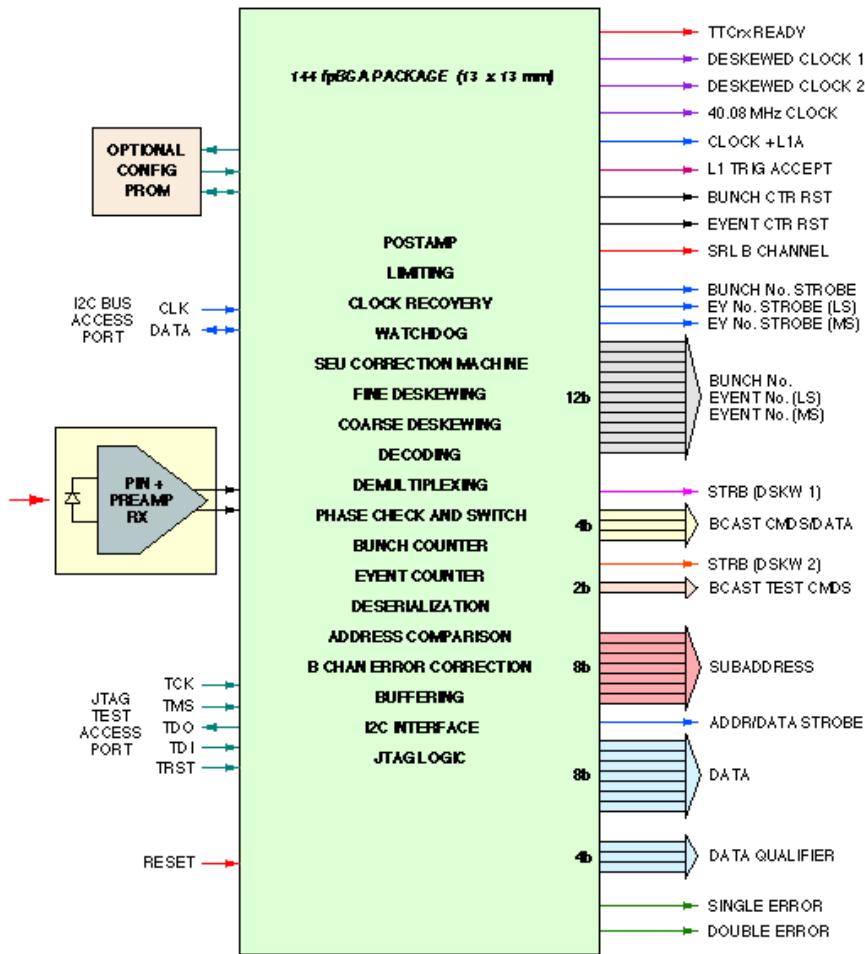


Figure 18 TTCrx receiver ASIC.

3.2.2.2 Experiment Control System interface

The control, monitoring, and verification of the Level-0 electronics is performed by the ECS that communicates with the Level-0 electronics via the ECS interfaces. In LHCb the ECS interface to the Level-0 electronics has been standardized, to insure a consistent and well functioning control and monitoring system. The Serial Protocol for Experiment Control System (SPECS) derived from the SPAC bus (Serial Protocol for Argon Calorimeter [30]) has been chosen as the preferred solution for the interface between the Level-0 electronics and the ECS. The chosen system for programming and reading the registers of the Level-0 electronics provides interfaces to both I2C and JTAG which is important as two options exist for a VELO Level-0 chip: Beetle chip uses the I2C interface protocol and the SCTA_VEL0 chip uses a reduced JTAG interface protocol. The last is identical on the hardware level to standard JTAG thus the modified protocol can be implemented in software.

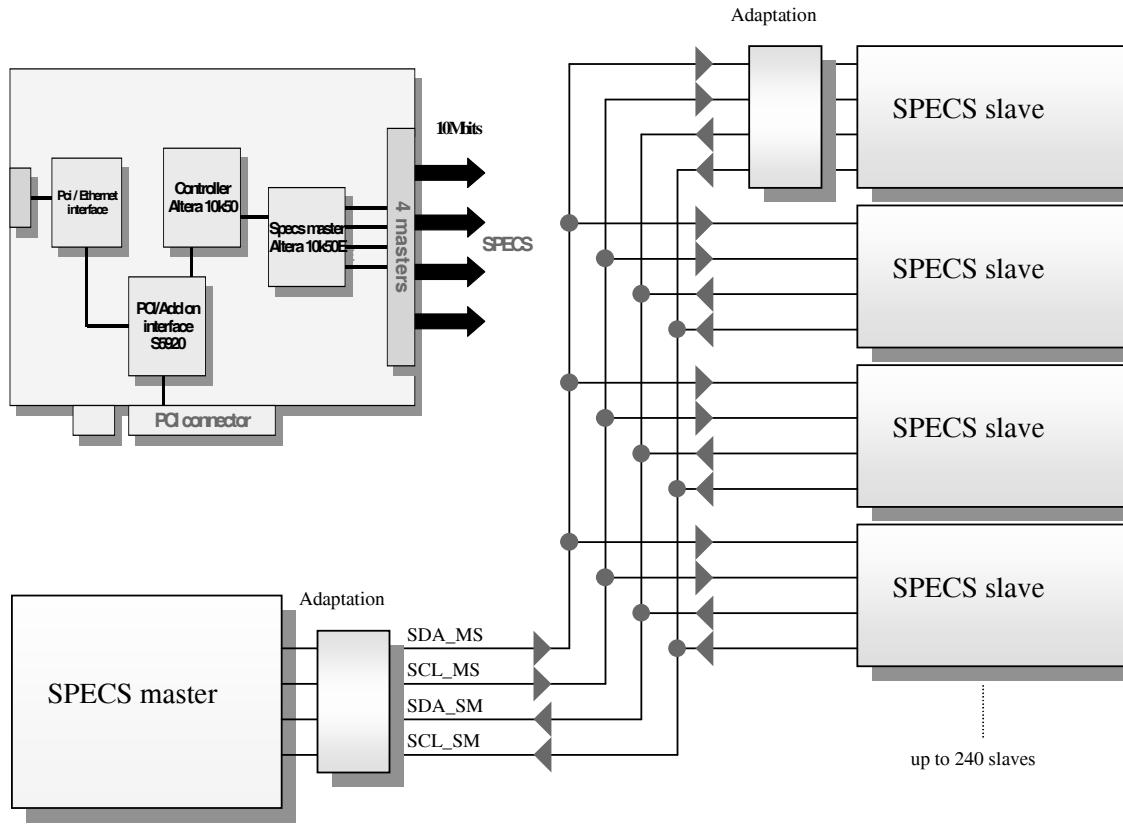


Figure 19 SPECS bus.

SPECS is a one-master n-slaves bus (Figure 19) where the master is implemented in a PCI board located in a PC in the counting room. The SPECS master board provides up to 4 output SPECS buses. The SPECS bus is fast (100 Mbit/s) and works up to 100 m using cheap AWG26 Cat5 cables. Up to 240 slaves can be connected to one SPECS bus.

The slave boards are located in the cavern, close to the detector. The slave board acts as a SPECS to the Level-0 electronics transceivers and contain four SPECS slaves, each provides four differential I2C and JTAG buses either directly or via an active bus splitter. A total length of about 10 m can be realized for I2C and JTAG interfaces, hence the slave board may be located at a distance where the radiation dose is below 100 Rad/year and therefore may be radiation tolerant, for example, implemented in an Actel FPGA with SEU tolerant antifuse technology.

The number of Level-0 chips connected to a single bus is only limited by the 7 bit I2C/JTAG address scheme. For both I2C and JTAG, all chips on a hybrid will be connected to a single bus from SPECS slave. Thus the Velo Level-0 control system has to provide 100 I2C/JTAG buses, one for each hybrid.

3.2.2.3 Digital repeater card and overall timing/control layout

The overall timing and control layout for the VELO Level-0 electronics is described in [31] and shown on Figure 20.

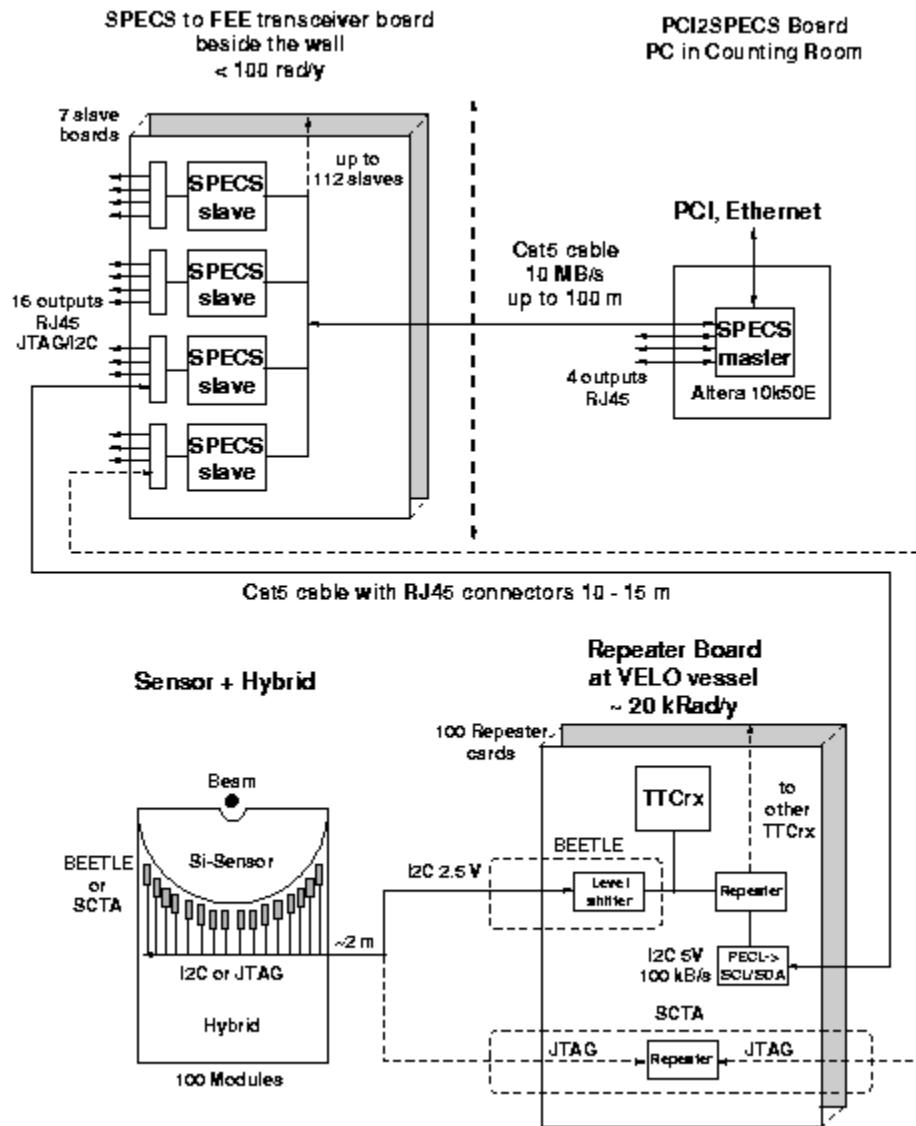


Figure 20 VELO Level-0 electronics control (from [31]).

One SPECS slave board provides up to 16 I2C/JTAG buses, therefore, 7 slave boards, located in a single crate, are sufficient to connect all 100 “digital” repeated cards to the SPECS bus. As the SPECS bus can be distributed in the crate via the backplane, only one link is needed to connect the crate to the SPECS master located in the counting room. “Digital” repeater cards (one card per hybrid, 100 cards in total), which are located on the flanges of the vacuum vessel, provide connection to the timing and control systems. Each “digital” repeater card contains:

- One TTCrx chip which receives timing and fast control signals via optical fibre from the TFC system. The output signals (40 MHz clock, reset and Level-0 decision) are converted to 2.5V LVDS signals and are transferred to the Level-0 chips on the hybrid. The TTCrx chip is controlled in the same way as the Level-0 chips on the hybrid via I2C interface.
- I2C/JTAG bus receivers which converts the differential I2C/JTAG signals to the standard 2 wire bidirectional bus. They are connected to the SPECS slave on the slave board, located at the distance of about 10-15 m from the vacuum vessel,
- power connectors for high and low voltage.

3.2.3 Analog data link

The front end chip samples detector signals with the LHC bunch crossing frequency of 40 MHz. The analog data have to be stored in the chip until a Level-0 trigger decision arrives and then are transferred to the VELO Level-1 electronics. A single chip has 128 analog inputs which are multiplexed to 4 lines at a clock frequency of 40 MHz. 32 samples of the analog data (charge released in the silicon and encoded as a voltage level) plus two samples of control information (constant voltage levels) are sequentially sent out of the Level-0 chip via kapton cable to the feedthroughs and then to the “analog” repeater card.

3.2.3.1 Link requirements and implementation options

The analog data from the Level-0 chips has to be transmitted to the read-out boards. A preferred location of the VELO Level-1 electronics is in the underground counting room behind the massive concrete wall at the distance of about 40 m from the VELO detector where radiation level allows to use standard components.

The definition of the analog data link includes all link components starting from the link drivers on the “analog” repeater card, connectors, cables, receivers, up to the digital output of the link inside the Level-1 electronics. The requirements to the link between the Level-0 and the Level-1 electronics are:

- a minimal distortion of the analog data during transmission over long cable due to a sample-to-sample crosstalk (<5%) and a signal attenuation,
- a minimal degradation of the signal to noise (S/N) ratio at the receiving end of the link (10%),
- low sensitivity to the electromagnetic radiation (noise),
- 8-bit digital output data at the receiving end,
- link implementation matching the Level-1 electronics granularity - 32 or 64 analog links per Level-1 board (in order to avoid an extra cost overhead).

Several possible implementation options has been taken into consideration [32]. They are differ by their parameters and cost.

An analog electrical link is the simplest and cheapest one (Figure 21). It is based on the twisted pair cable for the data transmission. The analog data from the Level-0 chip are amplified by the radiation hard link driver on the “analog” repeater card in the vicinity of the detector and transmitted to the read-out board via multi-conductor shielded twisted pair cable.

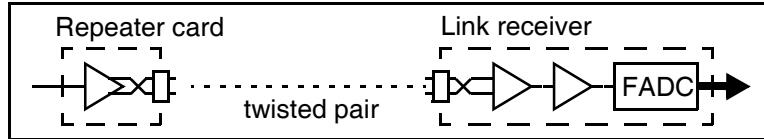


Figure 21 Analog electrical link.

On the read-out board, after link receiver and amplifier, the analog signal is converted into 8-bit digit by FADC. This link provides required technical parameters at relatively low cost. It is also well matched to the Level-1 electronics granularity.

A digital optical link (Figure 22) is under development for the LHCb inner tracker readout [33]. The analog data from the Level-0 chip are digitized directly on the “analog” repeater card by radiation hard FADCs (two dual FADC AD92288 per one Level-0 chip). Four 8-bit words are serialized and transmitted to the read-out board via 1.6 Gbit/s digital optical link (e.g. Gigabit Optical Link transmitter, GOL, from CERN microelectronics group).

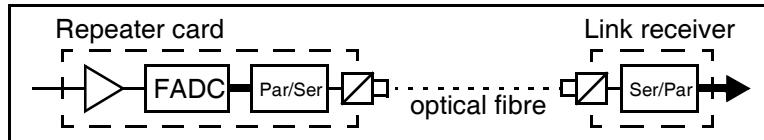


Figure 22 Digital electrical link.

Parallel optical transmitter and receiver (VCSEL) and 12 fibre optimal MPT cable may be used to transfer the data. Parallel optical link receiver performs optical to electrical conversion. The incoming digital data are deserialized and distributed to the Level-1 electronics. The link cost is about 50% higher than the analog electrical link, and the cost optimal link implementation is not well matched to the VELO Level-1 electronics granularity.

An analog optical link [34] has been developed for the inner tracker of the CMS experiment. The optical link is schematically shown in Figure 23. The link is based on a multi-way unidirectional edge-emitting laser transmitters coupled to single-mode optical fibres, multi-way connectors and pin-photodiode receivers.

The total length of the link is approximately 100m, of which about 10m is within the high radiation environment.

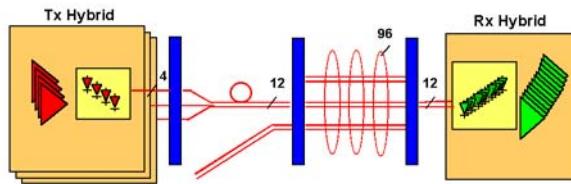


Figure 23 Analog optical link.

The optoelectronic transmitter and receiver components are assembled using Si-submount technology. The laser diodes are commercially available Multi-Quantum-Well (MQW) InGaAsP edge-emitting devices selected for their good linearity, low threshold current and proven reliability. Photodiodes are epitaxially grown, planar InGaAs devices of small active volume. This link provides required technical parameters, but its main disadvantage is a relatively high cost (about 3 times higher than the analog electrical link).

3.2.3.2 Analog link design (by R. Frei, UniL)

The analog electrical link was chosen as a possible analog link implementation due to its low cost and a possibility to provide required technical parameters.

The transmission of an analogue stream at 40 Msample/s over a short distance is quite straightforward. Some distortions appear for >40 m resulting in sample-to-sample crosstalk. The attenuation of a shielded cable is proportional to the square root of the frequency and will introduce a severe distortion in the rising and falling edges of a pulse. The distortion will limit the length of the cable that must be used in the application. Two methods are used to compensate these effects:

- the use of high quality twisted pair cable with low attenuation variation vs. frequency,
- the use of electronic circuits (a line equalizer) which compensate the attenuation of the cable vs. frequency.

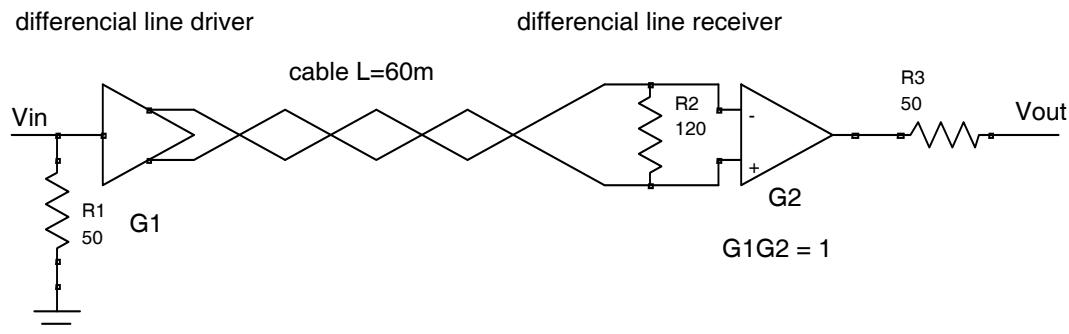


Figure 24 Analog link measurements setup.

The complete analog link setup, used for the measurements, is shown on Figure 24. A set of measurements has been done on this setup in order to make a characterization of the cable [35]. It includes a measurements of pulse and frequency responses. The 60 m cable has been used to provide a safety factor.

The differential line driver and the differential line receivers are made with a single chip HFA1212 from Harris which is a dual video buffer. The overall gain of the transmission system is unity. A sinusoidal signal with constant amplitude had been applied at V_{in} and the output voltage had been monitored vs. frequency. The Figure 25 shows the attenuation of the system vs. frequency between 1 MHz to 100 MHz. The loss at 40Mhz is greater than 6,5 dB.

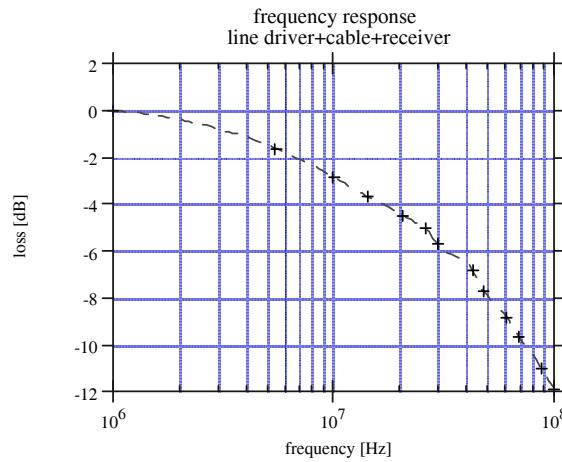


Figure 25 Cable frequency response.

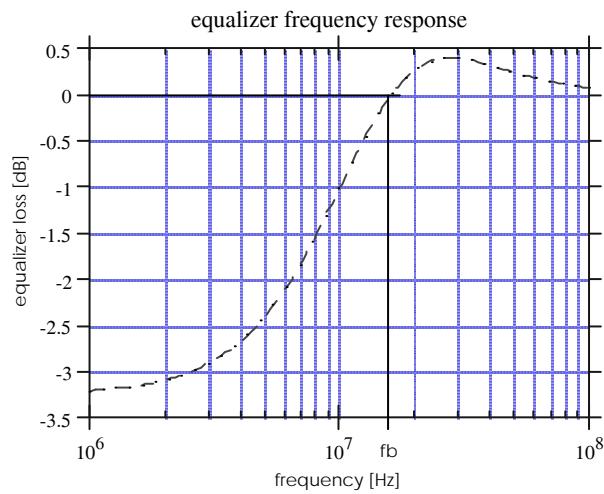


Figure 26 Equalizer frequency response.

The measured cable parameters provides an input for calculation of the characteristics of the line equalizer, which is used to compensate the attenuation of the cable vs. frequency. The details of the line equalizer, designed by R.Frei, can be found in [35].

The Figure 26 shows a simulation of the equalizer frequency response between 1 MHz and 100 MHz and the Figure 27 shows the result the frequency response through the system with the equalizer. The response is flat up to 20 MHz. A post amplifier with a gain of 4 dB is necessary to recover the loss due to the cable and the equalizer.

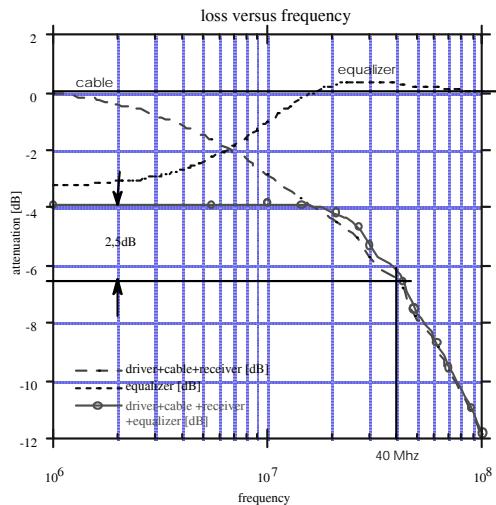


Figure 27 Cable + equalizer frequency response.

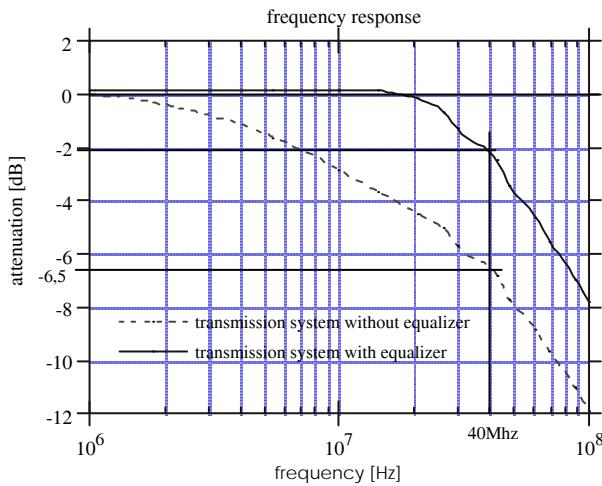


Figure 28 Simulated frequency response through the system.

The Figure 28 shows a simulated frequency response of the system without (dash line) and with the line equalizer and the post amplifier (solid line). The response is flat up to 20 MHz.

A complete analog link setup (Figure 29) uses two different boards. The line driver is mounted on one PCB, and the receiver part is mounted on a second one. The second board is the FADC board, a prototype of the VELO Level-1 electronics board RB2 [43].

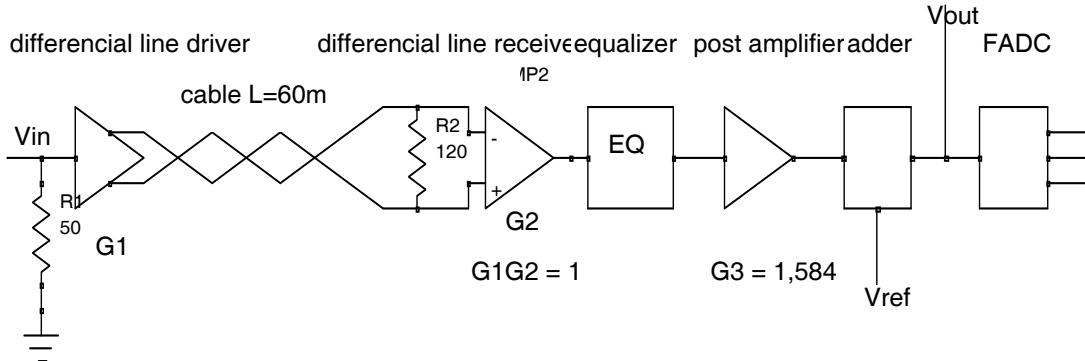


Figure 29 Complete analog link.

The line equalizer is added with the post amplifier with a gain of 4 dB. An adder is needed to provide the voltage reference required by the FADC. The post amplifier and the analogue adder are done with an AD8055 from Analogue Device.

A sinusoidal signal with constant amplitude is applied to V_{in} . The output amplitude is monitored at V_{out} point when the frequency changes from 1 Hz to 100MHz. The attenuation vs. the frequency is reported on the Figure 30. The continuous line is the measurement.

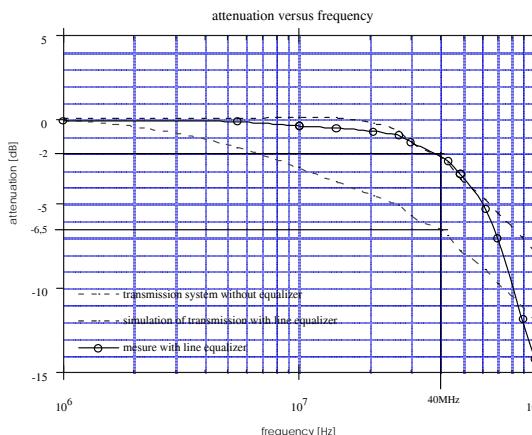


Figure 30 Frequency response.

The linearity of the chain is the ratio of the output amplitude over the input amplitude in the range of 0 to 2,5 V. The gain of the system can be adjusted via a variable resistor. The gain must be set at 1. The Figure 31 shows the output voltage vs. the input voltage.

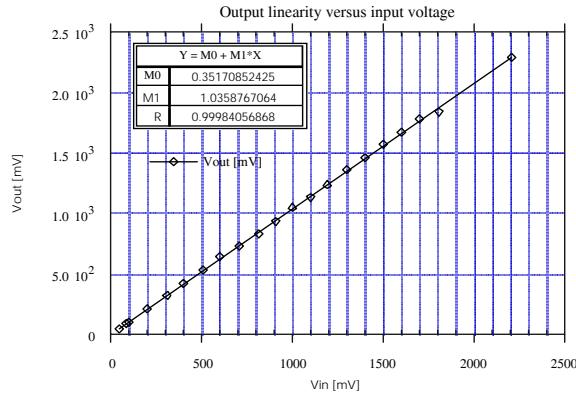


Figure 31 Output voltage vs. input voltage.

The output voltage increases linearly up to 2,2V and starts to saturate above this value. The saturation appears also at -2,2V for negative input voltage. The global gain is 1. The output range of the FE chip used in the detector will be 1V which will be the maximum input voltage of the analog link.

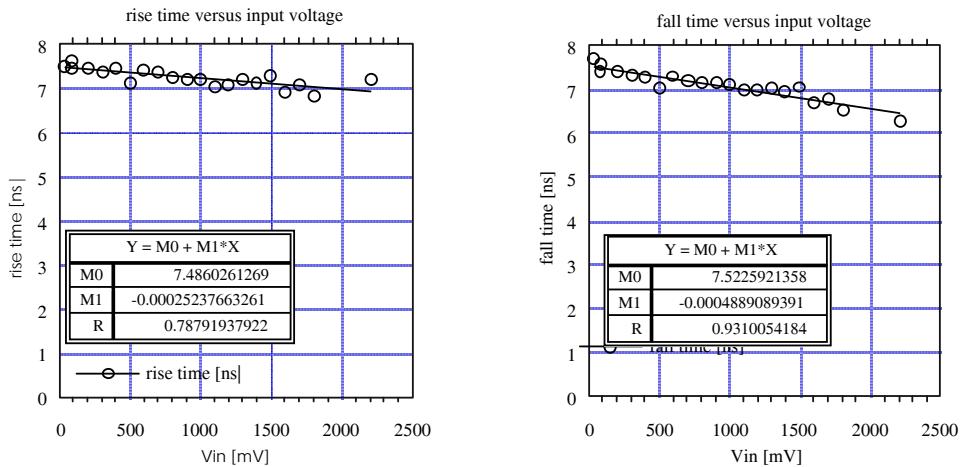


Figure 32 Rise and fall time vs. input voltage.

The rise and fall time vs. input voltage has been measured. A 25 ns pulse is applied at the input and the amplitude is increased until the voltage saturation of the amplifiers. The rise and fall time of the output signal is monitored for each input amplitude. The Figure 32 shows the output signal rise and fall time vs. the input voltage. The output rise and fall time is equal to 7,5 ns vs. the input voltage. With an input voltage range of 1V, which correspond to a FE chip output, the rise and fall time of the signal is not affected.

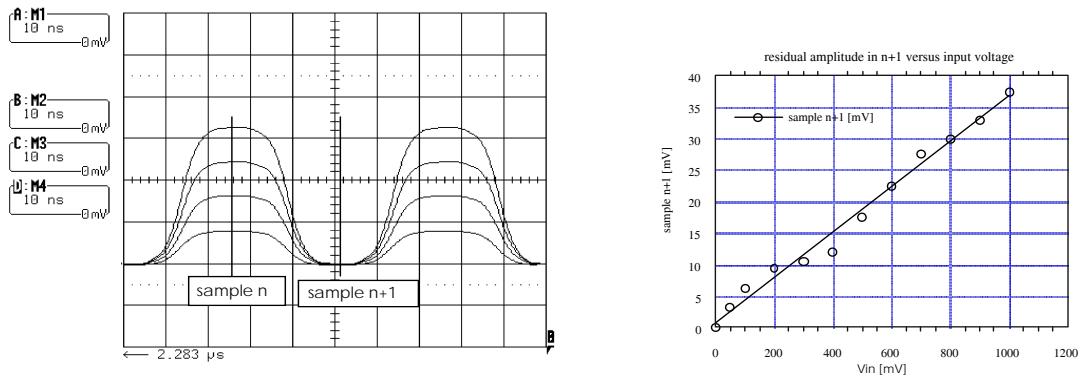


Figure 33 Samples digitization and crosstalk factor.

Distortions introduced by long cables can often be ignored in pulse transmission, but are critical in time multiplexed readout. Their effects will appear as some crosstalk between data samples. These effects are illustrated through the crosstalk factor CF, which is defined as the fraction of sample n that persists in the amplitude of the sample n+1. The amplitudes are measured at the middle of their duration. The sample n+1 is digitized 25ns after the sample n. For the measurement, the sample n amplitude rises from 0 to 1V, and the residual voltage is monitored in the sample n+1, i.e. 25 ns after the sample n.

The Figure 33 shows how the samples are digitized and the residual voltage in sample n+1 vs. the amplitude of sample n. The crosstalk factor (CF) is the slope of the line in this case. The crosstalk factor is equal to 0,037 and slightly dependant on the moment on which the samples are digitized. The crosstalk factor have been measured for cables with different length without a line equalizer. They are summarized in the table below. The CF = 0,037 for 60 m cable is quite similar as using a cable with a length of 8 meters without line equalizer.

Length [m]	CF
5	0,0277
10	0,0526
35	0,156
40	0,172
60 + EQ	0,037

The equalizer allows to recover distortion introduced by long cable with a minimum of components. Pre-emphasis at the transmitter end could also improve the frequency response of the analog link.

The final line equalizer design will be done when all the parameters of the cable are known. Cross-talk between individual twisted pairs in the cable will be also measured.

3.3 VELO Level-1 electronics development

The VELO Level-1 electronics is located in the underground counting room behind the massive concrete wall at the distance of about 40 m from the VELO detector. Event data for the events, accepted by the Level-0 trigger system, are sent from the Level-0 chip derandomizers via analog links to the Level-1 electronics. The total number of analog links is 6400 (for the LHCb TP layout).

The overall layout of the VELO Level-1 electronics is shown on Figure 34.

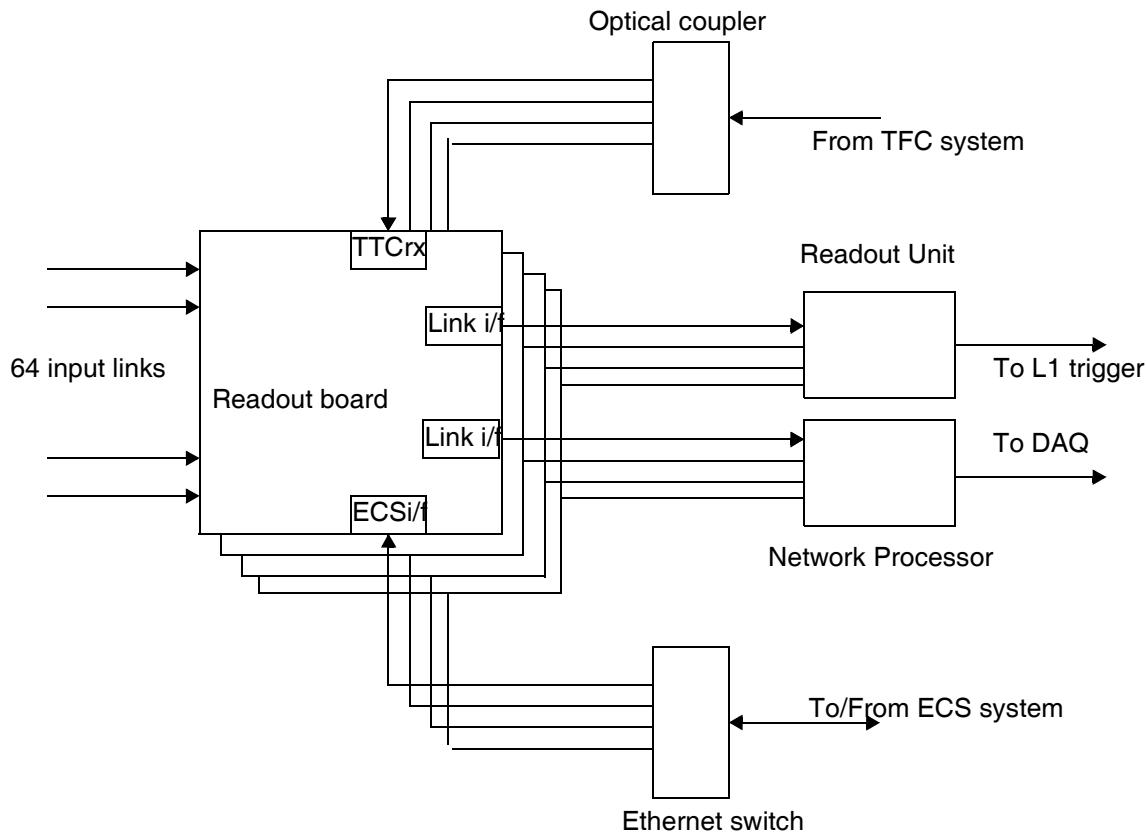


Figure 34 Overall VELO Level-1 electronics layout.

The VELO Level-1 electronics performs the following tasks:

- conversion of the incoming analog data sequence from the Level-0 electronics into 8-bit digital data using 8-bit, 40 MHz FADC,
- synchronization check of incoming data using information from the TFC system and embedded information in the incoming data from the Level-0 electronics, as described in [36] and [37],
- data preprocessing for the Level-1 vertex topology trigger (cluster finding) and transmission to the Level-1 trigger system,

- digital data storage in the Level-1 buffer during the Level-1 trigger latency until the Level-1 trigger decision, distributed to the Level-1 electronics via the TFC system,
- data processing by the digital signal processors after the Level-1 Accept decision (zero suppression) and transmission to the data acquisition system (DAQ),
- control and monitoring of the data flow through the Level-1 electronics.

Each board of the VELO Level-1 electronics receives the analog data from the 64 analog data links (100 Level-1 electronics boards in total). Therefore, the VELO Level-0 electronics for one silicon sensor with 2K detector strips (one hybrid with 16 Level-0 chips and four “analog” repeater cards) is connected to one VELO Level-1 electronics board. The boards are located in the crates and racks in the counting room and connected to the VELO Level-0 electronics by the multi-conductor shielded twisted pair cables.

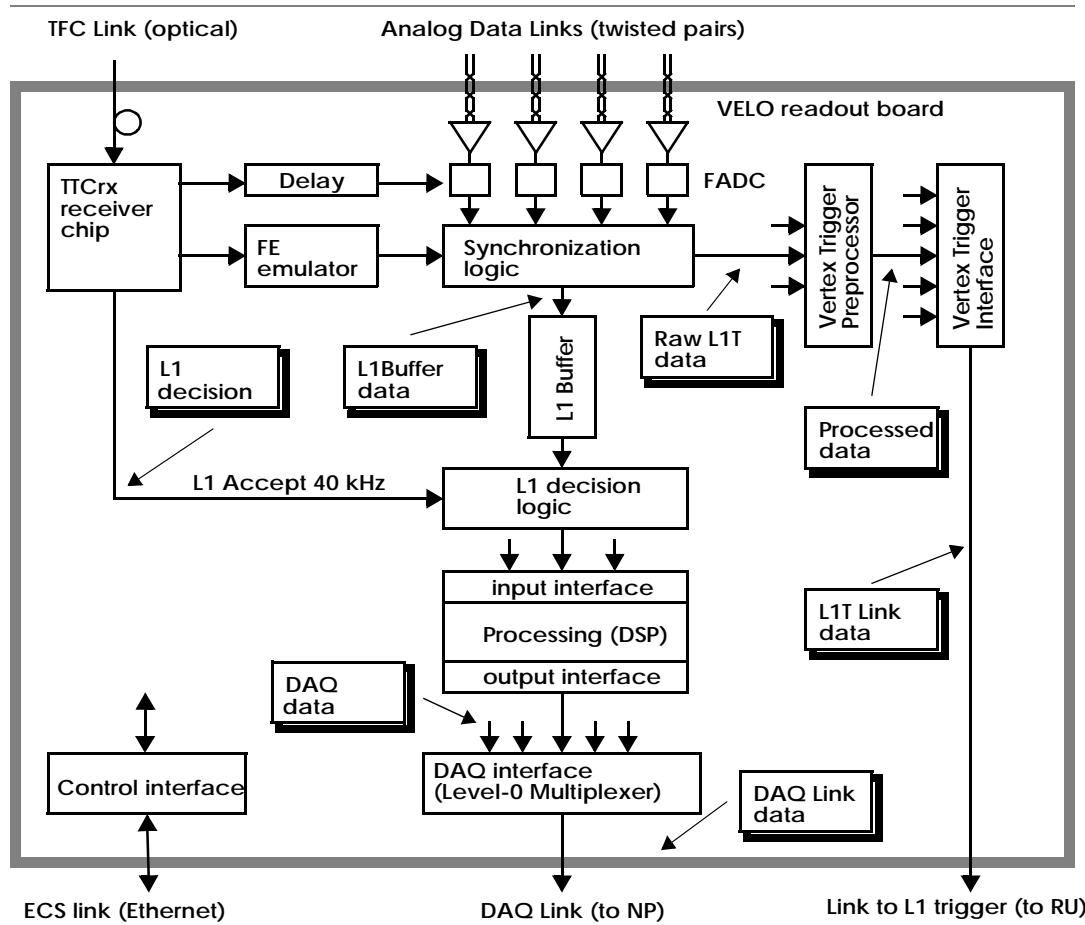


Figure 35 VELO Level-1 electronics board layout.

For the proper operation, the VELO Level-0 electronics is controlled by two LHCb systems, as described in 2.1 and 2.4 - TFC and ECS. The TFC system delivers the timing and fast control information to the VELO Level-0 electronics via optical distribution network based on optical couplers, and TTCrx receiver chips on the Level-1 boards. The ECS system is connected to the VELO Level-0 electronics via Ethernet network (Etherner switches) and micro-controllers on the Level-1 boards.

Each VELO Level-1 electronics board sends data to the LHCb Level-1 trigger system and to the LHCb DAQ system via two separate links. Links to the Level-1 trigger system are connected to the Readout Units [38] in the Level-1 trigger system. Links to the DAQ system are connected to the Network Processors [39] in the DAQ system.

The Level-0 electronics board (Figure 35) performs analog data digitizing, synchronization tasks, data preprocessing for the Level-1 vertex topology trigger, digital data storage during Level-1 trigger latency, data processing by digital signal processors (DSPs) after Level-1 accept and transmission to the data acquisition system (DAQ).

The VELO Level-1 board is a custom 64 channels module. It is implemented as a 9U module (366.70 mm x 400.00 mm, IEEE1101.10 mechanics). It is housed in a standard crate with a custom power distribution backplane, which provides power to the boards.

The board uses standard commercial (non radiation hard or radiation tolerant) components. Connectors for the multi-conductor shielded twisted pair cables are located on the front side of the module. On the read side, above the power backplane, there are connectors for the output links to the LHCb Level-1 trigger system and to the DAQ system, Ethernet connector for the ECS system and optical connector for the TFC system.

The total number of the VELO Level-1 electronics components for both, LHCb TP and “LHCb light” layouts are summarized in the table below:

VELO Level-1 electronics component	Total number (LHCb TP)	Total number (“LHCb light”)
Analog links	6400	5376
64-channel Level-1 boards	100	84
Optical couplers (32 to 1)	4	3
Ethernet switches (16 to 1)	7	6
Level-1 trigger Readout Unit	25	21
DAQ Network Processor	25	21
Crates	5	4

3.3.1 Level-1 electronics prototyping

The VELO Level-1 electronics must conform to the defined requirements for the LHCb Level-1 electronics. The logical data flow architecture of the Level-1 electronics is based on extensive simulation of the LHCb electronics architecture. The main goals of the LHCb electronics simulation are:

- determine the best architecture of the Level-0 and the Level-1 electronics,
- optimize buffering requirements and prevent buffer overflows in the Level-0 and the Level-1 electronics,
- define models to be used as a highly accurate specification of the electronics implementation.

A simulation model was developed to simulate the Level-0 electronics and define key Level-0 electronics parameters [40]. Several extensions and improvements have been added to the model to make it appropriate for simulation of the Level-1 electronics [41]. The simulation has been developed using VisualHDL. This tool enables graphical and language based descriptions, as well as both top-down and down-top design strategies. The top level of the architecture is described using block diagrams. Detailed building blocks have been made directly in VHDL. This approach enables a quick overview of the global architecture and a precise behavioural description of basic functions.

The general behavioural simulation of the LHCb electronics architecture defined several important parameters, like the Level-1 electronics buffering requirements, Level-0 electronics readout time, etc. The VELO Level-1 electronics development is based on the results of the simulation.

Some simulation languages have in fact from the start been defined as a hardware specification language. After a refinement of a general (behavioural) simulation model the designers of Level-0 and Level-1 electronics can obtain detailed (register level) simulation models which can be used for detailed simulation of the implementation of the Level-0 electronics for a specific sub-detector. Integrating such a detailed implementation simulation model into the more general system simulation model can be used to verify its correct function in the system. Detailed register level models can finally be used as a source to automatically synthesize the logic of Field Programmable Gate Arrays (FPGA) or hardwired Application Specific Integrated Circuits (ASIC).

The LHCb electronics behavioural simulation, however, doesn't provide implementation details. The functional prototyping stage is necessary to understand a complexity of different parts, to check new ideas and to define a possible further implementation. It also may be used to setup the development and test environment and to provide tools for different tests of other parts of the VELO detector and Level-0/Level-1 electronics.

3.3.1.1 Design flow

The VELO Level-1 electronics board is a complicated device which involves different technologies and techniques. The design generally started from the preparation of the overall detailed specification, partitioning of the future design in individual functional blocks and definition of interfaces between them. For several designers, involved in the project, this gives a possibility to work in parallel on individual blocks. The specification phase may need several iterations steps.

The design flow used for the VELO Level-1 electronics prototyping is presented schematically on Figure 36. The design specification phase is followed by the implementation. During the functional prototyping stage, some parts of the electronics may be implemented on separate mezzanine cards, located on the main motherboard. The mezzanine card may correspond to the functional block or several blocks. This allows to perform in parallel mezzanine cards implementation, debugging and test. The main board also may be designed without waiting for the final design of the mezzanine cards as soon as the interfaces are defined.

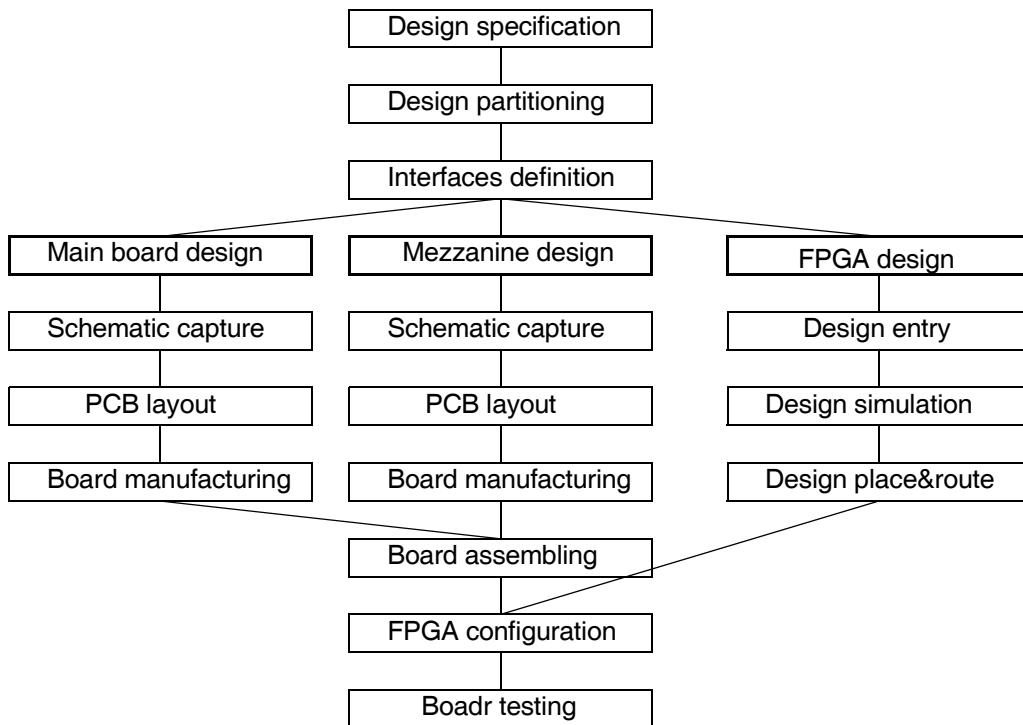


Figure 36 Design flow.

The main board and mezzanine design started with schematic capture using library components. Printed Circuit Board (PCB) layout is based on the output of the schematic capture. Finally, all components are mounted on the board and mezzanine cards.

Modern digital electronics boards are largely based on FPGA devices to implement necessary functionality. Standard components are restricted to analog part of the design, digital storage devices (static random access memories - SRAM, dual-port memories - DPM, first-in first-out memories - FIFO) and standard communication, computing, power and timing devices. Similar to the mezzanine cards, each FPGA may correspond to the functional block or several blocks. The interface definition for FPGAs allows main board layout in parallel with the FPGA design. FPGA design is mainly based on hardware description languages (HDL) such as Verilog and VHDL which supports design entry and simulation. For the design entry stage, different techniques may be used - simple text entry with a text editor and more sophisticated graphical entry tools. Several tools are available for the design simulation. The last phase - place and route of the design in a particular FPGA device - are executed by the vendor specific tools which are optimized for a particular FPGA family.

Simulation of the design is an important step during the design flow as it allows to discover errors on the early stage and helps during later phase of the design debugging. For the proper design simulation, the surrounding environment in which design (a particular FPGA device or the complete board) is working must be described correctly. For example, in case where FPGA is connected to a memory device or to an interface to another external system, a proper HDL model of such a memory or interface shall be available or created by the designer. The verification of the design will be correct to the level of correctness of the HDL model of such external system.

The time necessary for the creation of the models of external systems may be comparable or even exceed the creation time for the design itself as external systems may be more complex than the design. Therefore, models for external systems are often simplified to the level of required functions and are implemented to the extend of their understanding by the designer. This shorten the verification phase but reduces the verification power of the simulation environment.

During complete design debugging in a real test setup, the existence of the simulation environment helps to discover internal errors. The model of the external system may be adjusted to reflect the real behaviour of the test environment and used to correct possible errors in the design.

3.3.1.2 Level-1 electronics prototypes

The proposal [42] for the VELO Level-1 electronics prototyping was prepared before the prototyping began. Initially, it was decided to limit the prototype functionalities to the interface to the VELO Level-0 electronics - analog data digitizing and synchronization tasks.

The prototype of the interface to the Level-0 electronics was designed to match the final implementation LHCb read-out chip. As an intermediate step, this prototype may be adapted for other read-out chips (e.g. SCTA128). The prototype functionality will be developed gradually using re-programmable logic (FPGAs). Prototypes of the other parts of the Level-1 electronics were also foreseen.

The first prototype of the Level-1 board (sometimes referred as readout board one, RB1) was implemented as a 6U VME wire-wrap board and has limited functionalities. The board clock frequency was limited to 10 MHz due to the wire-wrap implementation. The main purpose of this prototype was to setup design and test environments and to implement some basic features.

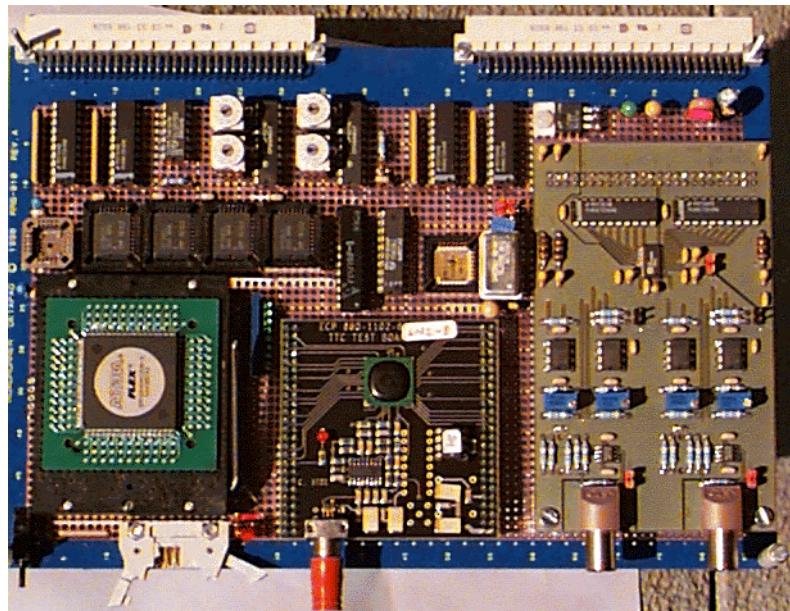


Figure 37 RB1 prototype with FDAC card and TTCrx card.

The RB1 includes:

- 2 channel analog to digital interface card,
- Local storage - 2K FIFO memory, 16 bit wide,
- FPGA (VME interface and logic prototyping),
- interface to the TFC system (TTCrx receiver chip).

The VME interfaced was used as a control interface to access module internal registers and FIFO memory. The interfaces to the Level-1 trigger system and to the DAQ system were not implemented, however, initial prototyping of some Level-1 trigger interface functionalities was done with this prototype. Due to its limitations and clock frequency, this prototype was not used for the actual Level-0 chip readout.

The second prototype of the Level-1 board (referred as readout board two, RB2 [43]) is implemented on a printed circuit board and works with 40 MHz board clock. The RB2 module is designed for the read-out of up to 4 analog links with multiplexed analog signals from the VELO detector Level-0 chip(s). Seven boards were produced and used in the lab and test-beam to readout Level-0 chips (SCTA128 and Beetle). User manual [43] was written and updated several times during gradual module development.

The RB2 module is a 6U VME module and it occupies 2 slots in the crate when used with the daughter cards. It consists of a main VME board and 3 daughter cards as shown on Figure 38 and Figure 39.

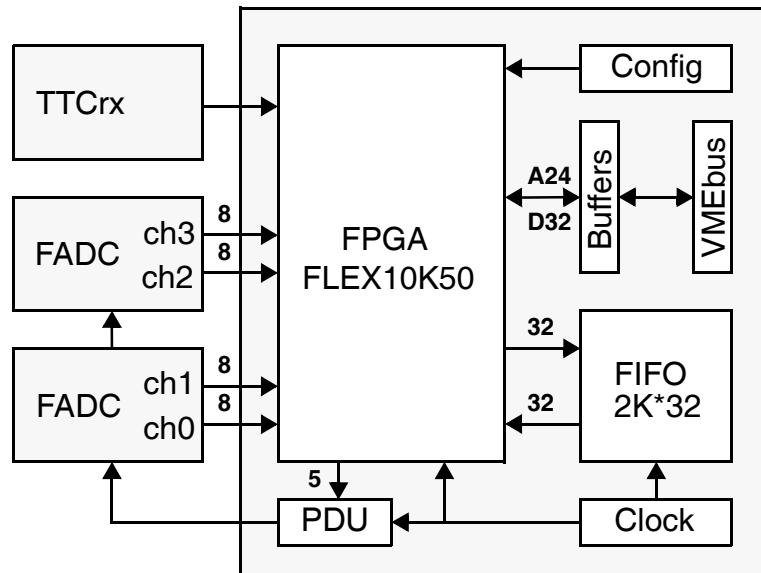


Figure 38 RB2 block diagram.

The main VME board provides:

- Altera FLEX FPGA EPF10K50RC240-3, connector for FPGA configuration via down-load cable and socket for the configuration EPROM (EPC1PC8),
- VMEbus slave interface (A24/D32) which is used as a control and monitoring interface to the module,
- 40 MHz internal clock oscillator and programmable delay unit for FADC clock adjustment (PDU15F-1 from Data Delay Devices), LEMO connector for the BUSY output signal (TTL open collector, active low) and the Reset button,
- 2K*32 bit of FIFO (4 SyncFIFO chips Cypress CY7C4231, 15 ns access time).
- 2 connectors to a TTCrx board carrying a TTCrx chip and 2 connectors for FADC cards (2-channels, 8-bit, 40 MHz, based on AD9059 from Analog Devices) and voltage regulators for FADC cards analog power.

One of the FADC cards can be replaced by the level-1 trigger preprocessor interface prototype [44] or the ECS interface prototype [45].

The RB2 module receives external clock and trigger signals via optical connection on the TTCrx board and Level-0 chip analog signals from 4 input analog links.

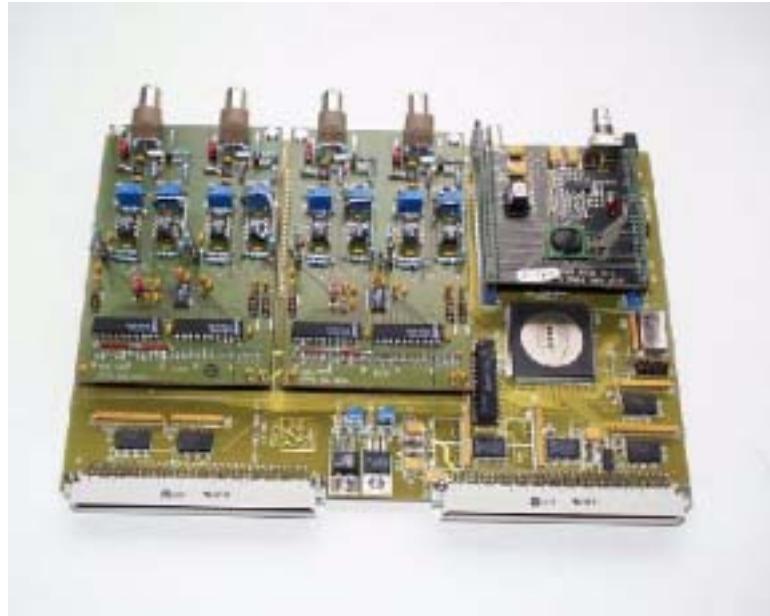


Figure 39 RB2 photo with 2 FDAC cards and TTCrx card.

The TTCrx board contains the TTCrx chip, the optical connector with an integrated detector/preamplifier and some other components. The input optical signal from the TTC transmitter carries 40 MHz clock and trigger signals.

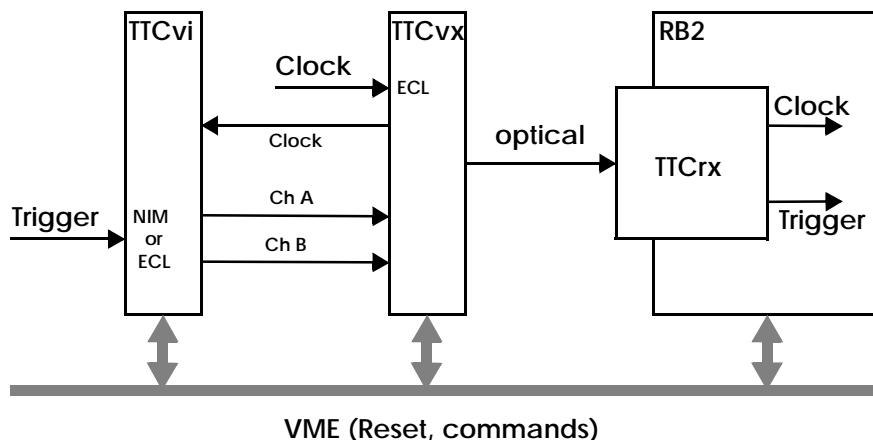


Figure 40 TFC setup environment for RB2 board.

In order to operate the TTCrx board the TTC transmitter (TTCvx [46]) and the TTC control module (TTCvi [47]) are necessary, as shown on the Figure 40. The 40.00 MHz clock signal (ECL levels) and the Trigger signal (NIM or ECL levels) are provided by the external logic.

The 2 channels FADC mezzanine card (Figure 41) contain link receivers, amplifiers, analog-to-digital converter AD9059 (dual 8-bit, 60 MSPS A/D converter) and output buffers. The input signals from the LEMO connectors are differential in the range from 0 to 1 Volts. The 50-pin DIN 41651 connector provides the digital and analog power, FADC clock and data enable signals for the FADC card from the RB2 module and the 2*8-bit output data from the FADC card output buffers to the RB2 module.

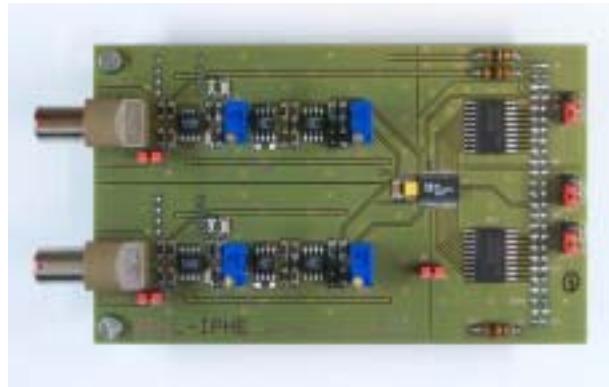


Figure 41 2 channels FADC card (by R. Frei).

The clock for both FADC cards can be adjusted in the range of (0-24) ns relatively to the RB2 module clock by the programmable delay unit.

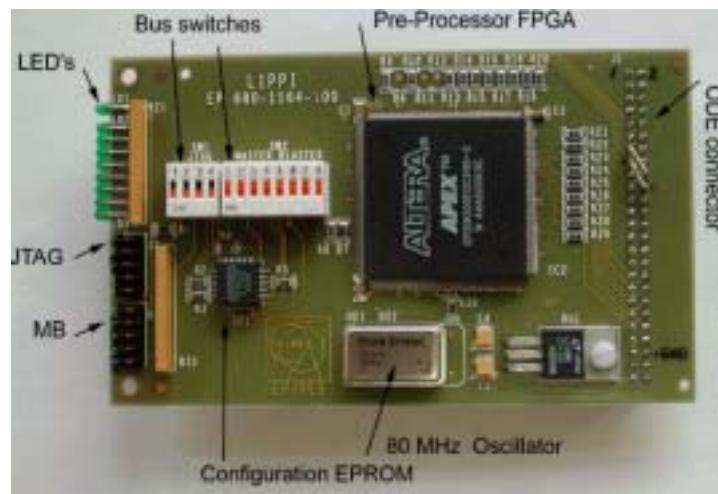


Figure 42 Level-1 trigger preprocessor interface prototype (by G. Haefeli).

The preprocessor interface to the Level-1 trigger is a very critical item because the quality of the data, sent to the Level-1 trigger defines the performance of the Level-1 trigger algorithm. A complete preprocessing algorithm (described in [44]) was implemented on the prototype card in APEX100KE FPGA, working at 80 MHz (Figure 42).

An ECS interface prototype, based on 68HC12D60 micro controller was designed and built [45]. It provides two I2C interfaces and JTAG interface. It allows a remote access to the RB2 board via serial interface and, optionally, CANbus interface. It can be used for reprogramming of different FPGAs (on the RB2 main board or on the Level-1 trigger preprocessor interface mezzanine card) or configuration EEPROMs via JTAG interface and downloading the parameters of TTCrx chip and internal registers in FPGA via I2C interface.

This interface was tested with the configuration EEPROM on the Level-1 trigger preprocessor interface and with the I2C interface in the RB2 main FPGA.

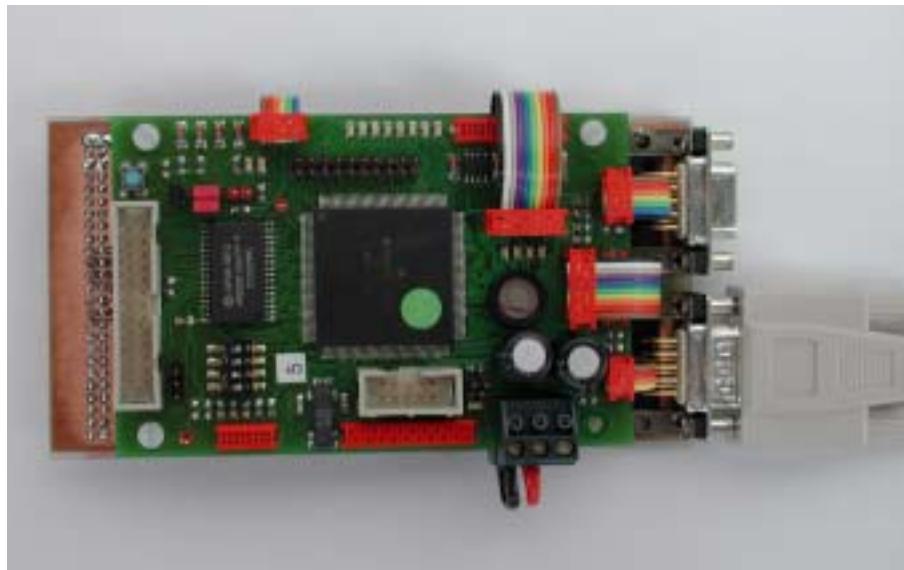


Figure 43 ECS interface prototype (by H. Dang, EIG).

The third prototype of the Level-1 board (referred as readout board three, RB3) has all the functionalities of the final board but reduced number of channels, 16 instead of 64. The specification of the module [32] was written before the actual design began in order to provide a starting point for the further design. It had undergone quite some changes during the RB3 design which will be reflected in the RB3 user manual.

The main purpose of the RB3 board is to check all implementation ideas and fixed the design parameters for the final module implementation. The RB3 board is not supposed to be used in the test beam environment and therefore only laboratory test setup has been prepared for the RB3 board tests.

The board is subdivided into 4 identical “data channels”, each processing data from four input links from one Level-0 chip. One “data channel” contains link receiver and FADC (1), synchronisation logic (2), preprocessor for the Level-1 trigger (3), Level-1 buffer (4) and data processor for the DAQ system (5) as shown on Figure 44.

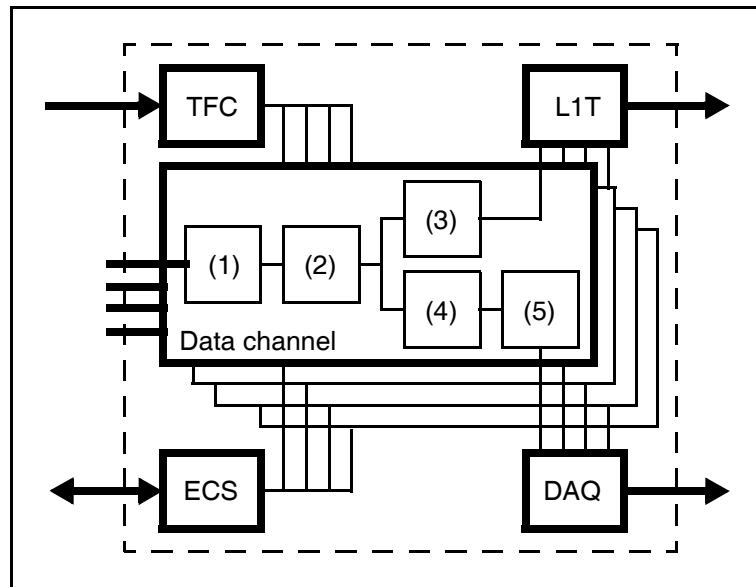


Figure 44 RB3 block diagram.

Four interfaces to the external systems - TFC, Level-1 trigger (L1T), data acquisition (DAQ) and experiment control (ECS) systems are common for all data channels and designed in such a way that may be used also for 16 “data channels” on the final 64-input Level-1 board. Some features of the RB3 may not be implemented on the final version if found unnecessary.

Similarly to the final design, the RB3 prototype is implemented as a 9U main board which has been specially designed to accept the plug-in mezzanine cards. The board uses standard commercial (non radiation hard or radiation tolerant) components. Some functional parts of the board (e.g. analog link receiver and FADC, Level-1 buffer, etc.) are implemented on daughter cards for possible different implementation without modification of the main RB3 board. The functional blocks of the RB3 board are:

- 4-channels FADC mezzanine card which contains the analog link receivers, line equalizers, amplifiers, and analog-to-digital converters. For each FADC card the main board provides 4 individually controlled Vref voltage and clock signals in order to allow individual control per input link. The card uses two connectors - one for analog power and Vref voltage and other for digital power, FADC clocks and 32-bit output data. The analog power on the main board are separated from the digital power and supplied from the individual connector.

- Synchronisation logic in the “data channel” (which processes the data coming from one Level-0 chip over 4 input links and digitized in one FADC card) and Level-1 trigger preprocessor (cluster finding), are implemented in the one FPGA.
- Level-1 buffer and DSP mezzanine card in the “data channel” provides data storage during the Level-1 trigger latency for the data from one Level-0 chip and data processing for the DAQ system after the Level-1 Accept decision.
- Interfaces to the Level-1 trigger and DAQ systems are implemented in separate FPGAs and uses S-LINK [48] interface specification for the data transmission.
- Interface to the TFC system includes the TTCrx receiver chip on the TTCrx board, Level-0 emulator, based on the Beetle chip, and control FPGA which provides an interface to the RB3 internal logic.
- Interface to the ECS system, based on the ARM microprocessor from Samsung, which allows to control whole board via Ethernet link (there is no VMEbus interface on RB3).

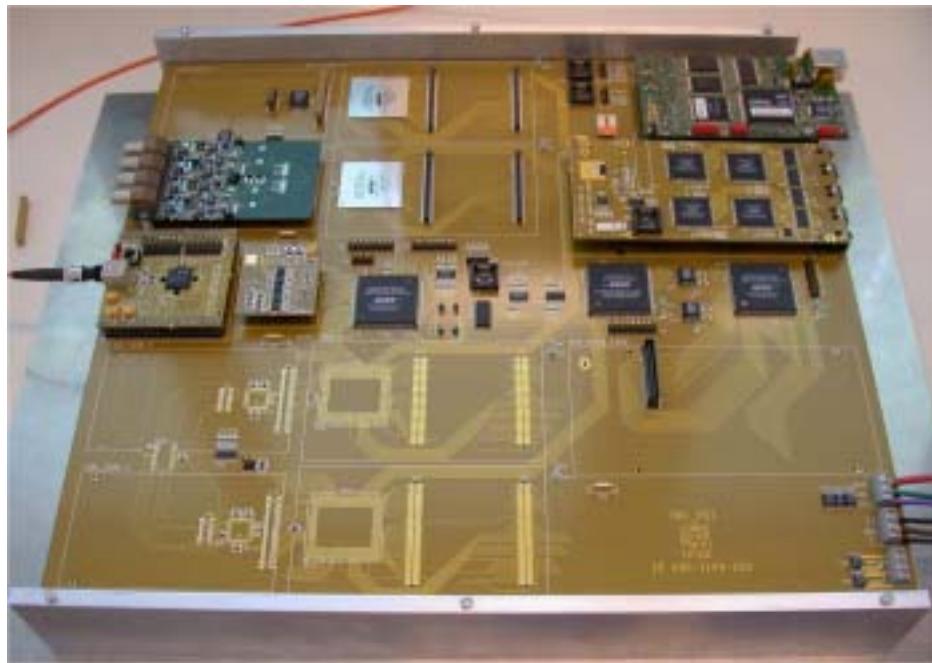


Figure 45 RB3 with TTCrx card, Level-0 emulator card, 4channel FADC card, ECS interface and output SLink card.

Two main boards (Figure 45) have been produced but only half of each board is equipped with component. This allow to reduce prototyping expenses but sufficient for the functional tests.

3.3.2 Tests on the Level-1 electronics prototype

The RB2 board, was used for several tests of different components of the VELO Level-0 electronics.

3.3.2.1 Test of the complete analog link

This test setup [35] was based on the RB2. A test has been performed using the SCTA128 output signal instead of a pulse generator. The meaning of the test was to provide initial measurements of the analog transmission performance using a more realistic setup.

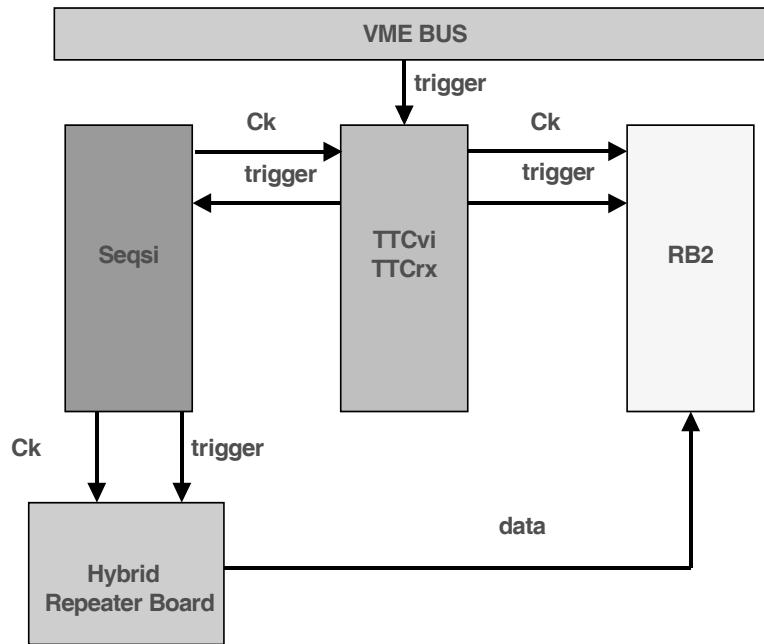


Figure 46 Analog link test setup with SCTA128 chip.

The main components of the setup (Figure 46) are:

- TTcvi and TTCvx. This VME boards are used as the trigger generator for the system. In response to a VME command the board issues a trigger command that starts the data acquisition.
- RB2 board. This VME board is equipped with FADC cards that digitizes the input signals at 40 Ms/s. Data acquisition is triggered by external trigger command: at the trigger the board start sampling the input and stores the results into a 2048 location FIFO. It is possible to set with 1ns resolution the delay between the system clock and the sampling clock.
- SEQSI. This VME board issues the sequence command to the SCTA128 at an external trigger. The SEQSI 40 MHz clock is also the common clock for the system.

Two set of measurements was done for comparison - with a short cable and a long cable. The Figure 47 shows the parameters of the short cable setup. The data are transmitted from the repeater board to the FADC in the RB2 via a flat cable and a bipolar LEMO cable. The FADC is not equipped with the line equalizer.

The SCTA128 is pulsed with a 4 fC charge, close to the one released in the silicon detector by one MIP, and is read-out at 40 MHz. The digitized signal value is about 22 ADC count over the pedestal.

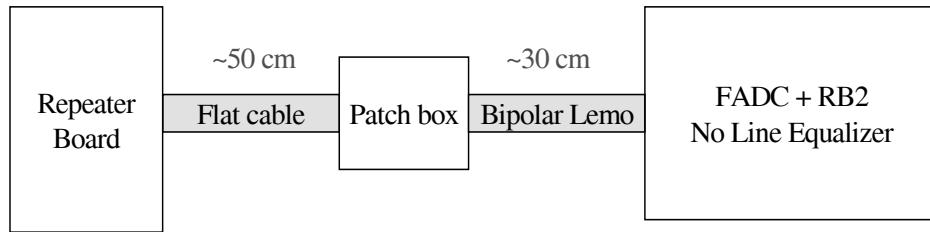


Figure 47 Short cable setup parameters.

The long cable setup schematic is shown in Figure 48. A 60 m cable is put between the repeater board and the FADC. A line driver is added to the amplifier chain because the repeater board line driver are not able to supply the necessary currents.

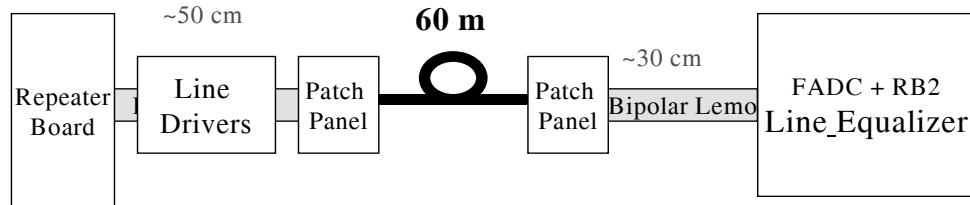


Figure 48 Long cable setup parameters.

The SCTA-128 has been pulsed with an 8 fC charge to compensate for the factor 2 effect and simulate one MIP signal. The sampling clock delay has been varied by 1 ns steps and allowed to explore the shape of the signal as seen in the FADC. In Figure 49 is reported the signal value as a function of the delay between the sampling clock and the SCTA128 clock. It is clearly visible a plateau region of about 10 ns where to sample the signal.

The raising time of the signal is ~7 ns. The signal value is ~ 20 ADC count over the pedestal value. The ~ 2 ADC counts difference between the signal in the long cable setup and the short cable setup was not expected: however, the systematic effect of the asymmetry of the line driver can be the source of the discrepancy

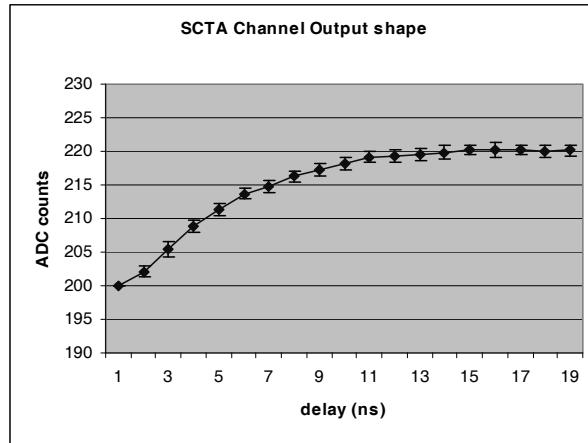


Figure 49 Signal vs. sampling time delay.

Additional check (Figure 50) has been performed on the noise and on the significance of the signal, defined as the ration between the signal and the signal RMS. The measured noise has an average value of 0.92 ADC count, which is of the same order of the one measured with the short cable setup. The signal significance is greater than 20 on the plateau region.

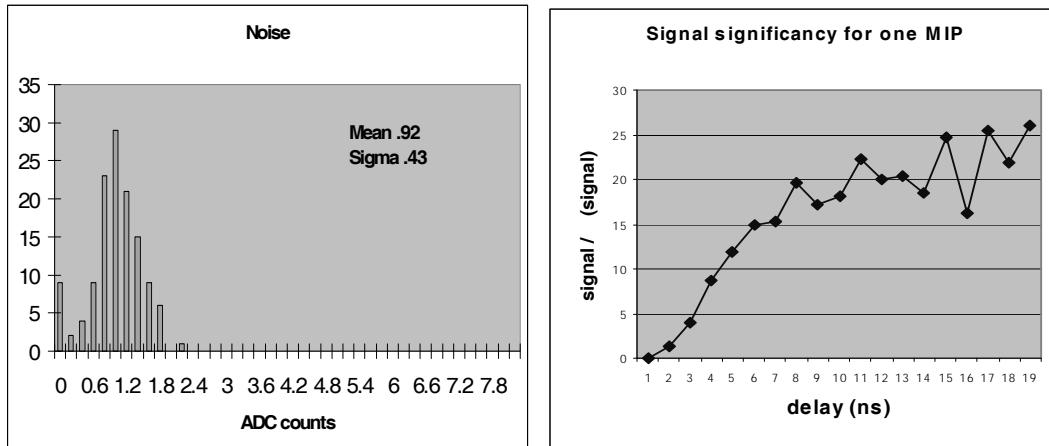


Figure 50 Left: noise distribution for the SCTA-128 chip with long cable setup; Right: Signal significance vs the sampling time.

3.3.2.2 Tests with the SCTA128 chip

First aim of this tests [49] was to test the Level-0 chips itself. In the summer 2000 VELO test-beam, the prototype sensors were equipped with SCTA128 chips.

The SCTA128 chips used were not tested by the manufacturer and a test system which is able to characterize the chip before the detector assembly was therefore required. The RB2 can be used as a data acquisition board for the test setup as it is capable of sampling the output sequence of SCTA128 at 40 MSample/s.

The other reason was to test the FADC card in the RB2 board. The SCTA128 chip is very similar to a possible future VELO Level-0 chip. In particular, the SCTA128 output after a Level-0 trigger consists of an analog sequence of the sampled channels with a rate that can be varied from 5 MHz to 40 MHz. The VELO Level-1 electronics has to digitize the analog data streams coming from Level-0 chips. This will be done by the RB2 prototype which carries up to two FADC mezzanine cards. The SCTA128 chip, therefore, can be used to test the performance of the FADC cards. The same setup was used as for the complete analog link test (Figure 46). The Repeater Board used in the test system supplies the analog and digital voltage to the Level-0 chip, and the reference voltage Vref. The value of Vref, as well as the analog and digital voltage, can be varied acting on a variable resistance and tested on a probe pin. The board translates the input commands (including the Level-1 accept), the reset and the clock from ECL to LVDS and routes them to the hybrid. Probe pins allows the signals to be monitored. The board provides line drivers that convert the analog FE chip output to a bipolar signal. It is possible to shift the signal baseline using a variable resistance on the board, in order to adjust the channel pedestal level to within the FADC dynamic range.

The SCTA-128 output signal dynamic range is 700 mV. In the FADC card the bipolar signal from the Repeater Board is converted back to the original SCTA-128 output signal. The gain of the total amplifier chain is set to 1. The output signal is added to a constant offset of 2 V, i.e. the FADC card 8-bit ADC chip AD9059 digitizes signal in the 2V - 3V range. The ADC conversion factor is $1V/256 = 3.90$ mV/adc count. The ADC linearity has been measured [50], using a voltage generator, to hold for the full ADC range. The measured voltage turned out to vary between samplings with a RMS up to 0.5 ADC counts. The RMS was found to depend on the voltage value. In the test setup the RB2 clock and trigger command is issued by the VME boards TTCvi and TTCvx. The TTCvi is used in VME trigger mode: the trigger command is issued by a VME command; the command is sent at the same time to the SEQSI through a NIM output and to the RB2 via the optical fibre as a trigger command to the TTCrx chip, encoded in the 40 MHz clock. The TTC-VI and TTC-VX system 40 MHz clock is provided by the SEQSI. The trigger command is synchronized with the system clock.

The SEQSI is a VME board which provides a programmable sequence of ECL signals at 40 MBit/s. Three ECL signals are sent to the SCTA-128 chip: the clock at 40 MHz, the reset (active low) and the command. Of the many features of the SEQSI board, the test setup uses the capability to provide a 40 MHz clock (used as the master clock of the system) and the capability to loop over an idle sequence and to switch to a data acquisition sequence when an external trigger is sent. The external asynchronous trigger is latched with the SEQSI master clock.

The SCTA-128 chips have been glued to ceramic hybrids. Two different kinds of ceramic hybrids have been produced: SCT3 and SCT6. SCT3 can be equipped with up to three SCTA128, while SCT6 can be equipped with up to six. In the SCT3 two of the three chips are read-out in a daisy chain, while one is read-out on its own. In the SCT6 all chips are read-out in daisy chain. A total of five SCT3 hybrids and two SCT6 hybrids has been fully equipped and tested. Some hybrids have been reworked in order to replace non-working chips.

The pedestal linearity and spread has been measured for all the chips. Figure 51 shows the pedestal distribution for a typical chip.

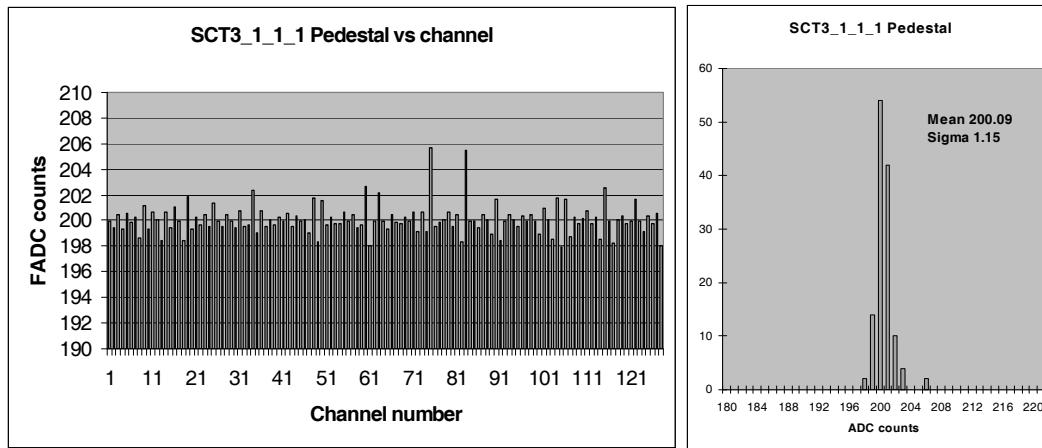


Figure 51 Left: SCT3_1 single-read chip pedestals. Right: pedestal distribution.

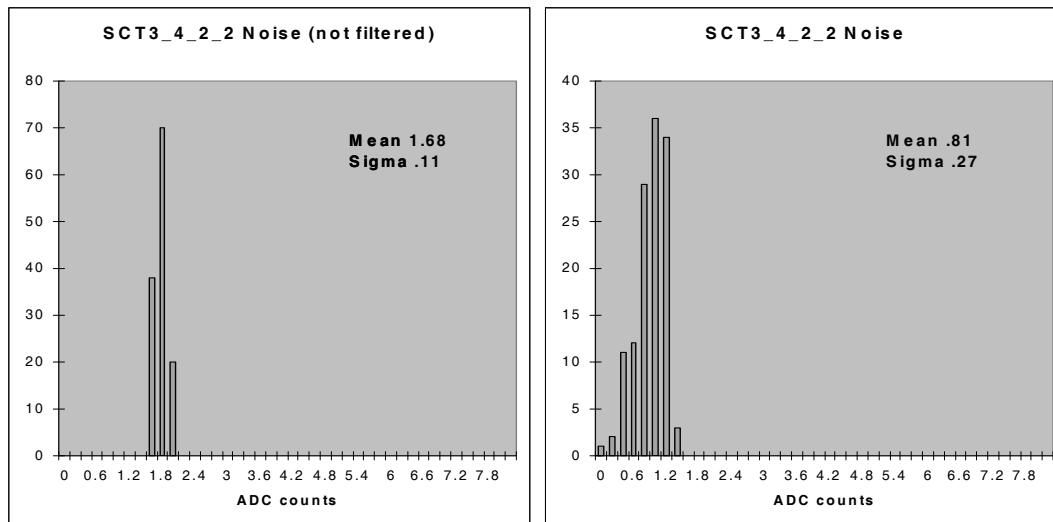


Figure 52 Left: Noise in adc counts for SCTA-128; Right: the same chip, but data are corrected by the median filter.

The channel noise is defined as the RMS of the pedestals. A median filter can be applied to the data: the effect is to reduce the RMS. Figure 52 shows the effect of the median filter on the noise measured in one SCTA-128 chip (SCT3_4_2_2).

The SCTA128 internal injection circuit has been used to pulse the preamplifier. Figure 53 shows the channel output vs. the injected charge. For large charges the gain (the ratio between the injected charge and the channel output) is smaller with a good linearity up to an injected charge of ~ 12 fC, a value that exceeds the typical 4 fC charge released by one MIP. Since the gain is only approximately linear, we have to choose a value of the injected charge at which we compute the gain. We choose a value of 7 fC, where the gain is still linear but above the charge released by one MIP.

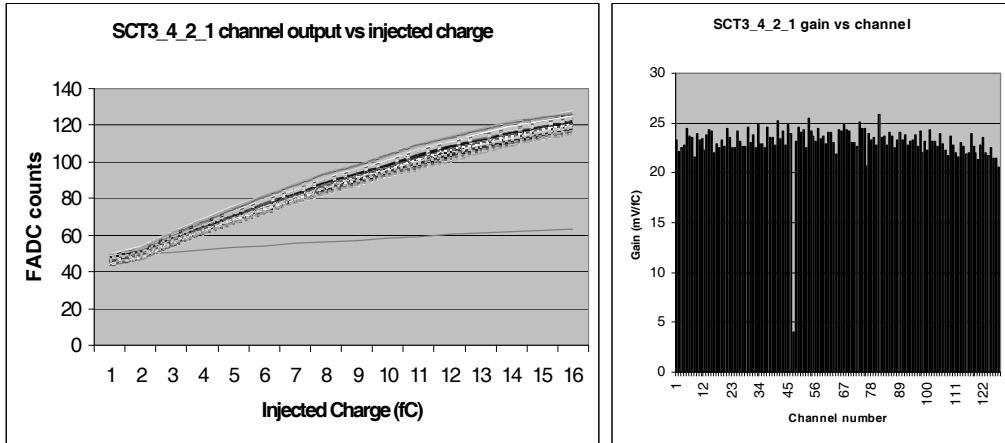


Figure 53 Left: Channel output as function of the injected charge. Each channel is represented by a line. Right: Gain distribution.

The typical measured gain value is of the order of 20 mV/fC. The gain uniformity and the number of dead channels varies from chip to chip.

3.3.2.3 Test of the VELO silicon sensor prototype

The Hamamatsu PR01-R 300 μm thick detector (VELO sensor prototype, Figure 54) was readout by a C-RAMS 10-bit ADC V550 from CAEN (Italy) in the summer 2000 test-beam. It has been also tested in our test setup [49]. The characterization of the Level-0 chips, which equip the detector, allows a comparison of the performance of the two systems. Moreover it was possible to obtain an absolute calibration of the RB2 FADC cards using test-beam data.

From the test-beam data measurements a value of 58 ADC counts as the most probable value of the charge Landau distribution for a MIP has been obtained [51]. A C-RAMS used in test-beam, with sensitivity range of 1.5 V, that implies a conversion factor of 1.5 mV/ADC count. Assuming that the most probable value of the Landau corresponds to 22000 e- for the 300 μm silicon sensor (but 16000 e- in the “LHCb light”) we obtain a conversion factor of 252 e-/mV. In terms of ADC counts, we have the following conversion factors: for the RB2 FADC card, 983 e-/ADC count; for the C-RAMS, 378 e-/ADC count.

Pedestals and noise for the hybrid, equipped with one SCTA-128 chip with no capacitive load, was measured. The pedestal spread is 1.14 ADC counts. The mean value of the measured noise is ~ 840 e- after common mode correction.

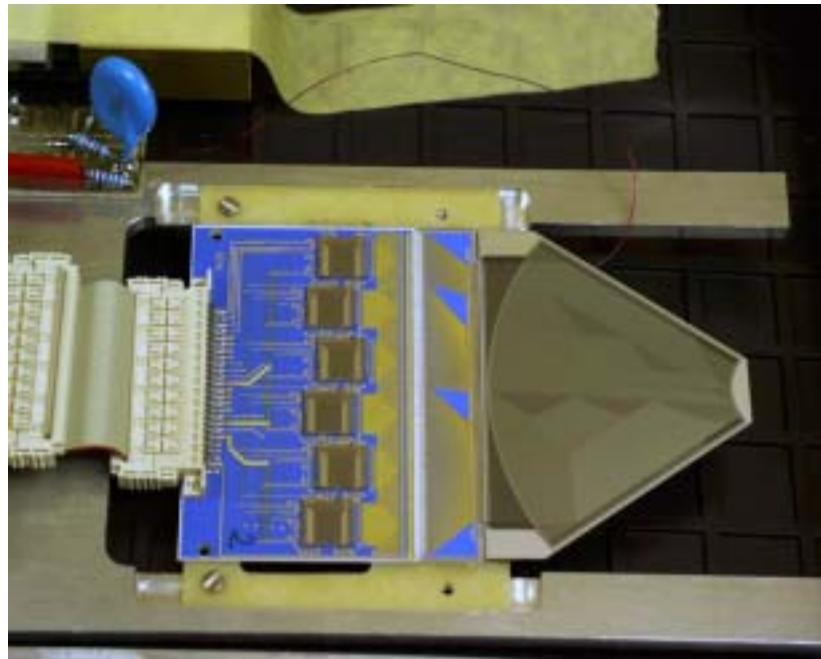


Figure 54 Hamamatsu PR01-R detector.

PR01-R detector was equipped with the SCT6 hybrid with two Level-0 chips connected to regions of the detector with different capacitance due to the different strip and routing lines lengths. In [52] a measurement of the capacitive load for PR01-R detector is reported: a value between 22 and 23 pF is expected to be for the first chip, connected to the longer strips, while for the second the capacitive load is expected to be about 15.5 pF. The effect, as seen in test-beam data, is to increase the noise in the first chip.

Except where is explicitly noted, all measurements have been done with the following settings:

- The preamplifier current is 200 μ A, the shaper current is 40 μ A, the read-out amplifier current is 70 μ A.
- The silicon sensor is reverse-biased at 90 V.
- The read-out speed of SCTA-128 is 40 MHz.

Noise measurements in laboratory are of particular interest since the noise measurements in the test-beam have been performed with the SCTA128 read-out at 5 MHz, while the laboratory measurements are done at 40 MHz rate as will be the case for the final VELO.

Figure 55 shows the noise vs. the channel number for the two central chips. The noise shows a dependency on the channel number, which can be mapped into a dependency on the capacitive load which increases with channel number for the first chip, while it is somewhat more constant in the second chip. Channels in the range 0 to 127 (first chip) are bonded to strips of 3.5 - 4.5 cm length.

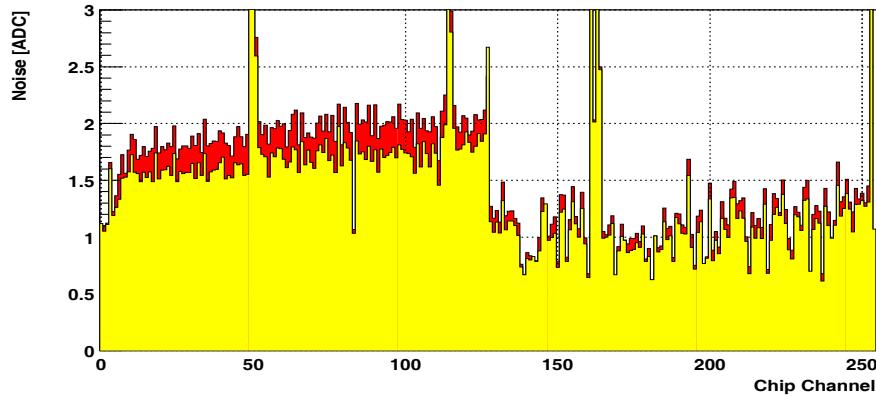


Figure 55 Noise vs. channel number.

Those in the range 128 to 256 (second chip) are bonded to 0.6 - 0.8 cm long strips. The mean ENC is 1646 e- for the first chip and 1033 e- for the second chip.

Figure 56 shows the noise vs. channel number for the same detector, as measured in a typical test-beam run. The noise value is in ADC count: the corresponding mean ENC value is about 1600 e- for the first and 1100 e- for the second chip.

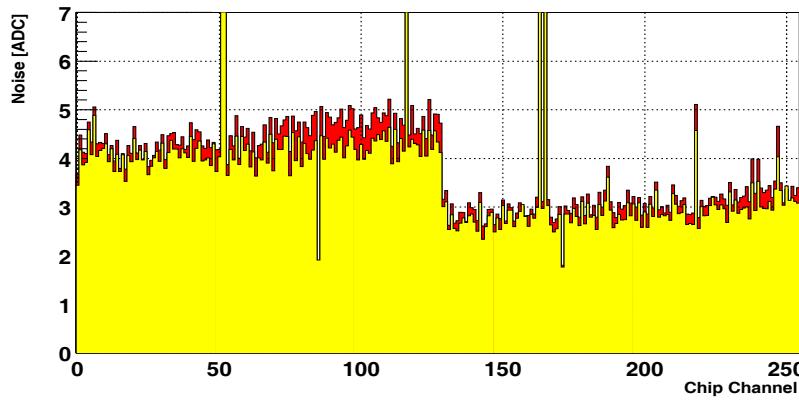


Figure 56 Noise vs. channel number for a typical test-beam run.

The mean noise measured varied between different runs. In the noisy runs the mean value of the ENC increased up to 1800 e- (1300 e-) for chip 1 (chip 2). To reduce the sensitivity of the system to external influences, a proper shielding is foreseen in the next version of the FADC cards. Using the measured noise ranging from 1650 e- to 1810 e- for the first chip and from 1000 e- to 1300 e- for

the second chip, and the signal for one MIP measured in test-beam, we can extrapolate, for a 300 μm thick n-on-n r-type detector, a signal to noise value between 17 - 22 for the inner region and 12 - 13 for the region with strip length between 3.5 cm and 4.5 cm.

3.3.2.4 Test of the complete readout chain

During year 2001 two test setups [53], based on RB2 board, were prepared in Lausanne and CERN. The two main goals of these new measurements were:

- study of the FADC clock adjustment and distribution,
- study of signal to noise of the complete readout.

Test setup in Lausanne uses pulses produced by a laboratory pulse generator and signals provided by a SCTA128 chip. In one test, half of the SCTA128 chip channels were connected to a silicon sensor (an LHCb Inner Tracker ladder prototype of 20 cm length). Every other channel was bonded. At CERN various tests were performed with another RB2 board. In the laboratory, the RB2 was employed to read out an ALICE sensor [55] connected to a pair of SCTA128HC Level-0 chips. Only a quarter of the chip channels were bonded. The S/N was measured both by using the SCTA self-calibration mode described below, and from a comparison to test-beam data. A further test was done by connecting the RB2 to a Hamamatsu PR01 prototype sensor.

The SCTA can be programmed for self calibration: charges of 4, 8 or 16 fC can be injected every 4 channels. Four runs are required for the complete calibrations of the 128 channels. 4 fC roughly corresponds to the average charge deposited by a minimum ionizing particle in a 300 μm Si sensor. The bonded channels see a load capacitance of about 20 pF which results in a larger noise on these channels but also a small pedestal change (the bonded channels are 1-3 ADC counts higher than unbonded ones).

The FADC mezzanine cards of RB2 can compensate for DC level offsets at the input and the gain can be adjusted within $\sim 30\%$. During the present tests the whole gain was set in such a way that 20 ADC counts corresponds to about 1 MIP. We have done tests with a 7m (short) and 65m (long) cable. In the latter, line driver and receiver (based on the HFA1212 chip) were inserted, with line equalization calculated on the basis of the cable parameters.

FADC clock adjustment and distribution

The RB2 board contains a programmable delay unit (PDU) which is used to delay the clock for both FADC cards in the range of (0-24) ns relatively to the main RB2 board clock (Figure 57). The 5-bit control code for the PDU is defined in the control register. This feature is used to shift a measuring point of the FADC to the best value of the input analog signal.

The FADC chip AD9059 and output register 74F245 have a specified minimum and maximum output propagation delay (t_{PD}).

Their difference defines a timing region (~7 ns), where output data are not guaranteed to be stable. This timing region (and corresponded control codes for the PDU) shall be excluded from the measurements. The FPGA on the RB2 main board has minimum input setup time of 5.7 ns for the data to be stable relatively to the RB2 board clock. The FADC chip has aperture delay t_A of 3 ns (a difference between FADC clock edge and real measuring time M). This two parameters define the correspondence between the PDU control code and the real measuring point on the input analog data relatively to the RB2 board clock [43].

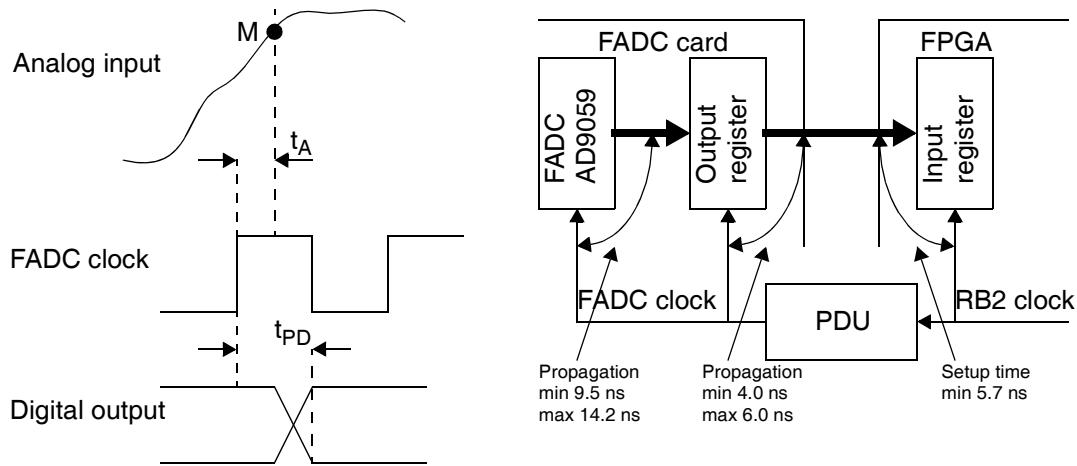


Figure 57 FADC - FPGA timing diagram.

The “dead” time region may be reduced by removing (unnecessary) output register on the FADC card but can’t be eliminated completely. It presence doesn’t allow to exploit whole range of the PDU, which restrict the test measurements. In practice, this may have a negligible effect if the “dead” time doesn’t fall on the sampling region of the input analog signal.

The PDU implementation of the FADC clock adjustment, while simple, create two clock domains, which results in the “dead” time zone. This can be avoided by shifting complete board clock, common for the FADC and the main board, relatively to the input analog signal and not only FADC clock. This is possible due to the build-in feature of the TTCrx receiver chip - the output clock may be delayed in steps of 0.1 ns relatively to the input clock from the TFC system. An adjustment of each individual FADC clock in a small range may be still implemented using separate PDU per FADC (or a similar device, e.g. 4-channel PHOS4 delay chip [56]).

This solution is implemented in RB3 prototype together with an improved board clock distribution scheme. The clock distribution network is implemented as a “tree” with the TTCrx chip is a source. Zero delay clock buffers (e.g. CY2308 from Cypress Semiconductor) funout one clock signal into multiple clock signals with zero delay and very low skew between the outputs. Series termination technique and clock transmission line impedance matching is also used to improve the clock signal quality.

Signal to noise study at Lausanne

The intrinsic noise of RB2 board itself was found very small. With the input analog line, terminated by a passive plug, the offset of one channel can be adjusted in such a way that the ADC converts to a unique digital value almost all the time. A conservative estimate of the noise is the rms of a rectangular distribution < 2 digits wide: 0.58 ADC counts. No noticeable change is observed when the passive termination is inserted after a short or long line.

An example of a dynamic test of RB2 is shown in Figure 58. Pulses corresponding to the response of the SCTA for a charge deposition of ~ 4 fC are sent directly to the RB2 (the cable was shorter than 1 m). The duty cycle of the waveform obtained from a generator was similar to the one of the SCTA calibration mode and synchronous with the readout clock. The rms width of the distributions is of about 0.8 ADC counts. The generator-intrinsic noise is 0.3 - 0.4 ADC counts.

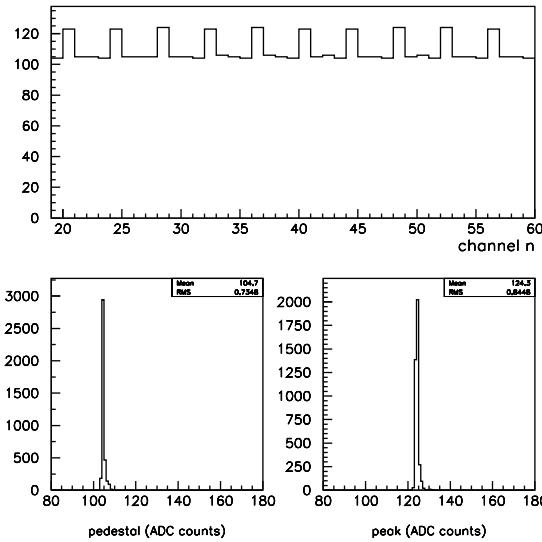


Figure 58 Response of RB2 to a rectangular waveform simulating the SCTA calibration signal: a pulse of 25 ns followed by 3 empty slots. The pedestal and the peak amplitude are presented in the two bottom figures.

Significant amount of noise appears only when the F/E chip and the repeater board with line driver are connected to RB2. The two top plots of Figure 59 shows the ADC response correlation between two unbonded channels (left) and two bonded (right). A short (7 m) cable was used. A pedestal value was subtracted from each reading in such a way that the average is zero for all channels. We can notice that roughly the same amount of correlated noise (CN) appears in the two plots. We also observe that the bonded channels have a larger random noise (RN), because of the capacitive load. A simple CN correction was applied which consists for each event to subtract from each channel the average amplitude registered by a set of channels.

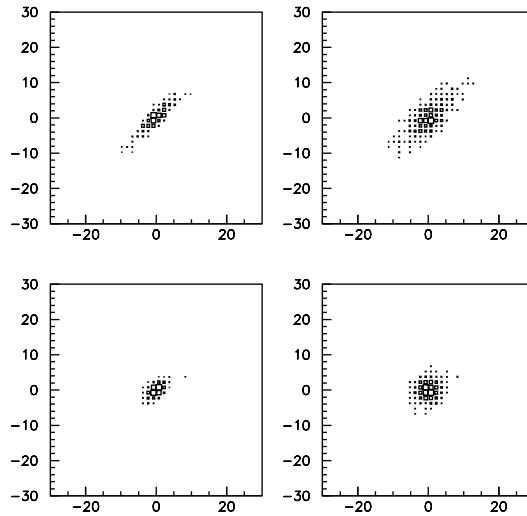


Figure 59 Correlated noise with a 7 m cable: Amplitude of channel $i+2$ vs amplitude of channel i . The plots at the left correspond to two unbonded channels, bonded are at the right. The bottom plots presents the correlation after the procedure of common mode correction has been applied.

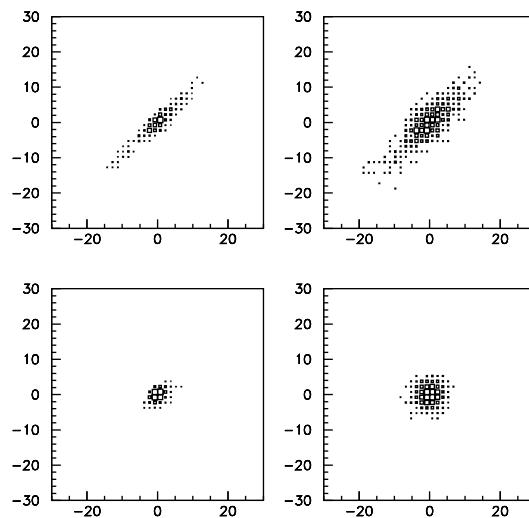


Figure 60 Correlated noise with a 65 m cable: Amplitude of channel $i+2$ vs amplitude of channel i . The bottom figure presents the correlation after the procedure of common mode correction has been applied.

In this analysis the 128 SCTA channels were subdivided in 4 regions of 32 channels. Moreover bonded and unbonded channels were kept separated.

In conclusions 8 sets of 16 channels are used in calculation of the CN correction. During this correction procedure the RN worsen by the factor of square root of $(1+1/N)$, where $N=16$ is the number of channels in the set.

Similar results are shown in Figure 60 for a long line. The RN did not change while the CN is somehow larger but can still be efficiently corrected. Some tests have been done to better understand the origin of the CN and to determine the better strategy to reduce it. In RB2 the analog power is derived from the VMEbus digital power lines, regulated and filtered (in RB3 and in the final product independent power lines will be provided by the backplane). We modified the RB2 board to accommodate an independent power supply for the analog boards but no noticeable difference was observed both in the CN and RN.

The calibration and S/N studies were done by the injection of a known charge at the level of the SCTA. 4 fC were injected every four channels. For these tests we use unbonded channels. The phase of the clock at the input of the FADC was set at the scope in such a way that the rising edge of the clock was close (~ 5 ns) to the end of the analogue pulse. We also did "delay curves" as will be explained later but we found that the setup at the scope was quite correct.

Figure 61 shows some results with a short line after CN correction. The top two plots are the average amplitude distributions for 0 and 4 fC injected every 4 channels, 32 in total. The averages are calculated over a run of 1000 events. The corresponding rms distributions are shown in the two plots in the middle, while the S/N are given on the bottom. The S/N is defined as the average value obtained at 4 fC (~ 1 MIP) divided by the rms width of the pedestal (i.e. the amplitudes recorded at 0 fC). For these particular runs, an average S/N of 15 ± 1 was obtained with the short line while 16 ± 2 was obtained with a long line.

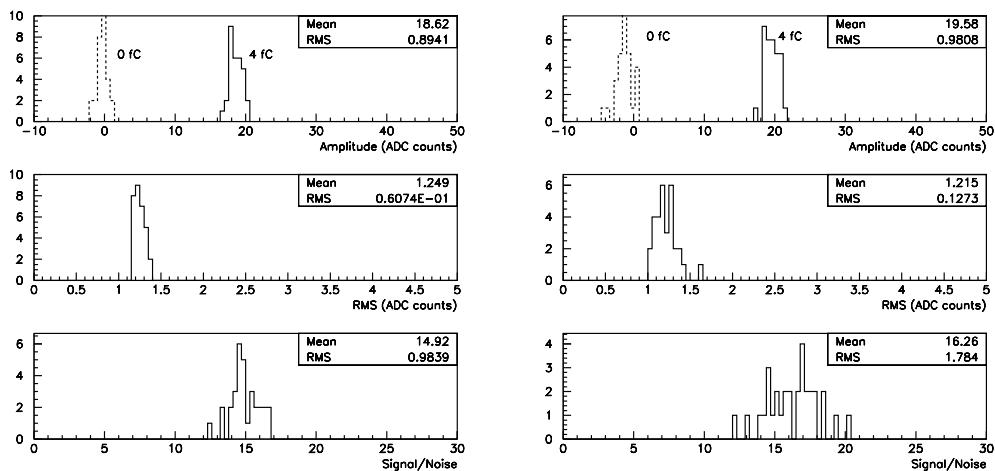


Figure 61 Left: amplitudes (top), rms (middle) and signal/noise (bottom) distributions for unbonded channels for a 7 m cable. 4 fC are injected to simulate 1 MIP charge deposition. Right: same for a 65 m cable.

Signal to noise study at CERN

At CERN (measurements done by U. Parzefall) the RB2 was used to read out an ALICE silicon sensor with 4 cm long strips, only a quarter of the chip channels were bonded which allows to measure the noise with and without capacitive load. Two different signal definitions were applied for the S/N measurements. In the standard laboratory tests, the signal was given by a 4fC charge injected with the self-calibration mode. In this way, a S/N of 19 ± 2 was obtained after common mode noise correction for the unbonded channels. With the capacitive load, the S/N reduced to 14 ± 2 .

An alternative way to define the signal in a laboratory environment is to calibrate the RB2 against a known data acquisition system, where signal and noise are well defined, by reading out the same sensor in both systems, and comparing the unique shape of the pedestal distribution for all strips. The shapes are fitted using an ADC scale factor and an overall voltage offset as the free parameters. We calibrated the RB2 against the C-RAM system, running at 5 MHz, which was used to read out the same ALICE sensor in a beam test. By using the scale factor obtained in the pedestal fit, MIP signals recorded with the same sensor could be converted into the equivalent signal for the RB2. We take into account that the most probable value for charge deposited by the MIP is 3.5 fC, and rescale the signal to 4 fC. This allows comparison with the other S/N measurements, which are based on the injection of 4 fC with the SCTA self-calibration mechanism. In this way, S/N values of 17.4 ± 2 and 12.9 ± 2 were measured for unbonded and bonded channels respectively.

The test beam measurement of the S/N was performed in the CERN SPS with a beam of MIPs, consisting of 120 GeV pions and muons. Here, the RB2 was used to read out a VELO PR01-R prototype sensor, equipped with 6 SCTA chips. On this sensor, all chip channels were bonded to strips, hence the S/N can only be measured with capacitive load. S/N values ranging from 11 to 15 were obtained for the individual chips, which are connected to strips of varying length. The noise was found to scale well with the capacitive load from the length of the individual strips. Averaging over all working chips, an S/N of 12.7 ± 1.5 was measured. Scaling this value to a 4fC charge deposition gave a S/N of 14.5 which was compatible with the measurements in the laboratory.

Discussion and conclusion

The RB2 boards, tested at Lausanne and CERN, showed S/N values ranging from 13 to 19, in different tests, using a range of signals and sensors. This value did not deteriorate when going to the long transmission line, which proves that such 60 m long analog links are feasible. A summary of the results from the various S/N measurements with the RB2 is given in Table 1. The S/N for unbonded channels is in reasonable agreement. For bonded channels, the S/N shows additional variation due to the different capacitive loads of the sensors. The Equivalent Noise Charge (ENC) in electrons, corresponding to the S/N measurements is also shown.

Sensor Signal	Inner Track Calib. pulse	ALICE Calib. pulse	ALICE MIP (calib.)	VELO MIP (direct)
S/N unbonded channel S/N bonded channel	15.5 n/a	19 14	17 13	n/a 14.5
ENC unbonded channel ENCbonded channel	1600e ⁻ n/a	1300e ⁻ 1800e ⁻	1450e ⁻ 1950e ⁻	n/a 1700e ⁻

Table 1 Summary of the measured S/N and noise values, reading out SCTA128-HC chips with the RB2 at 40MHz. The signal is defined to be a charge of 4 fC. The noise is given as the equivalent noise charge in electrons.

We have to notice that fluctuations of the order of one unit in the average S/N ratio are found for different runs. This might be due to the RF pollution in the experimental area but no formal proof has been established. We have studied the behaviour of RB2 when the clock phase is changed with respect to the input signal (Figure 62). We observe that the best value of ~ 16 is found in a “plateau” region between 20 and 25 ns.

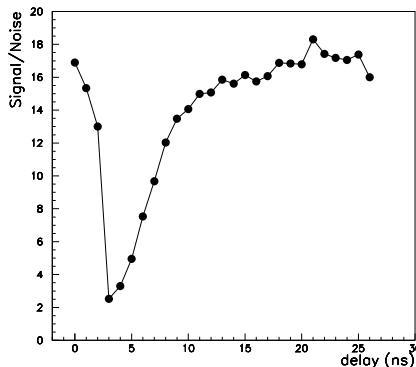


Figure 62 The S/N ratio variation with the clock phase.

In conclusion, the RB2 prototype of the Level-1 electronics for the VELO has been tested in the laboratory using signals produced by a generator or from an SCTA128 chip connected to a repeater board. We have seen that the S/N of at least 15 can be achieved with a short (7 m) line, connected to the SCTA, for unbonded channels. A similar result has been obtained with a long (65 m) line by the introduction of a line equalizer. The common noise was not negligible during these tests and was corrected by a simple procedure. We have observed that for the particular SCTA chip we used in Lausanne behaviour at 40 MHz is worse than when its multiplexer is running at 5 MHz. The S/N of 15 at 40 MHz improves to more than 23 when the readout speed is lowered to 5 MHz. The bandwidth reduction due to the insertion of a long line after compensation introduces a cross-talk of about 10% between adjacent channel.

3.3.2.5 RB2 signal to noise study

In August 2002 the complete S/N measurements [54] of the four RB2 boards, running at 40 MHz, were done with a non-irradiated 300 μ m thick *n*-on-*n* silicon detector, used in previous tests. The goal was to obtain similar results with the new setup (S/N was 15-20 with the C-RAM system, running at 5 MHz). For this purpose the detector was connected to different RB2s and different FADC cards were characterized (Figure 63). To obtain enough statistics several runs were taken and about 400000 events were accumulated.

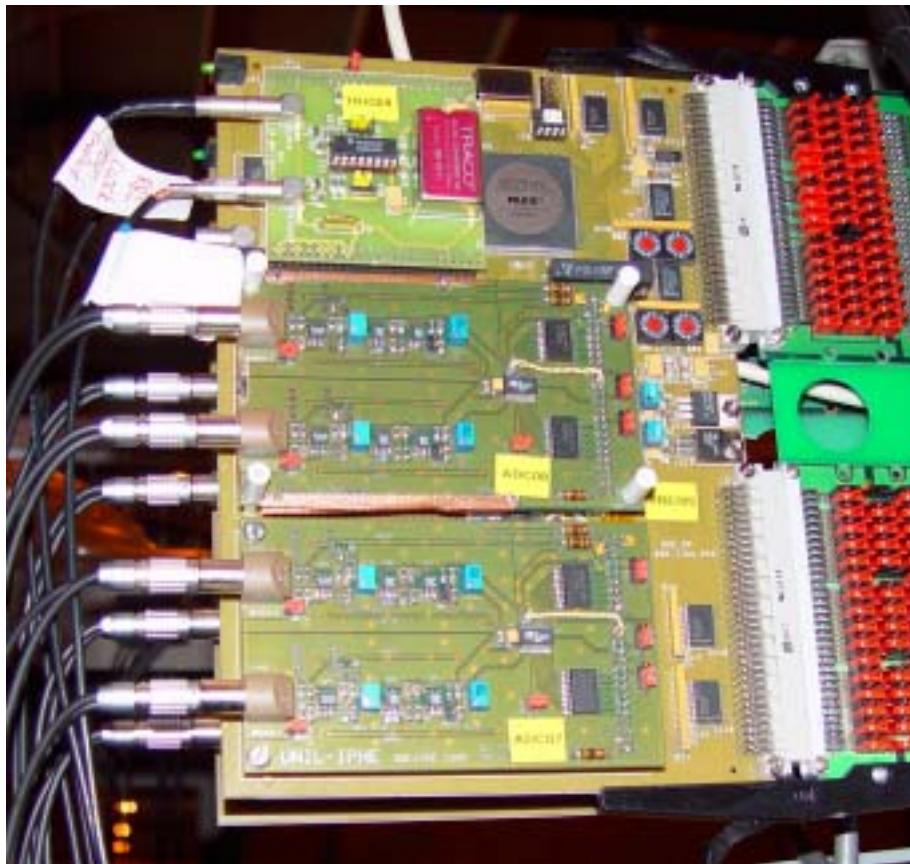


Figure 63 RB2 board with 2 FADC cards in the test-beam.

Preliminary analysis shows that S/N of 25 was achieved which is comparable with the S/N measured with the 5 MHz readout. However, different combinations of RB2 with the FADC cards behave differently - on some of them noise increased by factor of 2.

4 VELO Level-1 electronics integration

The VELO Level-1 electronics doesn't work in isolation, it is a component of the overall LHCb electronics, trigger and data acquisition. It must conform to the defined requirements for the LHCb Level-1 electronics [14] and it shall interact in a defined way with the other parts. Some system aspects of the VELO Level-1 electronics are discussed in [36], [37] and [59]. They include, among others, system synchronisation, error detection and reporting and system resets.

The VELO Level-1 electronics supply preprocessed data to the LHCb Level-1 trigger system and zero-suppressed data to the DAQ system. It operates under control of the Timing and Fast Control system and Experiment Control System.

A possibility of stand-alone operation of the VELO Level-1 electronics, independent from other detector systems, is provided by a partitioning possibility of the overall LHCb DAQ/TFC/ECS system. Therefore, no local data acquisition or control facilities are foreseen for the VELO Level-1 electronics after its integration in the LHCb electronics, trigger and data acquisition.

4.1 Timing and synchronisation

The VELO Level-1 electronics in LHCb, as well as in other LHCb sub-detectors and other LHC experiments, follows a synchronous pipeline model at Level-0 and asynchronous data buffer model at Level-1. For a proper operation of the Level-1 electronics synchronisation at different levels and in different contexts has to be achieved and monitored. The VELO Level-1 electronics specific discussion on timing and synchronisation can be found in [36] and [37]; general overview of the timing and synchronisation in LHC experiments are given in later article [57]. The Level-1 electronics operation is based on the assumption that at the input of every processing stage (e.g. analog to digital conversion, digital data processing, data storage) data are synchronized and belong to the same bunch crossing (the same event).

In first instance it requires a stable clock signal equally phased in every location of the Level-1 electronics. However, the phase of the clock signal, distributed to many destinations via TFC system, may vary in a range of a few nanosecond. In order to compensate for the clock phase variations during clock distribution, a programmable delay lines are introduced at clock destinations. From other hand, variations in the analog signal shape or variation in the cable propagation delay may require adjustment of the clock signal at some stages (e.g. in analog to digital conversion - to select the best signal sampling point, in data links - to compensate for the delay difference) which results in re-synchronisation of the local clock relatively to the global system clock. At these points, the system has to be synchronized again.

Moreover, missing or adding one clock cycle may result in incorrect data assignment to the bunch crossing by the control logic in the Level-0/Level-1 electronics. These “synchronisation” errors has to be detected and, if possible, corrected or recovered and reported.

Several timing and synchronisation issues should be considered during the VELO Level-1 electronics design [36]:

- the FADCs on the Level-1 board may need a possibility of the adjustment of their clock phase to shift a measuring point of the FADC to the best value of the input analog signal (and, in some cases, to compensate a difference in cable lengths of the input analog data links from different part of the VELO detector, which may goes up to 2-3 m or 10-15 ns) - FADC clock adjustment,
- the beginning of event data in the continuous incoming stream of analog levels from the analog data link has to be defined in the Level-1 electronics in order to separate individual events, as there is no any additional synchronisation signal (or “data valid” signal) from the VELO Level-0 electronics to the Level-1 electronics - event synchronisation,
- errors during Level-0 electronics operation may lead to synchronisation errors (data coming from different parts of the Level-0 electronics, which have to be associated with the same event, may belong to different events) which have to be detected and an error recovery mechanism has to be established - synchronisation error detection.

4.1.1 FADC clock adjustment

Two mechanisms will be exploit on the VELO Level-1 board in order to set a proper measuring point of the FADC:

- complete board clock, common for the FADC and the main board, may be shifted relatively to the input analog signal using the build-in feature of the TTCrx receiver chip - the output clock may be delayed in steps of 0.1 ns relatively to the input clock from the TFC system. FADC clock remains the same as the global board clock.
- an adjustment of each individual FADC clock in a range of (1-24) ns will be implemented using 4-channel PHOS4 delay chip. In this scheme, two clock domains (FADC and digital logic) are created and a FIFO buffer is placed between the FADC and the digital logic in order to synchronized these two clock domains.

The clock distribution network an the Level-1 board will be implemented as a “tree” with the TTCrx chip as a source. Zero delay clock buffers with zero delay and very low skew between the outputs will be used to distribute the clock on the board. Series termination technique and clock transmission line impedance matching is also used to improve the clock signal quality.

4.1.2 Event synchronisation

The input to the Level-1 module from the Level-0 electronics is a continuous incoming stream of analog levels from the analog data link. The Level-1 module control logic has to define the first sample of the 32 analog samples block in order to separate individual events.

The identification of the first sample may be done using a Level-0 emulator (FEE) which provides timing prediction of the arrival of the first sample from the 32 analog samples block. From the timing and synchronisation point of view VELO Level-0 and Level-1 electronics are driven by the same clock and Level-0 accept signals from TFC and may be considered as completely synchronous system with deterministic behaviour. The behaviour of the Level-0 electronics, therefore, may be predicted in the Level-1 electronics using the FEE (implemented as a real Level-0 chip or emulator of a Level-0 chip control logic in FPGA).

The FEE is set to the same modes of operation and receives the same control signals as the real Level-0 chips. It provides:

- a data valid signal, which indicated arrival of the first sample of the event data,
- emulated values of the pipeline number to check the consistency of the data from the Level-0 electronics.

On the RB3 board the FEE is implemented with a real Beetle chip. On the final board FEE implementation will be defined by the Level-0 chip used by the VELO detector (SCTA_VELO or Beetle).

4.1.3 Synchronisation error detection

From a synchronisation point of view, in an error free system, all data from different parts of the Level-0 electronics belongs to the same Level-0 accepted event. After a synchronisation error, the data coming from the part of the FEE which is “out of synchronisation” could be associated with the wrong event. A possible origin of such errors in the Level-0 electronics could be missed or fake fast control signals (reset, clock, Level-0 accept) which drive the Level-0 chip pipeline, derandomiser and output multiplexer. This could happen in the TFC system or in the Level-0 chips and may result in corrupted data from a single Level-0 chip (internal chip error) or from a group of Level-0 chips (e.g TTCrx chip error). In order to detect errors, every Level-0 accepted event is tagged in the Level-0 electronics by an unique identifier - the Level-0 chip pipeline number. The error detection is performed in the Level-1 electronics by

- cross-checking pipeline numbers from different Level-0 chips,
- cross-checking pipeline numbers from the Level-0 electronics and the FEE.

The pipeline number is an internal Level-0 chip pipeline counter driven by clock which follows the pipeline write counter with a specified latency and stored internally on Level-0 accept to be used as a read-out pointer. The counter is 8-bits wide and is reset by the Level-0 reset signal. The pipeline number depends on all fast control signals (clock, reset, Level-0 accept) and therefore may detect all synchronisation errors.

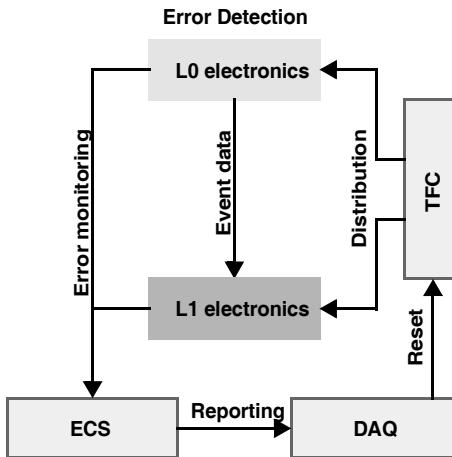


Figure 64 Error detection and recovery.

Upon detecting an error the synchronization logic masks (set to zeroes) event data for the Level-1 trigger. The error flag is also written in the Level-1 buffer together with the event data. Synchronization errors, detected in the Level-1 electronics, are monitored by the ECS system and reported to the DAQ system [37] as shown on Figure 64.

In order to recover from errors, the global periodical resetting of the electronics has been chosen rather than local re-synchronization since it guarantees the uniform behaviour of the whole experiment. Possible scenarios [58] include resetting of only the Level-0 electronics, Level-1 electronics or both.

The resetting frequency is calculated using error detection rate in the electronics. The reset signal is send to all LHCb electronics from the central place via the TFC system and may be synchronized to the gap in the LHC orbit to reduce event losses.

4.1.4 System resets

VELO Level-1 electronics must react to LHCb reset signals. They are sent to the Level-1 electronics (to the TTCrx chip) via the TFC system from the Readout Supervisor which is controlled by the Level-0 and Level-1 trigger systems and the LHCb ECS system. All event identification counters (bunch counter, Level-0 and Level-1 event counters) are reset via the TFC system broadcast command.

Level-0 Reset

Level-0 Reset resets complete Level-0 electronics including Level-0 pipelines and derandomizers. It is defined to occur at the end of the large bunch gap so Level-0 pipelines can be cleared with a minimum event loss. It will be sent to the sub-detector Level-0 electronics such that it can also be used to reset bunch counters related to the input of the Level-0 pipeline.

When issued for error recovery the Readout Supervisor will insure that the Level-0 derandomizers are empty (to prevent confusing the Level-1 electronics when no Level-1 Reset is issued). The sub-detector Level-0 electronics must be capable of starting with normal functionality within a few clock cycles after this reset. The first Level-0 trigger accept will only be issued after 160 clock cycles (Level-0 latency).

In the VELO Level-1 electronics Level-0 Reset is used only to reset the Level-0 chip in the front end emulator on the Level-1 board. It resets Level-0 pipeline pointers, Level-0 derandomizer pointers and stops any running Level-0 chip readout process.

Level-1 Reset

Level-1 Reset resets the whole Level-1 electronics including Level-1 buffers and all derandomizers. This reset will normally be issued only together with a Level-0 Reset (but not for all Level-0 resets). The Level-1 electronics must be capable of accepting events from the Level-0 electronics within 160 clock cycles after this reset (Level-0 latency). The first Level-1 trigger will not be transmitted to the Level-0 before 1-2 ms (Level-1 latency) to allow DSP based zero-suppression units sufficient time to be ready to accept new event data.

The Level-1 Reset is used to reset the control logic (counters, pointers, state machines, error flags) and to reset the Level 1 Buffer read/write pointers and to restart the DSP algorithm of the Level-1 electronics without its re-initialisation via ECS system. Parameters, which are downloaded via ECS system, are not affected by the Level-1 Reset (e.g. TTCrx configuration).

4.2 Level-1 trigger system interface

The Readout Unit [38] is an interface between the VELO Level-1 electronics and the processors in the farm (Figure 34). Each RU receives data from four VELO Level-1 boards (event “fragments”, or event “messages”) over four links, one per the VELO Level-1 board, and builds a subevent (concatenates event fragments into one output message). A specification of the interface between the VELO Level-1 electronics and the Readout Unit defines:

- level-1 trigger preprocessor algorithm specification,
- an electrical interface and a data transfer protocol,
- data format, required by Level-1 trigger.

An initial interface specification in [16] are being revised in order to reflect the latest ideas and changes in both RU and the overall Level-1 trigger system design.

4.2.1 Level-1 trigger preprocessor (by G. Haefeli, UniL)

Level-1 trigger PreProcessor Interface (L1PPI) in the VELO Level-1 board [44] prepares the data for the trigger algorithm, collects the data on the Level-1 board and transfer them to the Level-1 trigger via S-LINK. The parameters of the Level-1 trigger system preprocessor are set via ECS interface on the Level-1 boards. The tasks performed in the preprocessor are:

- Pedestal subtraction - each channel of the detector has an offset (pedestal) which can be determined from uncorrected detector data during a special mode run. The pedestal data, 1 byte per detector channel, can be down-loaded via ECS interface to a dedicated RAM block on the L1PPI and are subtracted from the raw data in the first stage of processing.
- Faulty channel masking - if a detector channel develops a fault, it is necessary to have the option of ignoring it in all processing stages. For example, a channel which oscillates and returns large values, would distort the common mode calculation and also would be counted as a hit. The faulty channel mask can also be determined using uncorrected detector data. The mask (1 bit per detector channel) can be down-loaded via ECS and is stored in a LUT on the preprocessor. With this mask the value of the faulty channels after pedestal subtraction is set to zero, assuming that this value has the least impact for the subsequent processing.
- Common mode suppression - In the present preprocessor prototype we have studied only Linear Common Mode Suppression algorithm (LCMS) which has the form $\text{noise} = a + bi$ (where i is the channel number). The common mode correction implementation is flexible in order to accommodate other algorithms in case of need.
- Hit detection - a hit is defined as a channel with an amplitude above a threshold value. The 8-bit threshold values are stored for each channel in a RAM block on the preprocessor and can be down-loaded via the ECS interface
- Cluster encoding - The low occupancy of the vertex detector makes zero suppression an obvious way to reduce the data. Moreover the Level-1 trigger algorithm requires 'clusterized' data. Several different cluster encoding schemes were studied. The present proposal is to form only clusters of one or two hits, clusters of three or more hits are split in several clusters.

The most demanding part of the L1PPI is the common mode suppression stage. The LCMS algorithm has been simulated and implemented in hardware in the L1PPI prototype.

The algorithm is applied on each set of 32 detector channels (detector data, coming to the Level-1 board over one input analog link). It consists of two identical iterations, in which a linear common mode is calculated. The algorithm subsequently identifies the hits and passes the information to the cluster encoding stage. The complete description of the LCMS algorithm can be found in [44].

An FPGA based L1PPI prototype [44] of the preprocessor has been realized to demonstrate that the LCMS algorithm can be implemented in hardware at no prohibitive cost, to show that the designed and simulated algorithm also works when implemented in hardware and to show that the timing requirements can be met. The hardware implementation for the LCMS has been tested and successfully compared with an identical C coded software version of the algorithm.

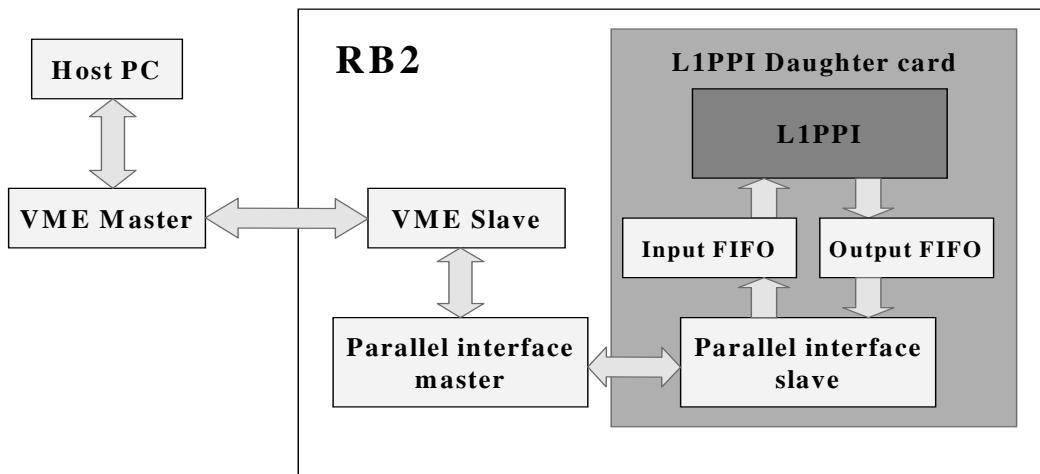


Figure 65 RB2 with the L1PPI prototype.

The prototype was realized as a plug in card for the RB2 board (Figure 65). An Altera APEX EP20K100KE FPGA was used to implement the algorithm. The FPGA, used in this prototype, provides sufficient programmable logic to perform the LCMS on 128 detector channels (detector data, coming to the Level-1 board over 4 input analog links from one Level-0 chip). The FPGA is operated at a frequency of 80 MHz to allow multiplexed processing. This reduces significantly the resources used in the FPGA. We have proved that eight 200k gate size FPGA's can process the LCMS for one Level-1 board (64 input analog links) and that the FPGA can stand the required I/O rates. The latency of the common mode suppression stage of 10 μ s dominates the total latency of the preprocessor (about 16 μ s).

The increasing densities of the FPGAs, availability of special processing blocks inside FPGA (ALU, multipliers, etc.) and increasing number of pins on the package may allow to implement a complete Level-1 trigger preprocessor for the detector data, coming to the Level-1 board over 32 input analog links in a single FPGA.

This FPGA may also include some other functionalities of the Level-1 board, like synchronisation error detection and significantly simplify the layout and size of the digital part of the Level-1 board.

4.2.2 Electrical interface and data transfer protocol

The S-LINK [48] interface specification defines the electrical interface (connector, signal levels and timing) and the data transfer protocol which includes data flow control. It also defines a mechanical dimensions of the physical layer card in case it implemented as a mezzanine card, however, it can be integrated on the main board. All 32-bit words transmitted by the S-LINK are accompanied by a control/data bit. A data block is defined as the data words between two control words (words with control bit equal to “1”). The data flow control feature of the S-Link is not used for the data transfer between the VELO Level-1 electronics and Level-1 trigger Readout Unit. Therefore a simplex S-LINK implementation may be used for this application which uses a “push” protocol without data flow control.

The S-LINK interface specification does not describe the physical link itself. A maximum clock frequency for the S-LINK interface is defined as 40 MHz (the data transfer rate on the physical link may differ). An LVDS transmitter/receiver cards [60] may be used as a physical layer cards. This card works with the SLINK interface clock of 20 MHz and provides 80 MByte/s data transfer rate at a distance up to 15 m (the Level-1 trigger system is located in the same counting room as the VELO Level-1 electronics). In case this data transfer bandwidth is not sufficient, we can use an optical 2.5 Gbit/s S-LINK transmitter/receiver physical layer card HOLA [61], which works with the SLINK interface clock of 40 MHz and provides 160 MBytes/s data transfer rate. This card requires only one duplex fibre and is not limited by short distances.

4.2.3 VELO - Level-1 trigger data format

For every event, accepted by the Level-0 trigger, event data are processed by the preprocessors on the VELO Level-1 boards. A message, containing event identification information and an information about found VELO clusters (particle ‘traces’ in the silicon sensors), is sent to the Level-1 trigger system via S-LINK (one link per Level-1 board). If no clusters are found in the event, an “empty” message is still sent to the Level-1 trigger system in order to keep overall system synchronisation.

Message size

Event data from the Level-0 electronics arrive to the Level-1 board at maximum event rate of 1.11 MHz (maximum allowed readout time for the Level-0 electronics is 900 ns per event).

In case the Level-1 board sends a constant size messages to the RU, the maximum number of 32-bit words per message (including control words) from the Level-1 board is 36 for the maximum 40 MHz clock frequency of the S-LINK interface.

In reality, the message size is variable and depends on the number of VELO clusters found (which, in turn, depends on the thresholds in the cluster finding algorithm). In [44], the average number of clusters per 60° part of the VELO sensor ranges between 6 and 10 (Figure 66), therefore for the 180° VELO sensor these numbers may be 3 times higher. Hence, in average, the message from the VELO Level-1 board to the RU contains information about 20 to 30 VELO clusters. Taking 16 bit/cluster plus several additional words/message results in 15 to 20 words per message in the average.

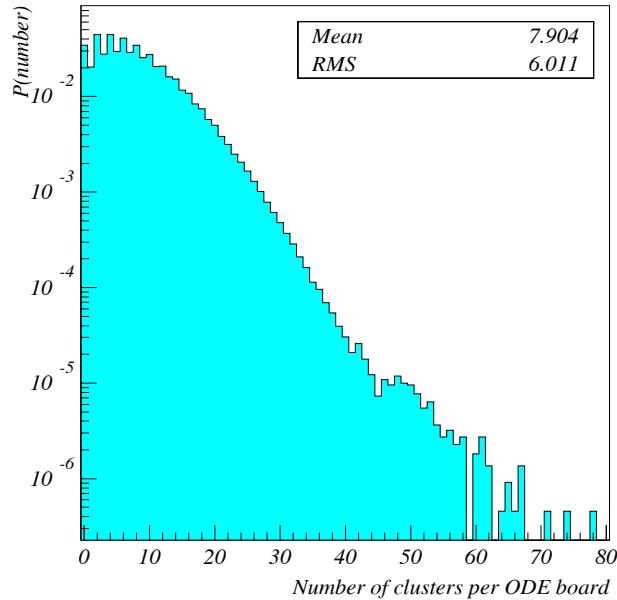


Figure 66 Number of clusters per 60° VELO sensor.

Occasionally, more clusters may be found per event. This fluctuation of the message size can be absorbed by the derandomizers in the VELO Level-1 boards and RUs. Additionally, the number of clusters per event, sent to the RU from one Level-1 board, is truncated and can't exceed the maximum number (64, 128 or 256) set via the ECS system.

Data format

The data format for the VELO/Level-1 trigger interface shall satisfy requirements of the S-LINK and the Level-1 trigger system (hardware and algorithm). It shall:

- conform to the S-LINK data transfer protocol: data block shall be embedded in two control words, event data format shall be adapted to the 32-bit S-LINK data width,

- contain necessary event identification information (event number), data source identification (VELO Level-1 board number), present the data in convenient way for the Level-1 trigger algorithm execution and handle error conditions,
- introduce a minimum overhead for “empty” messages, or messages with a little information and allow message “merging” in the RU without data duplication.

Attempts to define the data format were made in [62], [16], [38], [32] and [59]. A Subevent Transport Format (STF) for messages from the Velo Level-1 board to the Level-1 trigger (Figure 67) consists of the SLINK header and the SLINK trailer words that encapsulate an event data block.

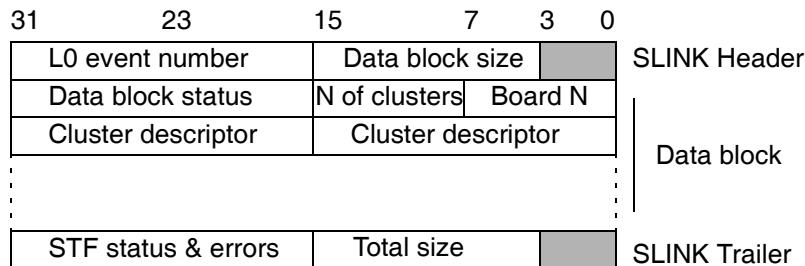


Figure 67 Velo/Level-1 data format.

During subevent building in the RU, the contents of the data block is preserved. The contents of the SLINK header and the SLINK trailer words may be modified by the RU during subevent building.

The SLINK header contains the following information:

- Data block size (12 bit) - a number of 32-bit words in the data block (recalculated in the RU during subevent building).
- Level-0 event number (16 bit) - an event identification from the TFC.

The SLINK trailer contains the following information:

- Total size (12 bit) - a number of 32-bit words in the message: data block plus two words - header and trailer (recalculated in the RU during subevent building).
- STF status & errors (16 bit) - zero at the output from the Velo Level-1 board, may be modified by the RU during subevent building.

The first word of the data block contains the following information:

- Board N (8 bit) - Velo Level-1 board number (LSB may be used to distinguish between boards, connected to the ϕ and r silicon sensors). Board number is set by the ECS system.

- N of clusters (8 bit) - a number of 16-bit cluster descriptors in the data block. For the odd number of cluster descriptors one empty descriptor is added to the data block.
- Data block status (16 bit) - VELO Level-1 board dependent information (not modified in the RU during subevent building). It may includes, for example, truncation flag, etc.

Each consecutive word of the data block contains two cluster descriptors, defined by the Level-1 trigger algorithm needs, e.g.:

- Cluster address (13 bit) - a position of the first strip of the cluster on the silicon sensor.
- Cluster width (2 bit) - defines a number of strips in the cluster (0 - one strip, 1 - two strips, 2 - three strips, 3 - more then three strips).
- Pulse height (1 bit) - indicates, which threshold was used to find cluster (a parameter, set via the ECS system).

For the odd number of cluster descriptors, one empty descriptor is added to the data block (without increasing the total number of clusters, N).

4.3 DAQ interface

The interface to the DAQ system on the VELO Level-1 board sends the zero suppressed (after processing by the DSPs) and formatted data to the DAQ system (Network Processors) over the DAQ link.

DAQ data processor

This functional part of the VELO Level-1 board performs the following tasks:

- extracts the event data from the Level-1 buffer upon receiving the Level-1 trigger decision from the TFC system - discard events, rejected by the Level-1 trigger, or retain accepted events for further processing and performs zero-suppression and detects clusters,
- (optionally) calculates the pedestals and noise for each of 256 detector channels and communicate them to the ECS system and sends non zero-suppressed data to the DAQ system in the special mode of operation or periodically,
- encapsulates the output data and sends them to the DAQ system via DAQ link.

The parameters of the DAQ data processor parts are set via ECS interface on the Level-1 boards. After a positive Level-1 trigger decision, the data are transferred from the Level-1 buffer to the Level-1 derandomizer buffer, where they remain until the DAQ data processor is ready to accept the next event. The output of the DAQ data processor is kept in the output buffer until it is transferred to the LHCb data acquisition system.

The DAQ data processor performs a similar data reduction as the Level-1 trigger preprocessor but with a better precision and lower thresholds since it has about a factor 10 more time available. A small fraction of the event data are recorded without zero-suppression for offline monitoring of the pedestals and noise per strip.

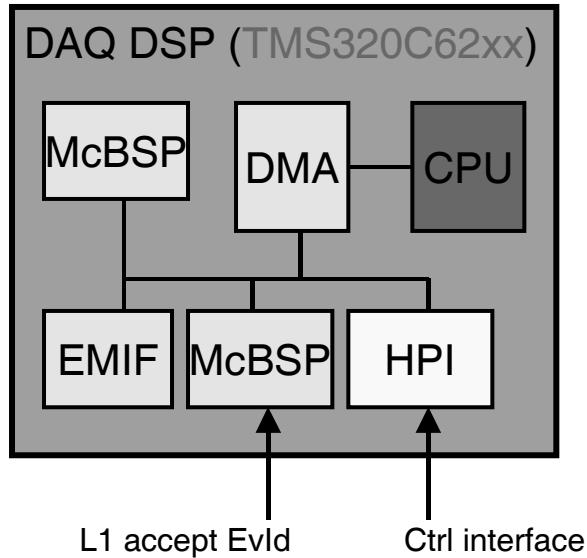


Figure 68 DSP based DAQ data processor (by G.Haefeli).

In order to evaluate the execution time for the zero-suppression algorithm in the DAQ data processor, a prototype of the DAQ data processor has been implemented using low cost TMS320C6200 DSP from Texas Instruments (Figure 68).

An interface to the DAQ link is defined as the S-LINK for the time being. A Gigabit Ethernet (GbE) as a DAQ link technology from the output of the Level-1 boards was adopted for the DAQ Level-0 Multiplexers and the Readout Units.

Data format

The DAQ link data format is not fixed yet. It consists of DAQ link transport format that encapsulate an event data block. The following information shall be included in the event data block (similarly to the Level-1 trigger data format):

- event identifier,
- size of the data block,
- VELO Level-1 board number, set by the ECS system,
- a number of cluster descriptors in the data block.

Each cluster descriptor containing a complete information about the found cluster:

- position of the first strip of the cluster,

- number of strips in a cluster (including neighbouring strips, if any)
- 8 bit FADC information for each strip in the cluster,
- Level-1 trigger information - a bit saying that this cluster was sent to the Level-1 trigger.

4.4 ECS interface

The VELO Level-1 electronic boards have to be connected to the LHCb ECS system for configuration, control and monitoring, as discussed in [63].

The majority of the VELO Level-1 board logic is implemented in the FPGAs, there are also static memories and some other components, like the TTCrx chip and the programmable delay chip and FPGA configuration EEPROMs. The ECS interface on the Level-1 board shall provide a possibility of:

- Read/write access to internal registers inside FPGAs and memories (LUTs, SRAMs, EEPROMs) inside and outside of FPGAs.
- Read/write access to the internal registers of the other components on the board.
- On-board FPGA configuration (directly or via EEPROM re-programming).

The ECS controller on the Level-1 board has to interact from one side with the components on the board and from other side with the ECS sub-detector controller. The on-board interfaces are already defined for some components (e.g. I2C interface for the TTCrx chip and the programmable delay chip, JTAG interface for the configuration devices). They shall provide an access to the commercial chips, FPGAs and memories. In LHCb The CC-PCs will be used to provide the necessary local intelligence on an electronics board [13]. They are connected to the central ECS via a conventional Ethernet and allow accessing the various components of the board.

To insure a correct identification and configuration of electronics modules, each ECS interface must have three identification registers:

- a board type identifier must define the module type,
- a revision number must define the hardware revision number,
- a serial number must uniquely identify the module.

The content of these identification registers should in general be hardwired by jumpers or solder bridges on the module itself. These three identification registers should be found on the three lowest addresses in the local ECS address space, to insure a consistent identification of modules across the whole system. In case a module has software or FPGA configuration data residing in permanent memories (e.g. Flash), it must be possible to read its revision number via the ECS interface.

An important part of the system monitoring performed by the ECS during running is to observe the error status of all Level-1 modules. It is therefore important that the Level-1 electronics makes extensive error status information available via its ECS interface. Error conditions that only have affected individual events should increment error counters. Fatal errors can be signalled with simple error flags. All error counters and error flags must be reset by the Level-1 Reset but must also be resetable directly via the ECS interface itself.

5 Perspectives and conclusions

The design of the final Level-1 board for VELO will be based on the experience, acquired with the previous prototypes, mainly with the RB3. The final implementation of the interfaces to the external systems (Level-1 trigger, DAQ, ECS), shall be frozen in order to implement them on the VELO readout board.

One of the major questions is an achievable density of the board - 32 or 64 channel. This is mainly defined by the implementation of the analog part of the board and power consumption of the digital part. 32-channel implementation results also in doubling of the number of crates, housing the Level-1 boards, and the number of links to external systems.

Functionality of the final design will be similar to the RB3 prototype but some functional part may be implemented differently. New generation of high density FPGAs (with increased number of logic elements, large memory blocks on the chip and embedded DSP blocks) allows much higher integration of the digital logic on the Level-1 board. Just a few large FPGAs may accommodate all functionality of individual components of the present prototype (synchronization logic, Level-1 trigger preprocessor, DAQ zero suppression, link interfaces, etc.). High density and high access rate memories (e.g. - Quad Data Rate, QDR memory) allows Level-1 buffer implementation with just a few memory chips.

A possible layout of the 64-channel board is drafted on Figure 69. The analog part is implemented on two separate 32-channel analog mezzanine receiver cards. They receive analog and digital powers from the main board. The 32 input analog links are brought to the analog mezzanine receiver card via connector located on the mezzanine card.

The digital part of the board may be implemented in a few FPGA - four of them provide all processing for board (16-channels each) and one FPGA provides an interface to the TFC and ECS systems and links to the Level-1 trigger and DAQ systems. This implementation greatly reduce the number of interconnection between individual parts of the board (and the number of traces on the printed circuit board).

In this option there is no mixture of the analog and digital parts layout, but the half of the main (digital) board is almost empty. As a variant of this layout, the design may be simply divided in two halves - analog and digital boards with only digital connections between two parts. This solution may reduce the cost of the printed circuit board for the digital part of the board.

The interfaces to the LHCb common systems (TFC and ECS) are standard LHCb interfaces (TTCRx chip for the TFC system and CC-PC for the ECS).

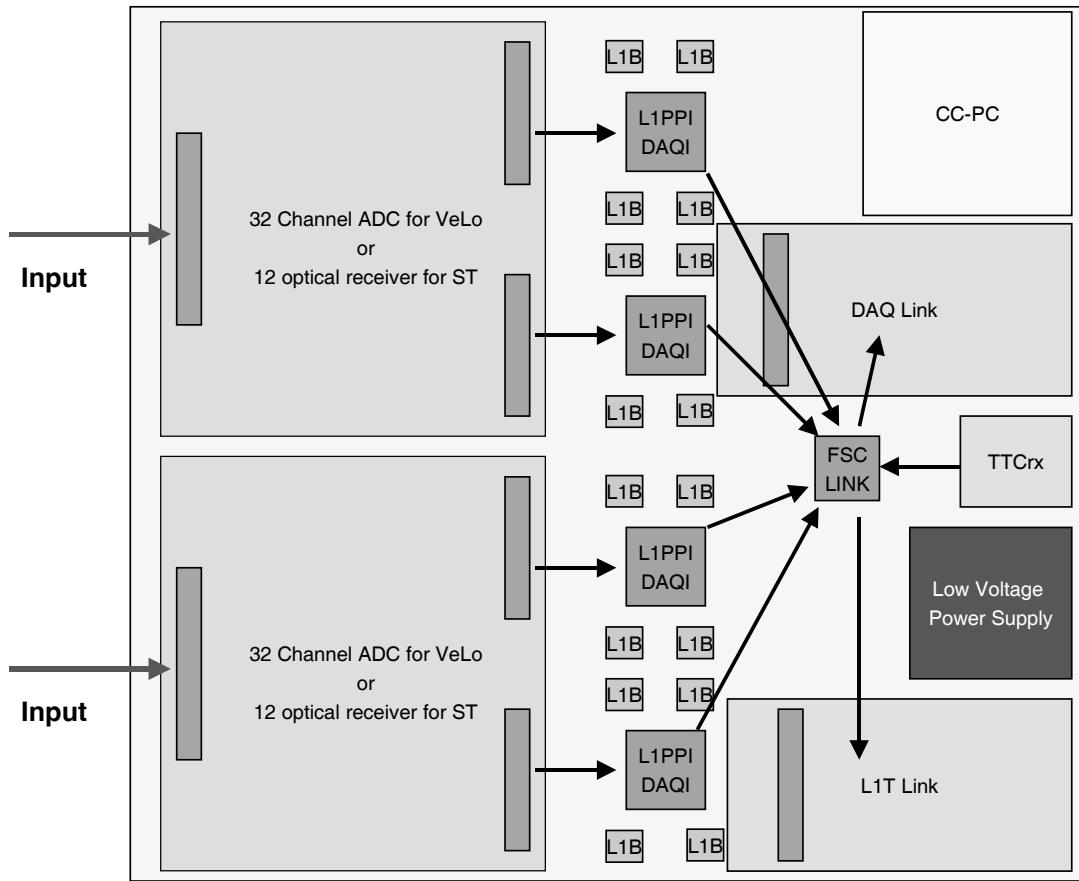


Figure 69 Possible layout of the final board.

We could also mentioned that the **digital** part of the VELO Level-1 board may be seen as a standard building block in the LHCb Level-1 electronics which contains such standard parts as the Level-1 buffer, DAQ processor and interfaces to LHCb common systems (TFC, ECS and DAQ). This features of the VELO Level-1 board may result in other application of the VELO Level-1 board in LHCb as discussed below.

5.1 Common Level-1 board for several subdetectors

Several subdetectors in LHCb use similar Level-1 electronics for readout their Level-0 electronics, namely VELO, Inner and Outer Trackers. All these detectors supply data for the Level-1 trigger. Therefore, an idea of a common Level-1 board may find sufficient support [64].

This may be a common digital mother board which may accept different mezzanine receiver cards for input links (analog or digital). It will contain standard functional parts of the LHCb Level-1 electronics:

- sufficient amount of digital logic resources for the synchronization, trigger and DAQ data processing,
- level-1 buffer and standard link(s) to the trigger/DAQ CPU farm,
- standard interfaces to external LHCb systems (TFC, ECS).

The digital logic will be implemented in FPGAs, which will be configured according to the application. The firmware (FPGA configuration) may be detector specific (e.g. for the Level-1 trigger preprocessing and DAQ zero suppression). Advantages of having such a common boards are obvious (manpower, cost, maintenance).

The following detector specific requirements shall be accommodated by the common Level-1 board:

- number of detector channels per board which is convenient for each subdetector (this is mainly defined by the detector layout, e.g. 2048 detector channels for the VELO, 3072 channels for the Inner Tracker),
- detector data link implementation (the best would be a single link for everybody) between detector Level-0 and Level-1 electronics (e.g. - VELO uses the analog electrical data link, Inner and Outer Tracker both use a digital optical data link),
- Level-0/Level-1 data check (synchronization, etc.) - which information for these operations will be sent by the detector Level-0 electronics and which will be required from TTCrx chip,
- number of detector channels for the Level-1 trigger preprocessing and for the DAQ zero suppression and algorithms to be implemented in the FPGAs,
- data formats in the Level-1 buffer, for Level-1 trigger and DAQ.

The development of this common Level-1 system, apart from the data link(s) and Level-1 board design, will require also selection of the crate and backplane as well as power supplies.

Test facility for the common Level-1 board debugging and laboratory tests will be set up. It will contain all necessary components of the LHCb environment. Data generators may be used initially to emulate the Level-0 data directly at the input of the digital board. A common test setup has to be established in several places. Certain efforts will be required for integration in LHCb TTC/ECS/DAQ environment.

For example, for the Inner Tracker this standard digital board will be equipped with two Inner Tracker specific input data receiver cards for the optical links. Each card receives input data from twelve fibres (digitized data from 12 Beetle chips) therefore, the complete Inner Tracker readout board receives data from 24 Beetle chips (3072 detector channels). A possible layout of the Inner Tracker Level-1 board and the receiver cards is shown on Figure 70.

Synchronization of the Inner Tracker Level-0 and Level-1 electronics and will be implemented in the same way as for the VELO electronics in spite of different data link implementation. The GOL serializer chip and the TLK2501 demultiplexer both provide a fixed data transmission latency which makes the optical data link equal to the electrical from the latency and synchronization task point of view.

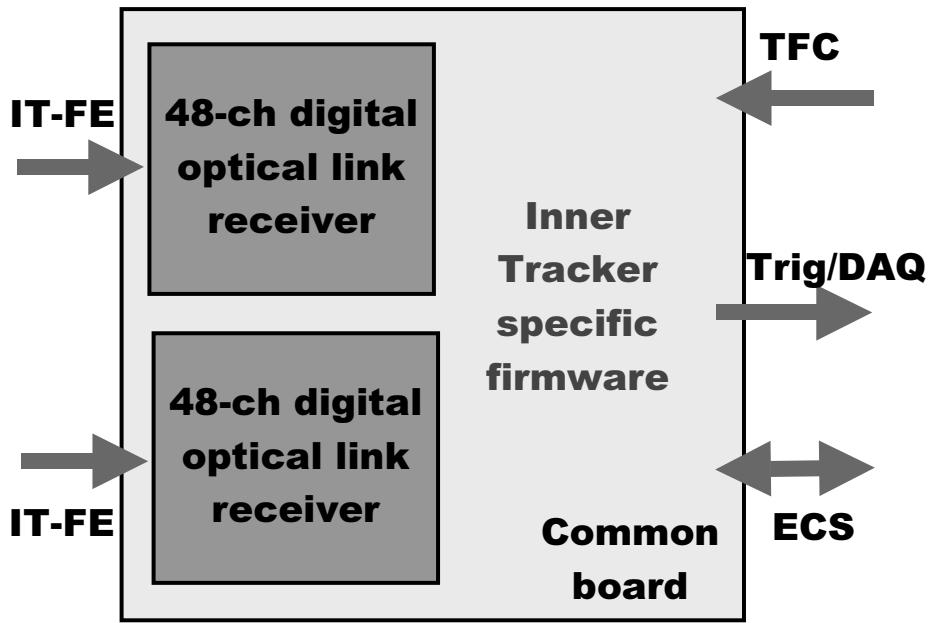


Figure 70 Inner Tracker Level-1 board layout.

Algorithms for data preprocessing for the e Level-1 trigger and for zero suppression for data acquisition will also be similar to the VELO algorithm. They will be defined after further beam test on final silicon sensors.

5.2 VELO Level-1 board as Level-1 Decision Unit

The Level-1 Decision Unit (L1DU, [65]), shown in Figure 71, acts as an interface between the Level-1 trigger CPU farm and the Readout Supervisor of the LHCb TFC system. The main tasks of the L1DU are:

- to interact with the Network Processor, NP of the Level-1 trigger, which collects the decision from individual CPUs in the Level-1 trigger farm, sorts them and sends to the L1DU,
- to convert the decision of the Level-1 trigger system into information, required by the Readout Supervisor (RS),
- to store all information, received from the Level-1 trigger and sent to the Readout Supervisor in the Level-1 buffer until final Level-1 decision, distributed via TFC system,

- to send information from the Level-1 buffer to the DAQ system,
- to collect and keep statistics on decisions from the Level-1 trigger system and provide it upon request to the LHCb ECS system.

In order to implement required functionalities, the L1DU shall be connected in a standard way to LHCb TFC, ECS and DAQ system and contain the Level-1 buffer. It also needs interfaces to the Network Processor and to the Readout Supervisor and digital logic for data conversion and monitoring.

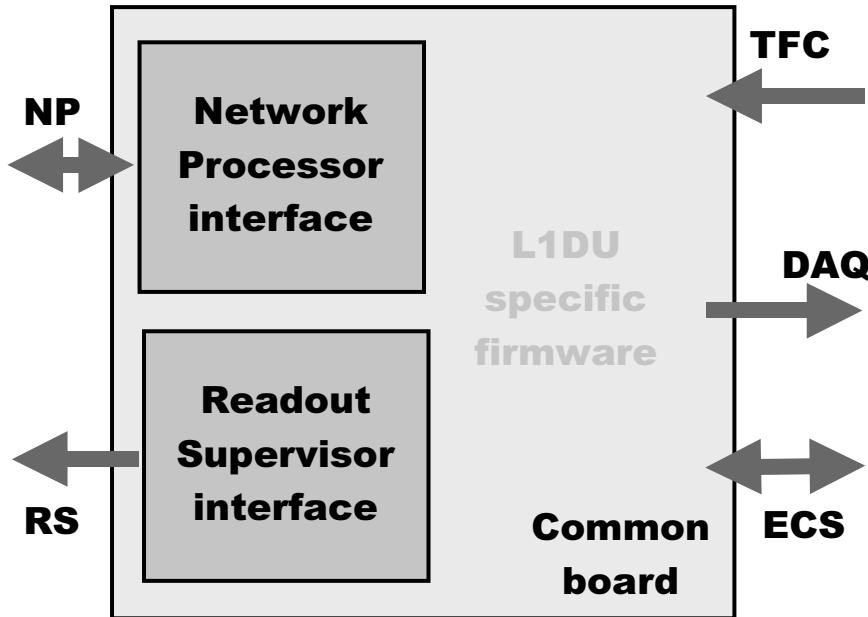


Figure 71 Level-1 Decision Unit layout.

These requirements may be satisfied by using the VELO digital Level-1 board as a main board. The necessary interfaces to the Network Processor and the Readout Supervisor may be implemented as two mezzanine cards in place of mezzanine receiver cards of the detector Level-1 boards. The FPGAs on the main board provide sufficient logic to implement data conversion functions (NP to RS) and to collect and keep statistics on the Level-1 trigger decisions.

5.3 Conclusions

The final implementation of the VELO Level-1 board, based on the previously acquired experience, may result in a common module design which may be used by several LHCb subdetectors and other parts of the LHCb trigger and DAQ systems.

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7 Acronyms

ALU	Arithmetic and Logic Unit
ASIC	Application Specific Integrated Circuit
BC	Bunch Crossing
CAN	Controlled Area Network
CMOC	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DAQ	DAta acQuisition system
DB	Data Base
DPM	Dual Port Memory
DSP	Digital Signal Processor
ECL	Emitter Coupled Logic
ECS	Experiment Control System
EEPROM	Electrically Erasable Programmable Read Only Memory
ENC	Equivalent Noise Charge
FADC	Flash Analog to Digital Converter
FEE	Level-0 Emulator
FEM	Level-0 Multiplexer
FIFO	First-In First-Out
FPGA	Field Programmable Gate Array
GPS	Global Positioning System
HDL	Hardware Description Language (Verilog or VHLD)
I2C	Inter-Integrated circuit Control bus (Philips Semiconductors)
IEEE	Institute of Electrical and Electronics Engineers
JTAG	Joint Test Action Group
L1B	Level-1 Buffer
L1T	Level-1 Trigger
LCMS	Linear Common Mode Suppression

LEP	Large Electron Positron collider
LHC	Large Hadron Collider
LUT	Look-Up Table
LVDS	Low Voltage Differential Signal
MIP	Minimum Ionizing Particle
NP	Network Processor
PC	Personal Computer
PCB	Printed Circuit Board
PCI	Peripheral Component Interface
PDU	Programmable Delay Unit
RMS	Root Mean Square
RS	Readout Supervisor
RU	Readout Unit
SCADA	Supervisory Control And Data Acquisition
SCI	Scalable Coherent Interface
SEU	Single Event Upset
SFC	Sub Farm Controller
SPAC	Serial Protocol for Argon Calorimeter control
SPECS	Serial Protocol for Experiment Control System
SRAM	Static Random Access Memory
TFC	Timing and Fast Control
TTC	Timing and Trigger Control
VELO	VErtex LOcator
VME	Versa Module Eurocard