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DEVELOPMENT OF AN X-BAND LLRF PROTOTYPE FOR THE EUPRAXIA@SPARC_LAB LINAC*

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Abstract

EuPRAXIA stands for "European Plasma Research Accelerator with eXcellence In Applications". It's a next generation free-electron laser (FEL) aimed at developing a compact, cost-effective particle accelerator based on novel wake-field accelerator technology. Traditionally, high-energy physics requires higher acceleration voltages, so developing the X-band acceleration technology, enables the possibility to achieve high gradients with very compact structures. The EuPRAXIA LINAC injector comprises one S-Band and two X-Band sections, achieving a max beam energy of 1 GeV. Low-Level Radio Frequency (LLRF) systems are crucial for RF station synchronization and machine stability at femtosecond precision. Currently, there are no commercially available X-band LLRF solutions, especially for pulse processing and control in the 100 ns range. This project aims to develop an X-band LLRF prototype, in collaboration with INFN, tailored to meet EuPRAXIA@SPARC_LAB LINAC's demands. Once confirmed on a real testbench, the prototype will be used as a starting point for the industrialization into a commercial instrument. This paper presents the architecture and preliminary results of the prototype.

INTRODUCTION

In recent years, the field of particle accelerators has witnessed significant advancements, driven by the need for compact, cost-effective, and high-performance systems. Among these innovations, the EuPRAXIA (European Plasma Research Accelerator with eXcellence In Applications) project stands out as a pivotal initiative aiming to develop the world's first compact accelerator based on plasma technology [1]. Within this framework, the SPARC_LAB LINAC (Sorgente Pulsata e Amplificata di Radiazione Coerente_Laboratori Nazionali di Frascati Linear Accelerator) plays a crucial role.

The EuPRAXIA SPARC_LAB LINAC, housed at the INFN-LNF (Istituto Nazionale di Fisica Nucleare - Laboratori Nazionali di Frascati) in Italy, is designed to serve as a testbed for advanced acceleration techniques and beam manipulation. Figure 1 shows the machine layout of the SPARC_LAB LINAC combining the conventional radio-frequency (RF) linear acceleration that includes 1 S-band RF gun, 4 S-band and 16 X-band RF structures with state-of-the-art plasma acceleration, aiming to achieve unprecedented beam quality and energy efficiency.

The integration of these technologies is expected to address some of the fundamental limitations of traditional accelerators, such as size, cost, and energy consumption.

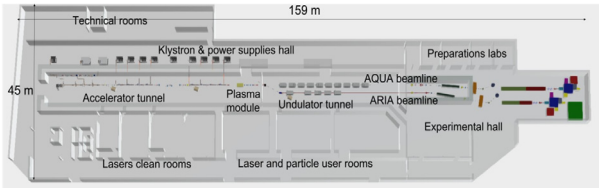

Figure 1: EuPRAXIA@SPARC_LAB machine layout [2].

A key component of this innovative system is the development of the X-Band Low-Level Radio Frequency (LLRF) system. The X-Band LLRF system is crucial for precise control of the accelerating fields, ensuring stability and high performance of the electron beam. Operating at higher frequencies than traditional S-Band systems, the X-Band technology offers significant advantages in terms of reduced accelerator size and enhanced accelerating voltage gradients in the order of 60 MV/m. This development is instrumental in achieving the compact and efficient design goals set by the EuPRAXIA project.

This paper provides a comprehensive overview of the EuPRAXIA X-band LLRF prototype requirements, detailing the architecture of the prototype, the realization of the prototype which includes the development and assembly. The results from initial experimental runs, highlighting the prototype's front-end performance in terms of amplitude and phase stability are presented.

Requirements

The below Table 1 describes the EuPRAXIA X-band LLRF prototype requirements that provides the input and the starting point towards the development of the prototype. The main requirements are the prototype operates in pulsed mode at a carrier frequency of 11.994 GHz, with a master oscillator input level of 0 dBm. It utilizes pulse length of 100 ns and a greater than equal to 250 MHz sampling rate for precise control and signal processing. The front-end should handle the input levels up to +20 dBm and require a bandwidth greater than 20 MHz to process the 100 ns pulses. The back-end should provide output level at +10 dBm with a rise time of 10-12 ns, maintaining signal integrity. The system should have a low added amplitude noise (0.01-0.05% RMS) and phase noise (0.01-0.015 degrees RMS) over 400 pulses, ensuring high signal fidelity. With two RF input channels and one RF output channel, an

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open-loop operation is sufficient for the evaluation of the prototype.

Table 1: EuPRAXIA LLRF Prototype Requirements

Parameter	Desired Value
Mode of operation	Pulsed
Carrier Frequency	11.994 GHz
MO input level	0 dBm
Pulse length	100 ns
Sampling rate	>=250 MSps
Front-end max. input level	+20 dBm
Front-end BW	> 20 MHz
Back-end output level	> +10 dBm
Back-end rise time	10 – 12 ns
Minimum pulse-to-pulse detectable amplitude (Front-end), (400 pulses)	0.01 – 0.05 % RMS
Minimum pulse-to-pulse detectable phase (Front-end), (400 pulses)	0.01 – 0.015 deg RMS
Back-end pulse-to-pulse added amplitude noise (400 pulses)	0.01 – 0.05 % RMS
Back-end pulse-to-pulse added phase noise (400 pulses)	0.01 – 0.015 deg RMS
No. of RF input channels	2
No. of RF output channels	1
Amplitude and Phase pulse to pulse feedback	Open Loop only

PROTOTYPE ARCHITETURE

The proposed approach to build the prototype is a single stage down-conversion and a double stage up-conversion with open loop which means the prototype has a separate front-end and back-end systems. Figure 2 illustrates the conceptual block diagram of the prototype which also includes the generation of LO and ADC signals distributing them to the LLRF subsystems. A 11.994 GHz master oscillator signal serves as the reference frequency for the system which is used to generate a 250 MHz reference signal for the ADC, generate a LO-S band signal for the IQ modulator, a LO-9 GHz signal for the back-end and a LO-X band signal used in the front-end for the down-conversion to IF frequency.

The main block diagram shows the primary signal flow within the LLRF subsystems, from the RF inputs to the final modulated output. The system receives two RF input signals where each RF input is processed by an RF front-end channel that included necessary amplification, filtering and down-conversion to an intermediate frequency using the LO-X signal. The IF signals are digitized using the KADC-8 module, operating at 250 MHz. Then the digital signals from the ADC are acquired by the FPGA, and the data is processed offline.

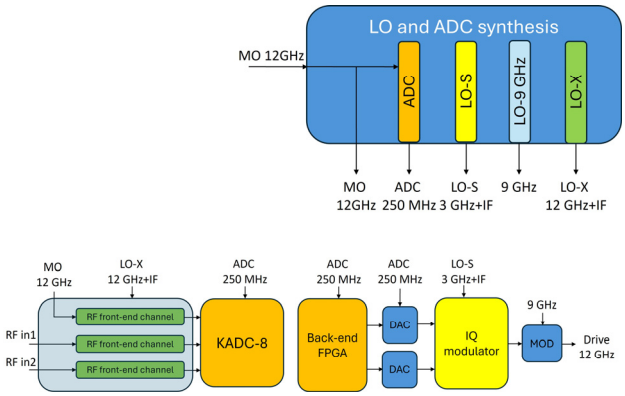

Figure 2: Conceptual block diagram of the prototype.

Since, the prototype operates in open loop with no feedback, the DAC's on the back-end are used to generate sequence of pulses of repeatable amplitude and phase. Then the analog signals are modulated using an IQ modulator with the LO-S signal combining in-phase and quadrature components. Finally, the modulated signal is upconverted to the drive frequency of 11.994 GHz for transmission.

PROTOTYPE SETUP AND MEAUREMENTS

The development and set-up of prototype is divided into two phases as shown in Fig. 3. The first phase is the design and evaluation of the front-end which includes the RF front-end channels and a KADC-8 module containing ADC and FPGA. The front-end performance is evaluated by offline processing of raw ADC data and measuring the standard deviation of the 400 acquired pulses with pulse length of 100ns each.

The second phase is the development and evaluation of the back-end that includes the FPGA development, DAC signal processing and IQ modulation. Also, the second phase includes the integration of the back-end within the X-band up-conversion to generate the 11.994 GHz drive signal and finally evaluating the performance again by offline processing of raw ADC data and measuring the standard deviation of the 400 acquired pulses with pulse length of 100ns each. Later the front-end is used to evaluate the back-end performance and therefore a loopback connection is applied.

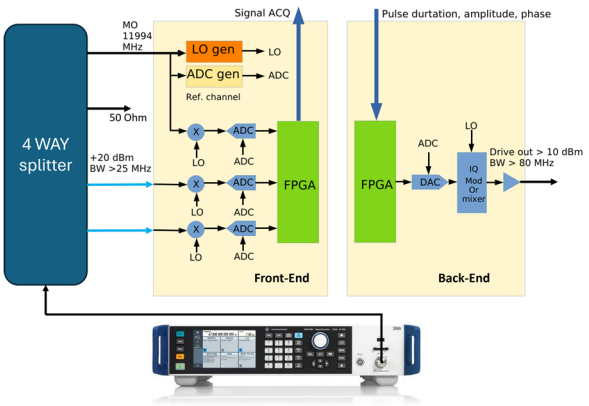

Figure 3: Prototype setup.

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In this paper the prototype setup and measurements on the front-end are tested and reported. The 11.994 GHz master oscillator signal is 4-way splitted where one signal is sent to the front-end to generate the LO, ADC signals and two signals are fed to the front-end RF channels directly for down-conversion to achieve the intermediate frequencies (IF) while the other signal remains terminated with a 50 Ohm load. The IF signals are then sent into KADC-8 module ADCs for digitizing and through the FPGA the raw ADC data over 400 pulses each of 100ns pulse length is acquired for further processing. The processing of the data includes the demodulation of the signal and calculating the standard deviation to achieve the pulse-by-pulse RMS amplitude noise and phase jitter which are presented in the results section.

Below Fig. 4 illustrates the Front-end LO and ADC signal generation components assembled on a 19" 3U aluminium chassis with a regulated voltage supply.

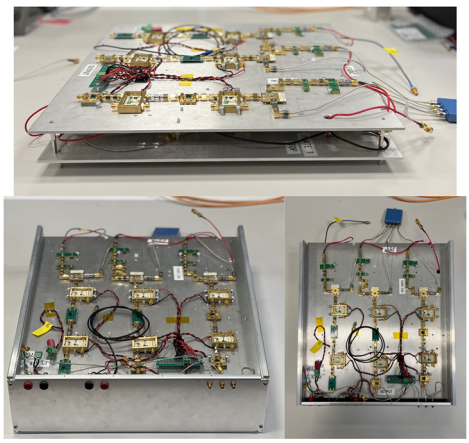

Figure 4: Prototype front-end on chassis.

RESULTS

In this section the front-end results are presented following the above-mentioned measurement setup. Figure 5 illustrates the front-end pulse by pulse amplitude noise measured on the two input channels over 400 pulses with each pulse having a pulse length of 100 ns and both the channels have the rms value of 0.018% which is well within the EuPRAXIA LLRF requirements.

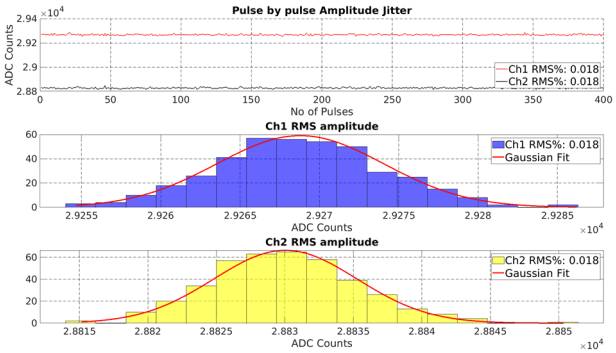

Figure 5: Pulse by Pulse Amplitude noise (Front-end)

Similarly Fig. 6 depicts the front-end pulse by pulse phase jitter measured on the two input channels over 400 pulses with each pulse having a pulse length of 100 ns and between the channels the rms value is 0.009 degrees satisfying the EuPRAXIA LLRF requirements.

Figure 6: Pulse by Pulse Phase Jitter (Front-end)

The histogram plots on the measurements are also plotted and a gaussian curve is fitted for quantitatively describing the data, understanding it's distribution and assessing the data quality.

CONCLUSION

This paper has presented the development and initial testing of an X-band LLRF prototype for the EuPRAXIA@SPARC_LAB LINAC, demonstrating its ability to meet the stringent requirements of the EuPRAXIA project. The prototype architecture, featuring a single-stage down-conversion and double-stage up-conversion system, achieved a front-end RMS amplitude noise of 0.018% and a phase jitter of 0.009 degrees over 400 pulses, well within specifications. Data quality was validated through histogram analysis and gaussian fitting. These promising results indicate the prototype's potential for future industrialization and commercial deployment, marking a significant advancement towards compact particle accelerator technologies. The next step is the development of phase-2 by assembling the back-end components and evaluating its performance in terms of pulse-by-pulse amplitude noise and phase jitter of the drive signal.

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