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ORIGINAL RESEARCH

Optimising energy consumption in Nano-cryptography: Quantum cellular automata-based multiplexer/demultiplexer design

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Abstract

Future global communications will depend heavily on nano-communication networks, which use ultra-low power nano-circuits to transmit data efficiently at very high rates. An essential part of distributed communication networks is the circuit-switched network, which distributes the input signal among several users. For designing nanoscale digital circuits, Quantum Cellular Automata technology (QCA) emerges as a formidable contender against the established complementary metal-oxide-semiconductor (CMOS) technology for low-power devices. The authors endeavour to achieve an efficient design for multiplexer and demultiplexer switching circuits. The designed multiplexer and demultiplexer have 15 cells with an area of 0.02 μm^2 and a latency of 0.5 clock cycles. The authors assess the energy dissipation and temperature impacts for both multiplexer and demultiplexer circuits. The novel design of switch circuits facilitates the sharing of a single communication link across multiple devices at the nano-scale.

KEYWORDS

quantum computing techniques, quantum dots

1 | INTRODUCTION

In the electronic industry, logic circuit development has made extensive use of CMOS technology during the past few decades. Today, it faces lot of limitations, such as high leakage current, high device complexity and high-power consumption, as moving to the nano-scale applications. Therefore, a scalable low power device is needed. Researchers have worked very hard to offer alternative nanotechnologies to address these problems [1, 2]. Several technologies were offered in this respect, including Quantum-dot Cellular Automata, Carbon Nanotube Field Effect Transistor, and Single Electron Transistor. Due to certain distinct features, namely high switching frequency (Tera Hertz), high scalability, and low power consumption. The greatest alternatives to CMOS technology are thought to be QCA technologies [3]. QCA uses electron positions inside a cell to represent binary data. Transistors are the main component used in CMOS technology for logic operations. Compared to CMOS, the QCA circuits have much lower heat dissipation and are far more power efficient. Furthermore, columbic repulsion is used in QCA to transport data, whereas current switching is used in CMOS technology. In QCA, the primary block is the cells with two free electrons in a square-shaped structure. The electrons can occupy the diagonal position of quantum dots among the four quantum dots inside the cell. It is a transistor-less technique in which the information is transmitted by these two electron positions rather than voltage or current levels [4].

QCA-enabled nano-communication networks are expected to revolutionise future global communications. The benefits of nano-communication over traditional communication networks include its integration with cutting-edge technology, which improves the functionality and security of smart products and systems. It can process large amounts of data quickly and effectively. Because of the incredibly low power consumption, which also increases device lifespan and reduces operating expenditures, the network is more energy-efficient.

Additionally, it provides scalability to accommodate more devices. The highly compact nano-communication devices can be integrated for a variety of uses, including industrial, environmental, and medical [5–7].

Furthermore, nano-communication networks can significantly enhance the functionality and efficiency of distributed communication networks. An essential part of distributed communication networks is the circuit-switched network, which ensures reliable and consistent performance by establishing dedicated communication paths. Multiplexing and demultiplexing are crucial techniques in circuit-switched networks for efficient signal management. A multiplexer selects data from one of the many input data lines and transmits it through a channel. At the receiving end, a demultiplexer routes the transmitted data to the appropriate output data line. Therefore, energy-efficient QCA-based circuit-switched networks are of primary concern. The different arrangements of QCA cells enable the realisation of a wide range of QCA multiplexer (MUX) and demultiplexer (DEMUX) designs among researchers [8–10].

In this article, an innovative design of MUX and DEMUX circuits is proposed by taking care of various performance constraints such as QCA cell count, area of layout, latency in clock cycles, and total energy dissipation in milli electron volt. The suggested circuit-switched network is implemented and QCADesigner-2.0.3 is used for verification. The main input of the paper is stated as follows:

- Implementation of a QCA-based Single-Layer 2:1 Multiplexer.
- Implementation of a QCA-based single layer 1:2 Demultiplexer.
- Comparative analysis of proposed circuits against existing works.
- Estimation of energy dissipation and analysis of temperature effects on the proposed switched network.

The paper is detailed as follows: Primitive details of QCA technology are presented in Section 2. Section 3 deals with the existing works related to the proposed circuits. In Section 4, the paper details the design of the proposed MUX and DEMUX structures. In Section 5, simulation outputs are displayed and various parameter performances are compared. Section 6 completes the paper.

2 | BASICS OF QCA

The QCA cell is the key element in quantum cellular automata circuits such as the transistor in CMOS circuit design. The columbic force of interaction pays the way for the data exchange between QCA cells. QCA wire is used for interconnection purposes. Two cell configurations 90° and 45° cells are there. The crossover can be possible in two ways, coplanar or multilayer. Due to the fabrication challenges, coplanar and single-layer designs are preferred. Figure 1a illustrates a primitive QCA cell and Figure 1b shows the two QCA Cell polarisations (P), representing logic 0 and logic 1, respectively.

The clocking schemes in QCA are utilised for data synchronisation. It acts as the power supply and controls the data flow. In the four-phase clocking technique, the clock signal comprises four phases namely Switch, Hold, Release, and Relax. Initially, termed 'Switch', QCA cells start depolarising with low electron tunnelling potential barriers. Throughout this phase, barriers between the dots are gradually increasing, causing cells to polarise by their drivers' states. The actual computation occurs precisely during this phase. Inter-dot barriers reach a height sufficient to prevent electron tunnelling, thus setting the states of cells at the end of the Switch phase. In the Hold phase, QCA cells maintain fixed states as barriers remain high, and act as inputs for the subsequent stage. During the Release phase, low barriers enable cells to relax to a depolarised state. Finally, the Relax phase keeps barriers low, maintaining cells in a ground state [11, 12]. Figure 2 illustrates the QCA four-stage clocking scheme [13].

The fundamental gates employed in QCA circuit design include majority gates and inverter gates as illustrated in Figure 3a and 4a respectively. The two types of majority gates: ordinary majority gates and rotated majority gates are represented in Figure 3b,c respectively for a three-input majority gates. By configuring a three-input Majority gate, a two-input logic AND gate and OR gate can be attained. For the AND gate, one input is permanently set to '0' in the Majority gate, while for the OR gate, one input is permanently set to '1'. The output function of three-input majority gates is represented by Equation (1) [14].

$$Y = AB + BC + AC \tag{1}$$

The QCA inverter is depicted in Figure 4b.

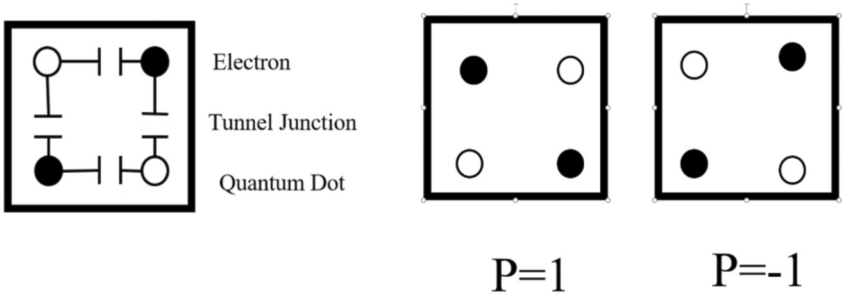

FIGURE 1 (a) Primitive QCA cell and (b) two cell polarisation states.

3 | EXISTING MUX AND DEMUX CIRCUITS

The design and simulation of digital logic circuits, including basic gates [15, 16], adders [17, 18], RAM [19, 20], ALUs [21, 22], and digital filters [23] are still the subject of substantial research in QCA technology. Furthermore, because quantum operations are inherently reversible, recent advancements in quantum computing have greatly aided the study of reversible circuits [24, 25]. Numerous studies on effective QCA multiplexer and demultiplexer designs have been reported thus far, and they will be included in this section.

The multiplexer is an exceptionally versatile circuit with the capability to select one input line from multiple input lines and direct it to a shared output line. Typically, it is represented as 2^n:1, indicating that there are n select lines to take one of the 2^n input combinations to be routed to the output. The basic MUX configuration is 2:1 MUX. Given the crucial role of the MUX circuit in digital circuit design, researchers have endeavoured various designs to enhance its performance.

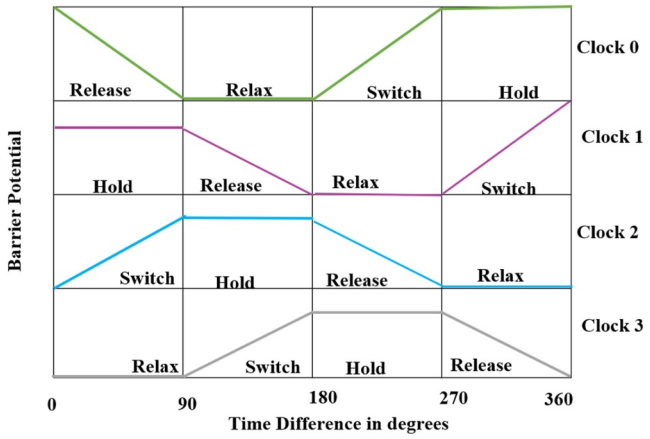

FIGURE 2 Four-phase clocking Mechanism.

Kim et al. introduced a MUX circuit in a coplanar crossover with 46 cells with a delay of 1 clock cycle [26]. Another MUX design was proposed by Mardiris and others to increase the circuit stability. It consists of 56 cells but the area is reduced from the design by Kim [27]. In ref. [28], the mux design buildup of 27 cells covering an area of 0.03 μm^2 is used to form different gates. Sen et al. introduced an innovative design of a 2:1 multiplexer considering the primitive block as the majority gates. The resulting design is made up of 19 cells occupying an area of 0.02 μm^2 [29]. Singh et al. recommended a 2:1 MUX circuit using 4 Dot 2 Electron QCA architecture [30]. The performance of 2:1 multiplexer and 1:2 demultiplexer QCA layouts was discussed in the study by Khan [31]. The mux design has 17 cells with a large area compared to the other designs. In ref. [32] three input XOR gate-based 2:1 MUX is designed. The cost of the XOR gate is minimised using Shannon's expansion theorem. Khan [33] calculated the energy dissipation and cost in the case of a 2:1 MUX design with 17 cells and an area of 0.01 μm^2. In ref. [34], Mosleh added a new 2:1 QCA multiplexer that makes use of the MV32 (three inputs and two outputs) gate. The suggested 2:1 multiplexer's multilayer implementation is shown with 21 cells and 0.75 clock cycle latency. Subsequently, 4:1 and 8:1 QCA multiplexers are built using the suggested architecture. Kassa [17] introduced another 2:1 multiplexer design consuming 23 cells, 0.04 μm^2 area, and 0.5 clock cycle latency. Ahmadpour et al. [20] present a 2:1 QCA mux with 10 cells occupying an area of 0.03 μm^2.

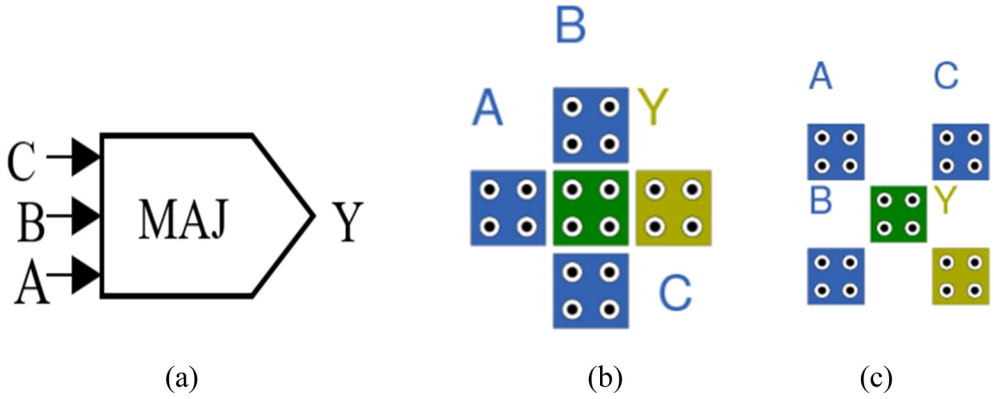

FIGURE 3 (a) Symbol of 3-input majority Gate, (b) OMG, (c) RMG. OMG, ordinary majority gates; RMG, rotated majority gates.

FIGURE 4 (a) Symbol of majority gate, (b) QCA based inverter.

Similarly, there are various designs for 1:2 DEMUX from the research community. Shah et al. introduced a 1:2 DEMUX with 56 cells and an area of 58,320 nm^2 using coplanar crossover [35]. A novel single-layer DEMUX circuit was introduced by Das with 32 cells [7]. The receiver portion in nano communication comprises one crossbar switch and the proposed demultiplexer. Iqbal explored a DEMUX with 27 cells and attained complexity reduction with other previous designs [36]. Ahamad [37] suggested a novel design for three input AND and OR gates to reduce total area, delay, and complexity challenges. The proposed DEMUX is a buildup of the three-input AND & OR gates. Khan [38] introduced an area-efficient demultiplexer that has a cell count of 21 QCA cells with an area of 20,412 nm^2 constituting an area usage of 33.33%. In ref. [39] an optimal, single-layered, 1:2 demultiplexer circuit is proposed using 19 QCA cells with a latency of a single clock cycle. The authors in ref. [40] proposed 1-to-2 DEMUX uses a rotated majority gate for its implementation. It contains 16 QCA cells with a total area of 0.02 μm^2 and 0.25 clock cycles as latency. For the first time, a demultiplexer is utilised to design a tree router.

Despite the implementation of various QCA-based MUX and DEMUX designs, there exist challenges in complexity, power, and area constraints. Accordingly, this paper presents energy-efficient multiplexer and demultiplexer designs.

4 | PROPOSED SWITCH CIRCUIT DESIGN AND SIMULATION RESULTS

In this section, a novel 2:1 QCA MUX circuit and 1:2 DEMUX circuits are developed.

4.1 | QCA-based MUX circuit

The block diagram and layout of the proposed 2-to-1 MUX circuit are depicted in Figure 5 a and (b) respectively. Table 1 indicates the truth table. The proposed 2-to-1 QCA MUX circuit employs a majority gate as the foundational building block, comprising one OR gate, two AND gates, and an inverter gate. By adjusting the input conditions of the majority gates, the AND and OR gates are configured. The circuit operates as: when $S = 0$, OUT = IN1, and when $S = 1$, OUT = IN2. This circuit occupies an area of 0.02 μm^2 with a cell count of 15 cells and a latency of 0.5 clock cycle. The output of the MUX is represented by Equation (2).

$$OUT = S'IN1 + SIN2 \quad (2)$$

4.2 | QCA-based DEMUX circuit

Demultiplexer circuits are frequently utilised in communication systems. These circuits are designed to choose one input data signal and distribute it across multiple output lines, effectively acting as data distributors. The truth table is given in Table 2. In QCA circuits, demultiplexers are typically constructed using inverters and majority gates. The block diagram and QCA layout of the proposed 1-to-2 DEMUX circuit are depicted in Figure 6a,b respectively. It consists of two AND gates composed of majority gates and one inverter. The design cell count is 15 QCA cells, occupying an area of 0.02 μm^2 with a latency of 0.5 clock cycles. The operation is defined as follows:

When Select line (S) = 0 and input (D) = 0, the output combination (Y2Y1) is 00.
When Select line (S) = 0 and input (D) = 1, the output combination (Y2Y1) is 01.
When Select line (S) = 1 and input (D) = 0, the output combination (Y2Y1) is 00.
When Select line (S) = 1 and input (D) = 1, the output combination (Y2Y1) is 10.

TABLE 1 Truth table for a 2:1 MUX.

Input	Select line (S)	Out
IN1	0	IN1
IN2	1	IN2

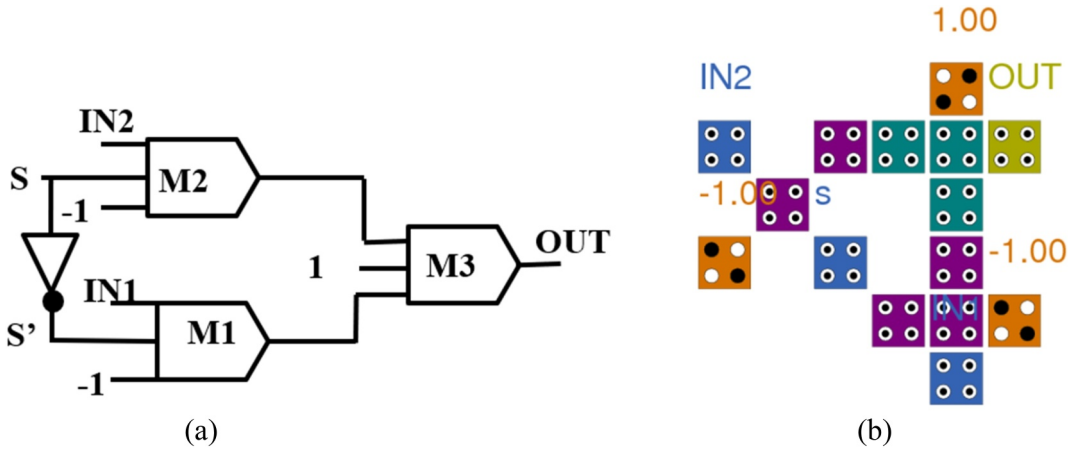

FIGURE 5 (a) Block diagram of Mux, (b) QCA layout of 2:1 MUX.

The circuits operate based on the logical expressions provided in Equations (3) and (4).

$$Y1 = S'D \tag{3}$$

$$Y2 = SD \tag{4}$$

Among the two AND gates, one uses normal majority gates, and the other uses rotating majority gates. The D input is common input to both majority gates. The selector line (S) serves as one of the inputs to the rotated majority gate, while its inverse (S′) is one of the inputs to the ordinary majority gate. The inversion of the selector line is performed by the inverter gate. The fixed polarisation, $p = -1$ is applied to one of the inputs of both majority gates to function as AND gates. The output Y1 is dependent on D if $S = 0$, while Y2 depends on D if $S = 1$.

5 | SIMULATION RESULT AND COMPARISON

The suggested 2:1 MUX and 1:2 DEMUX are simulated using the QCADesigner tool [41]. Figures 7 and 8 show the corresponding simulation waveforms. The functionality of both circuits is verified. Table 3 compares the existing MUX design with the proposed one. Similarly, Table 4 compares the existing DEMUX designs with the proposed one. Area, complexity, latency, and cost are taken for assessment parameters. The analysis demonstrates that the suggested MUX/DEMUX designs exhibit superior performance across assessment parameters compared to existing designs. So, the proposed designs are used for high-bit circuits such as $1{:}2^n$ and $2^n{:}1$ design.

TABLE 2 Truth table of 1:2 DEMUX.

		Outputs	
Select line (S)	**Input (D)**	**Y2**	**Y1**
0	0	0	0
0	1	0	1
1	0	0	0
1	1	1	0

5.1 | Energy estimation and average out polarisation

Another parameter for the assessment is the energy dissipation. QCA pro and QCADesigner-E tools are available, but QCAPro has limitations to support the latest version. So, for energy calculation, QCADesigner-E tools are utilised. The energy is regarded as a bath in the QCA Designer-E tool. The various type of energy transfer that occurs includes the energy that is transmitted between cells (E_{Io}), the energy that the cell receives from the clock (E_{Clk}), and the energy that is transferred to the environment (E_{Env}). While calculating the energy loss, a minimal error can occur and is estimated below in Equation (5).

$$E_{\text{Error}} = E_{Env} - (E_{Clk} + E_{Io}) \tag{5}$$

The error value can be either positive or negative. Table 5 provides the energy dissipation of MUX/DEMUX circuits at 1K. Table 6 reports the total energy dissipation and average energy dissipation, including their respective errors for the proposed MUX/DEMUX design, and compares it with existing works. Additionally, the Average Out Polarisation (AOP) is computed to observe the temperature effects [42], as

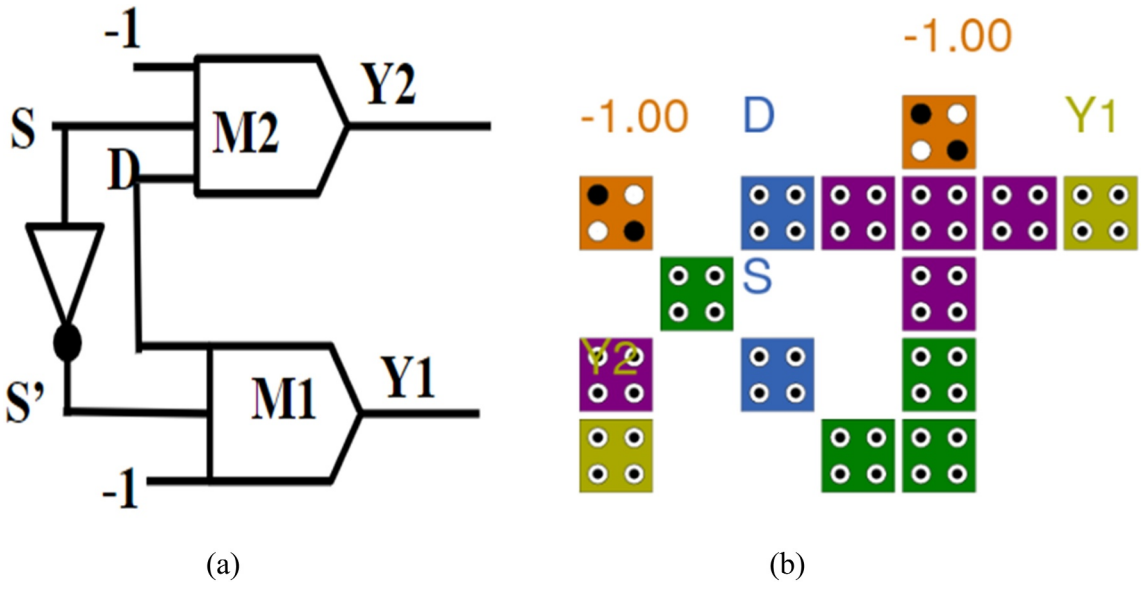

FIGURE 6 (a) Block diagram of 1:2 DEMUX, (b) QCA layout of proposed DEMUX.

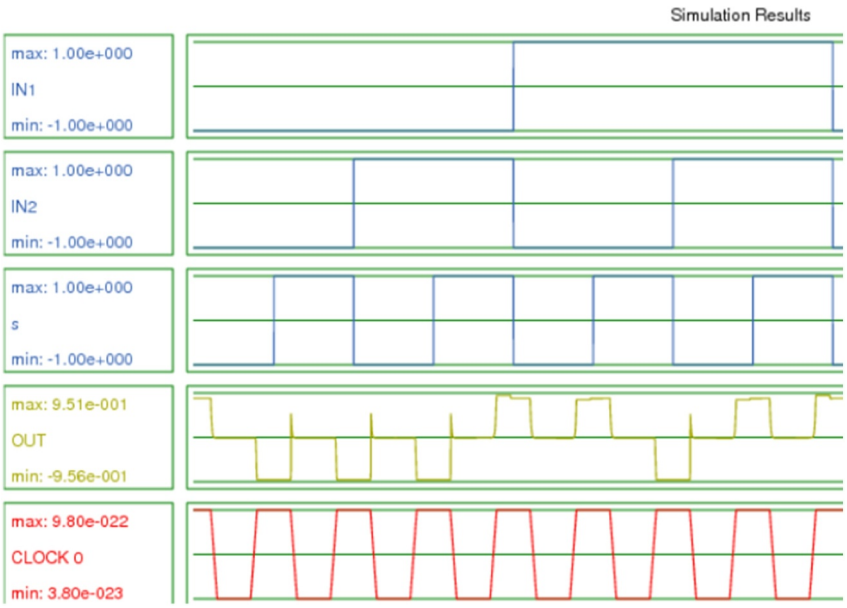

FIGURE 7 Simulation output of proposed MUX.

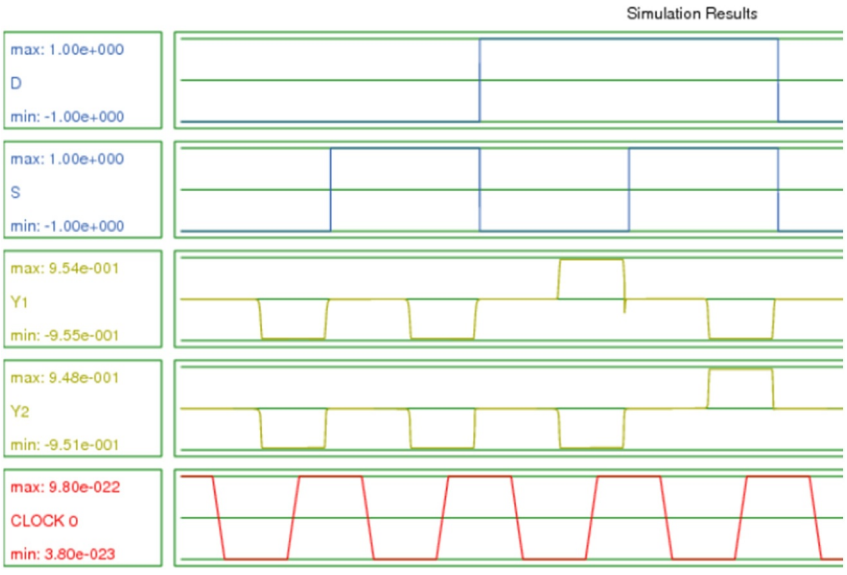

FIGURE 8 Simulation output of proposed DEMUX.

TABLE 3 Comparison of performance parameters of various MUX design.

Design	Cell	Area (um^2)	Latency (clock cycles)	Cost
[26]	46	0.08	1	3.68
[27]	56	0.07	1	3.92
[28]	27	0.03	0.75	0.607
[29]	19	0.02	0.75	0.285
[30]	19	0.02	0.5	0.19
[31]	17	0.05	0.75	0.637
[32]	21	0.015	0.75	0.236
[33]	17	0.01	0.5	0.085
Proposed MUX	15	0.02	0.5	0.15

TABLE 4 Comparison of performance parameters of various DEMUX design.

Ref	Cell	Area (um^2)	Latency (clock cycles)	Cost
[35]	56	0.08	1	3.24
[7]	32	0.026	0.75	0.62
[36]	27	0.04	0.5	0.54
[37]	21	0.03	0.75	0.47
[38]	21	0.03	0.5	0.31
[39]	19	0.014	0.25	0.06
[40]	16	0.02	0.25	0.08
Proposed DEMUX	15	0.02	0.5	0.15

TABLE 5 Energy estimation of proposed MUX and DEMUX designs using QCA designer-E tool.

Design	Temperature	Total Ebath (meV)	Error total Ebath (meV)	Average Ebath (meV)	Error average Ebath (meV)
Proposed MUX	1K	1.0	−1.35	1.0	−0.12
	5K	6.77	−0.872	0.615	−0.0792
Proposed DEMUX	1K	8.31	−0.851	0.755	−0.07
	5K	8.02	−0.82	0.729	−0.074

TABLE 6 Relative analysis of energy dissipation at 1K: Proposed design versus best existing work.

Design	Total Ebath (meV)	Error total Ebath (meV)	Average Ebath (meV)	Error average Ebath (meV)
[33]	14.30	−1.41	1.30	−0.128
Proposed MUX	1.0	−1.35	1.0	−0.12
[39]	11.3	−1.4	1.03	−0.10
Proposed DEMUX	8.31	−0.851	0.755	−0.07

TABLE 7 AOP measurement of proposed MUX and DEMUX designs.

		Temperature (K)				
Design	**Output**	**1**	**2**	**3**	**4**	**5**
Proposed MUX	OUT	9.19	9.17	9.01	4.90	4.37
Proposed DEMUX	Y1	9.53	9.53	9.49	9.33	9.03
	Y2	9.47	9.47	9.40	9.16	8.62

Abbreviations: AOP, average out polarization.

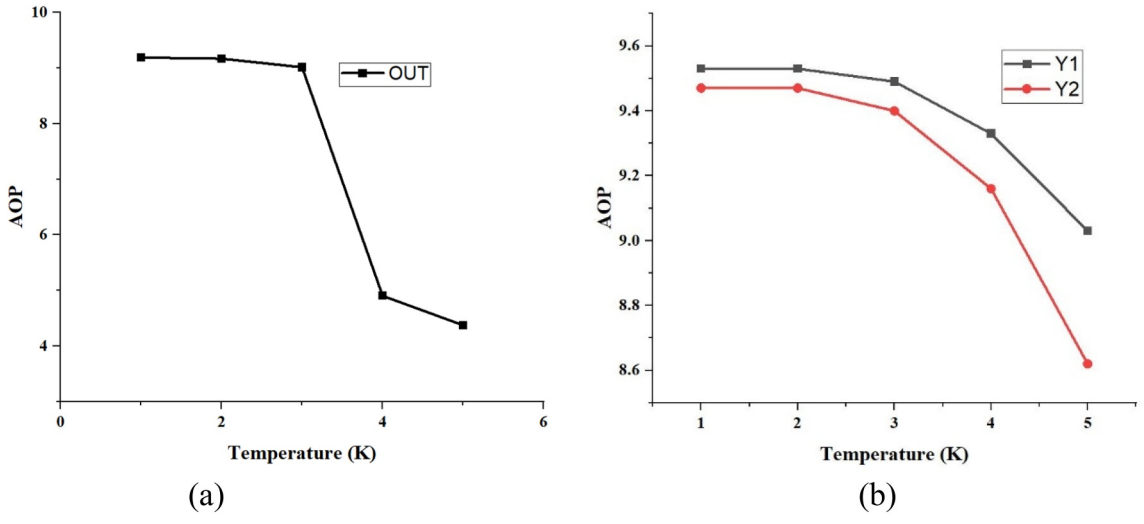

FIGURE 9 AOP versus temperature (1) MUX, (b) DEMUX. AOP, average out polarisation.

shown in Table 7. As the temperature value increases, the AOP decreases. AOP is calculated using the Equation (6).

$$\text{AOP} = \frac{\text{Maximum Polarization} - \text{Minimum Polarization}}{2} \quad (6)$$

A graphical illustration of the AOP is provided in Figure 9. It is observed that the recommended designs produce accurate results up to temperature 3K. After that, the circuit may malfunction.

6 | CONCLUSION

Among the nano-scale technologies, QCA is prominent in replacing CMOS due to high speed, low energy dissipation, and area efficiency. This paper aims to enhance existing switch network MUX/DEMUX circuits for low-power applications by leveraging three input majority gates and inverter gates in the architectural design. Novel MUX and DEMUX designs are introduced and their functionality is validated using QCADesigner tool version 2.0.3. The simulation results of the proposed MUX and DEMUX feature a simple layout comprising 15 cells, occupy 0.02 μm^2 area, and exhibit a latency of 0.5 clock cycles. Furthermore, the 2:1 multiplexer and 1:2 demultiplexer have 93% and 26.46% reduction in total energy dissipation using the QCADesigner-E tool compared with prior works. The efficient design of multiplexer and demultiplexer improve bandwidth utilisation, reduce latency, lower power consumption, enhance reliability, offer scalability, and improve overall network management. Such advancements are essential for the successful deployment and operation of nano-communication systems in various high-tech and crucial applications. So cryptographic methods for QCA-based secure nano-communication systems may be implemented in the future using the proposed switch network.

AUTHOR CONTRIBUTIONS

Aswathy N: Conceptualization; methodology; writing—original draft. **N. M. Siva Mangai**: Supervision; validation; writing—review and editing.

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CONFLICT OF INTEREST STATEMENT

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

DATA AVAILABILITY STATEMENT

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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