TN-67-34
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THE LOGIC OF THE HUMMINGBIRD I AND IX

General

This section describes the logic of the HBI, which consists of 2 MC/sec R-series Flip-Chip modules. Most of the HBII logic is similar. See for the major differences section:

Output/Input Cycle

The logic is shown on Fig. 8 and the timing on Fig. 9. The Selection (SEL) and Write Gate (WG) signals from the Device selector are nand gated. If both signals are present a 4 μs One-Shot (OS1) is set. The output of this OS is used to: (1) Strobe the outputs of the Binary to octal decoder. (2) To produce a Data Demand Signal (DD) to tell the computer than an output word has been received.

The inputs of the Decoder consist of the normal and inverted output bits 2, 3 and 4 (2nd, 3rd and 4th bit of an output word). Seven of the eight outputs of the Decoder are used.

On Fig. 10 we see the codes and their significance. An output cycle will be terminated by a Word Count equals zero (WC = 0) signal from the computer, which in return will send an End of Record (EOR) back to the computer.

CODE

bit 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
0	0	0	0													not used
0	0	0	1			YS9	YS8	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	Y-START (YS)
0	0	1	0			YF9	YF8	YF7	YF6	YF5	YF4	YF3	YF2	YF1	YF0	Y-FINAL (YF)
0	0	1	1	XS5	XS4	XS3	XS2	XS1	XS0							X-START (XS)
0	1	0	0	XF5	XF4	XF3	XF2	XF1	XF0							X-FINAL (XF)
0	1	0	1	R/F	MF10	MF9	MF8	MF7	MF6	MF5	MF4	MF3	MF2	MF1	MF0	MOVE FILM (MF)
0	1	1	0	TH3	TH2	TH1	TH0			D1	D0				ORTH	MISC. (MI)
0	1	1	1													CLEAR (CLR)

Fig. 10

The block diagram of all the HBI registers and their relationship is shown on Fig. 11.

code 1 (YS) strobes the 10 least significant bits of the output word into the Y register and counter

code 2 (YF) strobes the 10 least significant bits of the output word into the YF register

code 3 (XS) strobes bits 5 - 10 of the output word into the XS register

code 4 (XF) strobes bits 5 - 10 of the output word into the XF register

code 5 (MF) strobes the 12 least significant bits of the output word into the MF register

code 6 (MI) strobes bits 5 - 8 of the output word into the threshold register, bit 11 and bit 12 into the density FF (D), bit 16 into the normal/orthogonal FF (ORTH).

Codes 1, 2, 3, 4 are passive codes. Their only effect during the output cycle is the setting of a register. Codes 5, 6 and 7 are active codes. Some action takes place immediately during the output cycle. Code 5 (MF): the most significant bit of the 12 bit register determines the direction in which the film advance stepping motor turns; if this bit is "zero" the direction is forward, if "one" the direction is reverse.

The remaining 11 bits are used to indicate the number of steps the stepping motor has to do. Thus the maximum number of steps in either direction may be 2047. A 4 ms clock is enabled as soon as the register $\neq$ zero. The output of the clock is fed to the stepping motor circuitry but also to the register, which is connected as a down counter. If the register = zero, the 4 ms clock is disabled and an interrupt is sent to the computer to indicate that the Move Film is ready. Code 6 (MI): the output of the threshold register is connected to a Digital-to-Analog converter, which output is used as a threshold for the Track Center Circuit (TCC). Code 7 (CLR): clears all register of the HBI.

The input cycle starts with an RG (Read Gated) signal, (see Figs. 9 and 12), which will clear the output register (OR). A DD signal is sent back to the computer after 4 μsecs. Again 4 μsecs later the contents of the Y register will be strobed into the output register (OR), followed by another DD 4 μsec later. At the same time a 500 μsec delay is triggered (OS3). The end of this delay will start the actual scanning operation. The logic is shown on Fig. 12. The output

of OS3 sets FF 'A', the output of this FF will now allow FF 'B' to be set upon the next pulse from the 2 MC/S clock. The output of FF 'B' will start the sweep and allow the clock to have access to the X-counter (X CNT), see Fig. 11.

What will happen now when a Track Center Pulse (TCP) appears at the input of PA1? If the present value of the X-counter lies between XS and XF and the computer is not tied up reading previous data (FF 'C' = 1), FF 'D' will be set and the next clockpulse will produce the Strobe-X pulse (PA2), which will have the following effect: the contents of the X-counter are strobed into the output register; a DD signal is sent to the computer after a delay of 0.5 μsec to allow time to Strobe-X into OR; FF 'D' is reset, which prevents that more than one Strobe-X pulse is produced; also FF 'C' is reset, which prevents that another TCP sets FF 'D' while the computer has not yet accepted the data which is strobed into the OR.

The value of the X-counter lies between 0 and 4095. After 4096 counts the X-counter will send an EOL signal which will reset FF 'A' and thus FF 'B' will be reset upon the next clockpulse, which determines the end of the sweep and no more X-CNT pulses will be produced. An EOL will start the same sequence as the first RG caused, namely: CLR, OR, 4 μsec delay, DD, 4 μsec delay, Strobe-Y, 4 μsec delay, DD, 500 μsec delay, Start Sweep. Except for the case when YS = YF, then an EOR signal is sent to the computer to indicate the end of a scanning operation. Depending on the contents of the Density FF, an EOL will produce one or two Y counts (Y CNT). If the Density FF = 0, one Y CNT is made by every EOL. If the Density FF = 1, two Y CNT's are made by every EOL. The value of the Y-counter may lie between 0 and 1023, depending on the YS and YF value. The outputs of the Y-counter are connected to a 10-bit Digital-to-Analog converter (D/A); the output of this converter is used for the Y deflection (see Figs. 9 and 11).

Stanford Linear Accelerator Center — Stanford University	STATUS	CODE	SERIAL
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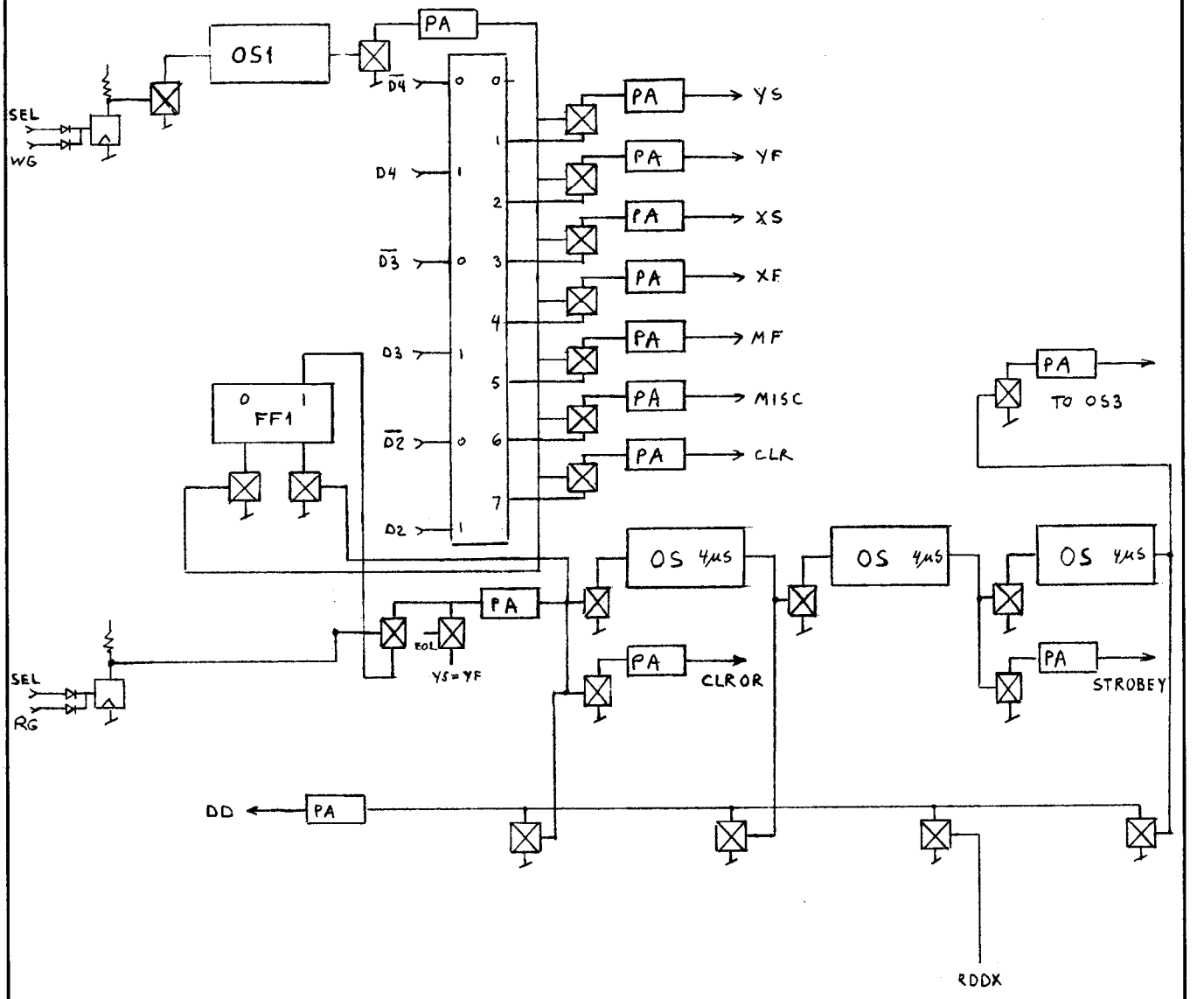
AUTHOR **H.J.Slettenhaar**	DATE	PAGE OF	
PROJECT—JOB **Hummingbird**			
TITLE Figure 8			



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AUTHOR H.J.Sletten haar	DATE	PAGE OF	
PROJECT—JOB Hummingbird			
TITLE Figure 9			

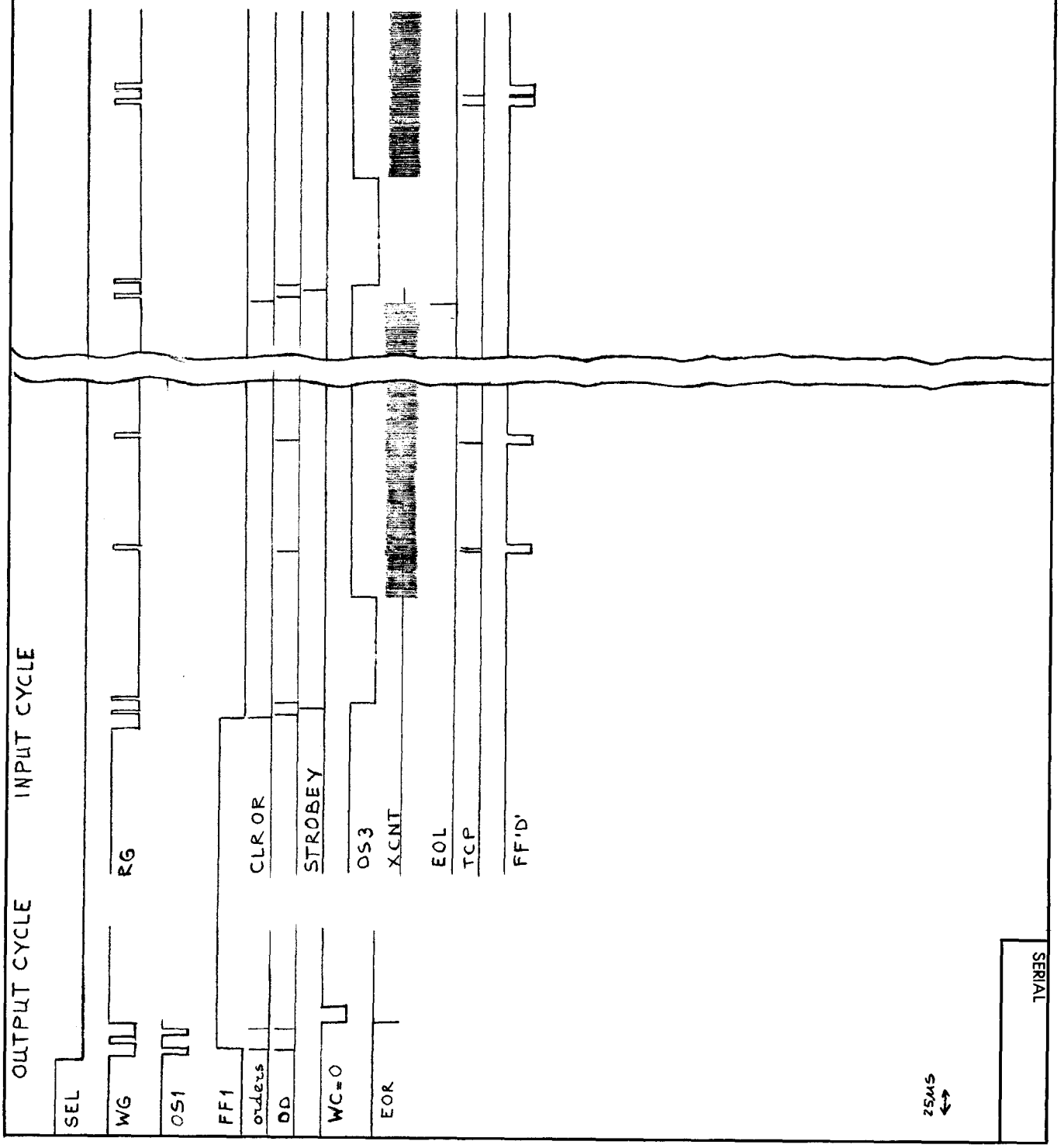
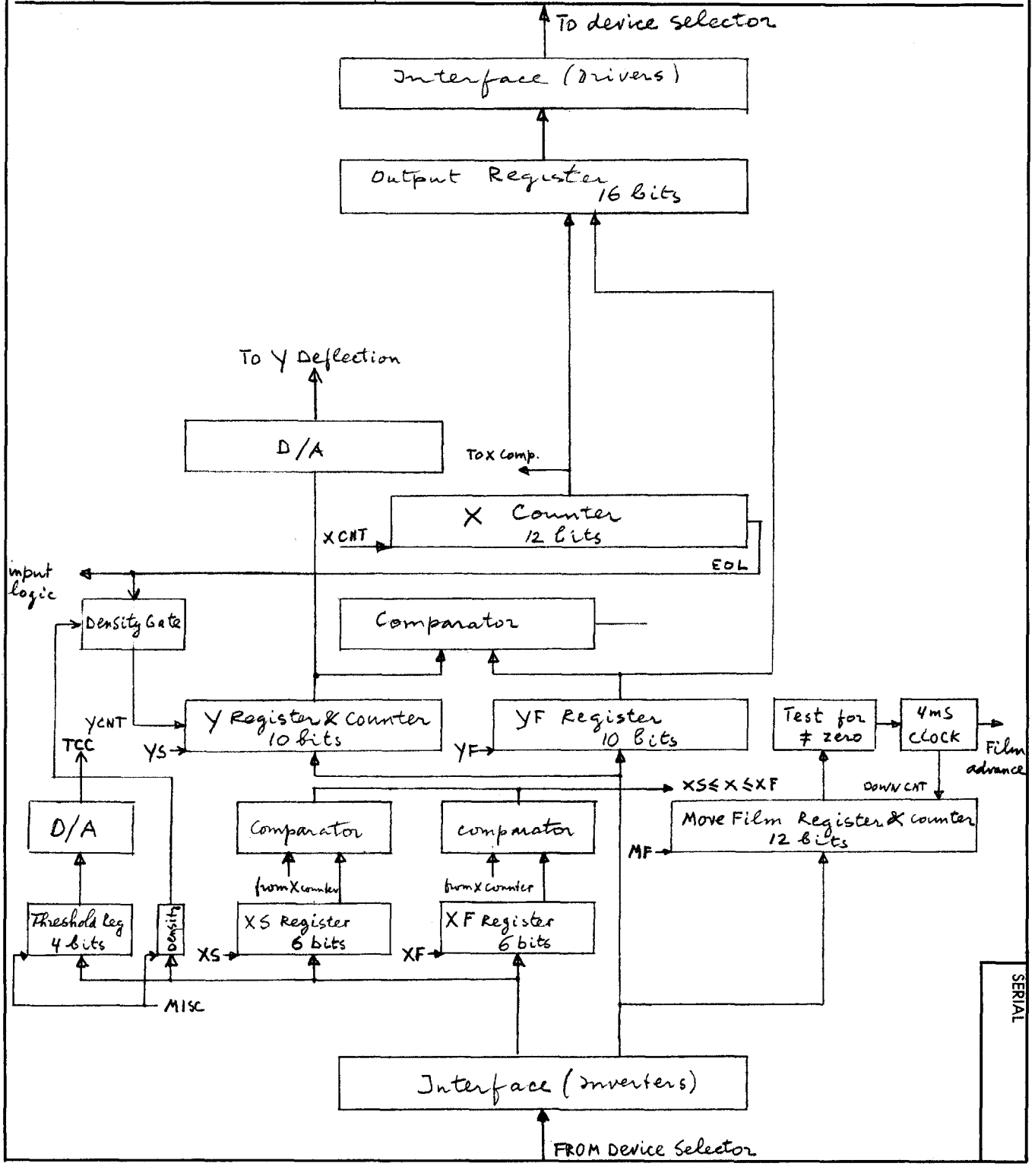
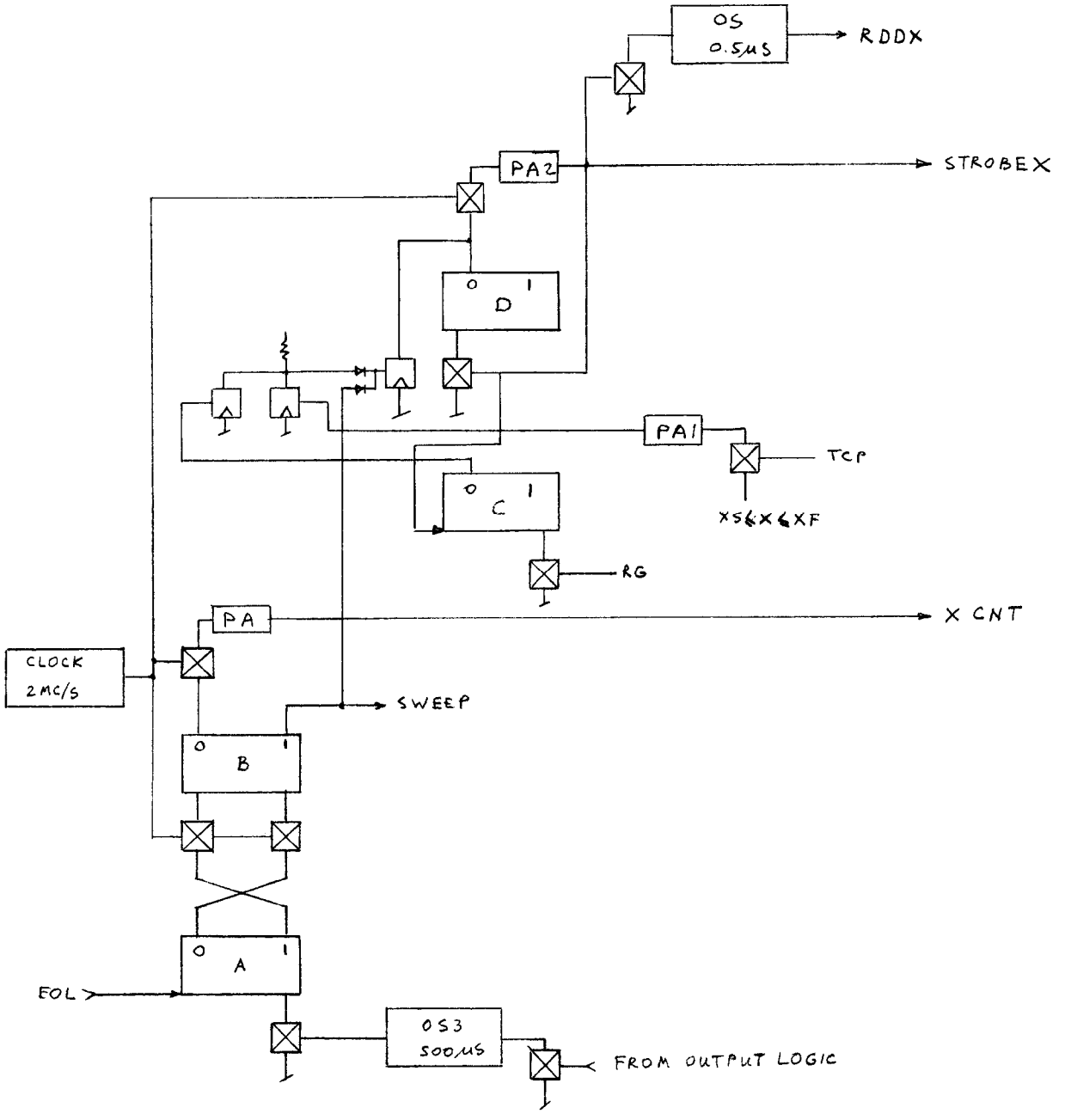


Figure 11


To device selector
Interface (drivers)
Output Register 16 bits
To Y Deflection
D/A
TOX comp.
X Counter 12 bits
XCNT
EOL
input logic
Density Gate
Comparator
YCNT
TCC
YS
Y Register & Counter 10 bits
YF
YF Register 10 bits
Test for ≠ zero
4ms clock
Film advance
XS≤X≤XF
DOWN CAT
D/A
Comparator
comparator
Move Film Register & counter 12 bits
MF
from X counter
from X counter
Threshold leg 4 bits
density
XS
XS Register 6 bits
XF
XF Register 6 bits
MISC
Interface (inverters)
FROM Device Selector
SERIAL

Stanford Linear Accelerator Center — Stanford University	STATUS	CODE	SERIAL
ENGINEERING NOTE			
AUTHOR	DATE	PAGE OF	
PROJECT—JOB			
TITLE Figure 12			



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HUMMINGBIRD 9

General

This section describes a feature, which exists on the HB I, namely the possibility to obtain grey-level information rather than track digitizings from film. In this way we are able to scan all kinds of "non digital" film, such as X-rays.
To the outside (Computer)world the HB 9 is a differend machine, which can be selected by addressing Device # 9.
There are seven grey-levels, which occupy 3 bits of a computer input-word of 16 bits of which the X co-ordinate occupies the 12 least significant places.

Output/Input cycle

Fig. 13 shows the first word of an output cycle. To select the HB 9 bit 13 should be 'one'.

Data Out

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

Fig.13

The output codes of the HB 9 are identical to those of the HB 1 However the HB 9 has one more output code. This is code 14, which is similar to code 6. As we see on Fig. 14 ,both codes have 4 data bits, which contain Threshold information. In the HB 1 this information is used to obtain a threshold level for the Track Center Circuit (TCC). In the HB 9 we use two levels to specify, which part of the Photomultipliersignal is to be decoded into grey-levels.

Data Out

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	1	1	0	X	X	X	X	0	0	0	0	0	0	0	0
1	1	1	0	X	X	X	X	0	0	0	0	0	0	0	0

Fig. 14

Of the 8 remaining data-bits of both codes only bit 12 is used to specify the Y density : Bit 12=0, density=1024 ; Bit 12=1, density= 512.

The input cycles of the HB 1 and 9 do not differ as far as the X and Y counters are concerned. The difference is the way the X-data and grey-levels are presented to the computer.

While the HB 1 is only sending an X co-ordinate after receiving an Track center pulse (TCP), the HB 9 is sending an X co-ordinate every 4 usecs together with 3 bits of grey-level information. (see Fig. 15)

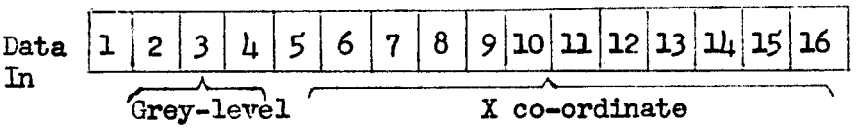

Fig. 15

The 4 usec interval between data-words is the smallest interval we can make because of the slow transfer rate of the Computer PDA.

In order to get a better overal 'picture' , we sample and send grey-level information in the following way :

During Y=Ys grey-level samples are sent every 4 usecs starting at X=4. As the X counts are 0.5 usecs apart, the next sample will be sent during X=12 then X=20 and so on.

During Y=Ys + 1 the starting point is at X=2, the next sample at X=10 and so on.

If the Y density is set at 512 lines, the sampling points will be always the same starting at X=4.

The HB 9 logic

The logic is shown on Fig. 16.It consists of two 4 bit registers with outputs connected to D/A converters. The upper register is set by code 6. The output of the D/A converter is called the upper threshold. The lower register is set by code 14 and its D/A converter output is called the lower threshold.

The voltage level of each D/A converter lies between 0 and -10 volts, it depends on the contends of the 4 bit register, which binary value lies between 0 and 15.

The signal which we get from the Photo-multiplier may vary between 0 and -10 volts.

The outputs of the two D/A converters are interconnected by means of 6 resistors of equal value. In this way we obtain seven voltage-levels with equal difference. These seven voltage-levels are connected to one input of seven comparators, which have the PM signal on the other input. The output of a comparator is true, when the PM signal is more negative than the level-input.

The outputs of the comparators are also inverted and sent to gates, which decode the 7 outputs into three binary levels. These three levels are at the inputs of three FF's (G0-G2), which are strobed * every 4 usecs during a sweep. The outputs of these FF's are the input Data-bits 2,3,4 (see Fig.15 .The FF's are cleared 2usecs before strobing. The position of the strobing depends on the setting of the 'ODD' FF. If this FF is in the '0' position, the strobing takes place every time when 'X 2' goes to zero. (see Fig.17. If the 'ODD' FF is in the '1' position, the strobing takes place every time when 'X 2' goes to one. The inputs of the 'ODD' FF are counter connected. Every Y count changes this FF. (If the density is 512, we get 2 Y counts after every line, the 'ODD' FF will thus remain in the zero position.) Fig.17also shows the position of the CRT spot at the sampling points during a scan with density 1024.

* The strobe pulse (STR) is treated in the same way as the HB 1 TCP and has the same effect.

Stanford Linear Accelerator Center — Stanford University	STATUS	CODE	SERIAL
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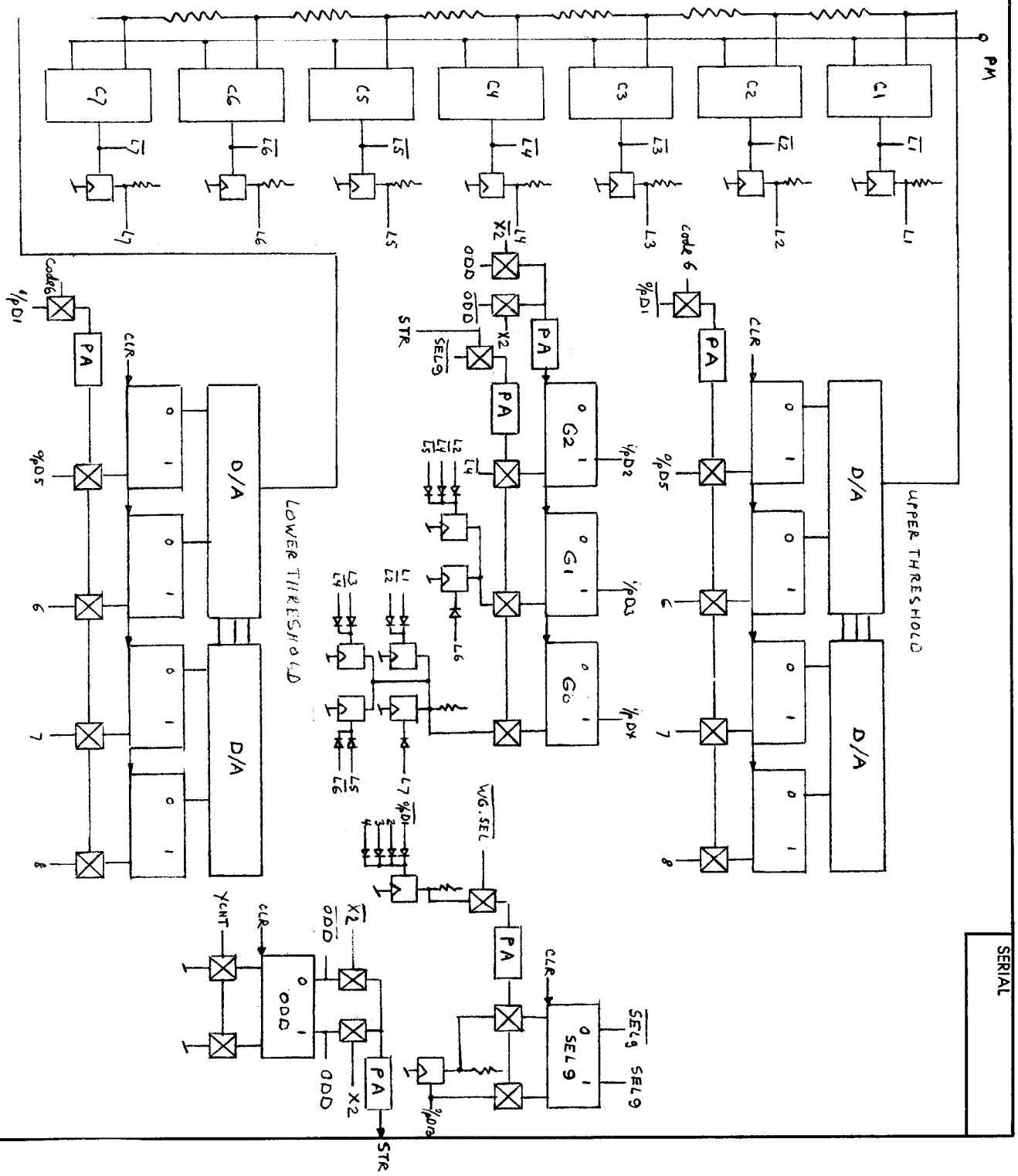
AUTHOR: H.J.Slettenhaar	DATE	PAGE OF	
PROJECT—JOB: Hummingbird 9			
TITLE: Figure 16			



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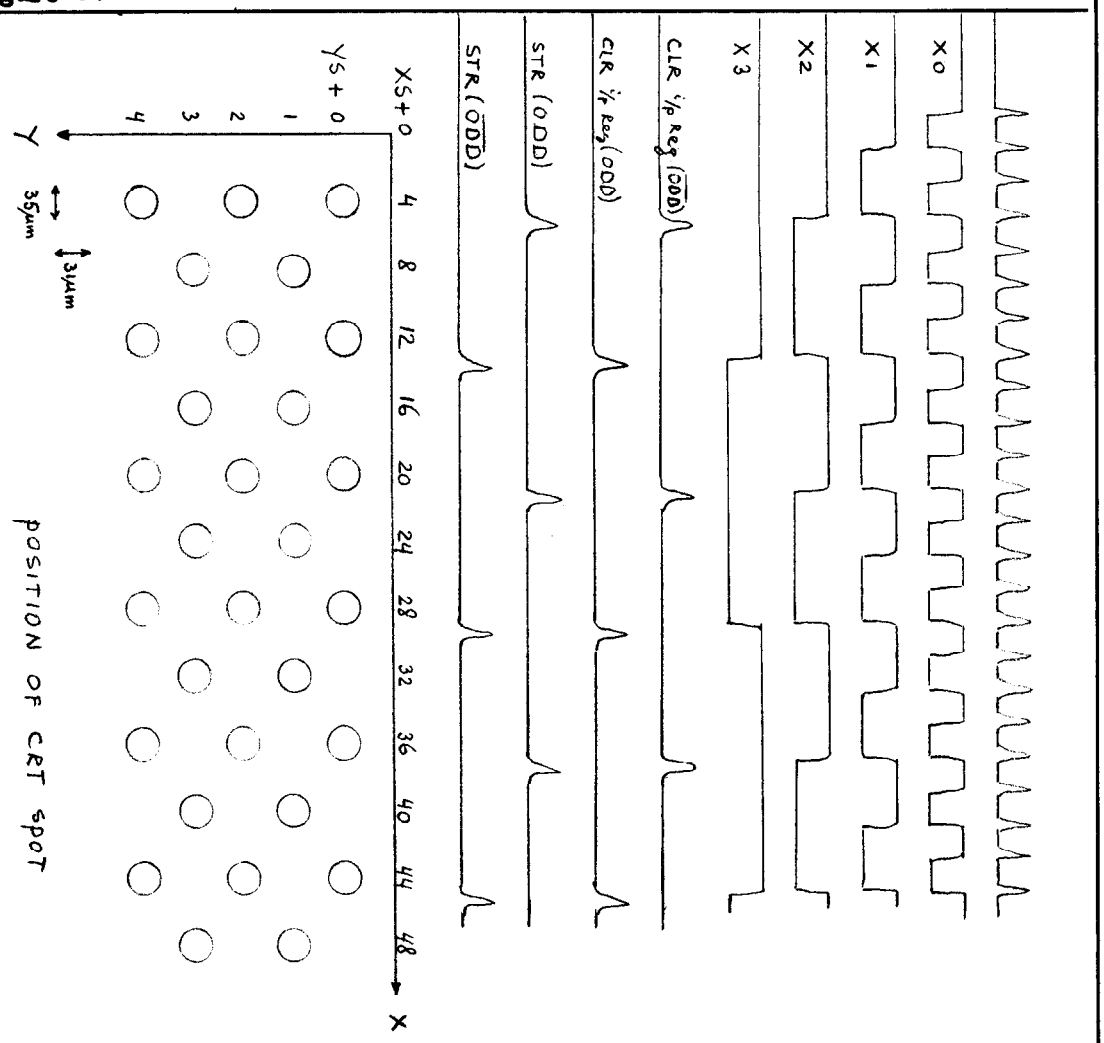
PROJECT—JOB **Hummingbird 9**			
TITLE **Figure** 17			



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