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TIME-INTERLEAVED-SAMPLING FOR HIGH BANDWIDTH BPM SIGNALS *

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Abstract

In the realm of Beam Position Monitor (BPM) signal processing, the reporting of signal phase and magnitude is typically achieved through either digital or analog down-conversion at a single RF frequency. Nevertheless, the raw digitized BPM signal may encompass a broader bandwidth with multiple beam harmonics that could prove useful. This paper describes an FPGA implementation designed to efficiently capture the full bandwidth of the BPM signal, utilizing minimal processing resources. This scalable approach allows for the capture of as many beam harmonics as required, constrained only by the bandwidth of the employed ADC. The BPM signal's periodic nature is leveraged in conjunction with time-interleaved sampling to effectively multiply the ADC's sampling rate.

INTRODUCTION

The Facility for Rare Isotope Beams (FRIB) is a new scientific user facility for low energy nuclear science that provides some of the highest intensity beams of rare isotopes available anywhere [1].

The Beam Position Monitor (BPM) system at FRIB is one of the most important diagnostic systems for beam tuning [1] [2]. Shown in Fig. 1, there are 152 BPMs deployed throughout the approximately 500 meters of beamline. The BPMs are utilized to report beam position offset (in mm), beam intensity, and beam phase [3]. The BPM phase information is utilized to calculate beam energy between two BPMs [4]. At the FRIB, we utilize a Field Programmable Gate Array (FPGA) and front end analog-to-digital converters (ADCs) to digitize signals from the four BPM buttons, perform digital down-conversion (DDC) at the 2nd harmonic of the RF frequency ($2 \times 80.5 = 161$ MHz), and calculate the signal magnitude, phase, and position at 1 MHz rate. This data is averaged and decimated in the FPGA at 100 Hz, and software performs the next level of averaging and decimation, reporting a moving 1-s window average at 5 Hz rate.

This approach to BPM signal processing, focusing on a single RF frequency, has met the FRIB requirements to support tuning new beam ion species, commissioning the machine, and running experiments. Nevertheless, there is some interest in exploring the information contained in higher-order beam harmonics, especially in the longitudinal distribution and bunch length of the RF modulated beam. It is beyond the scope of this paper to evaluate the merits of such efforts, but simply to provide a BPM data acquisition framework that can efficiently capture BPM signals with multiple beam harmonic frequencies.

Proposed here is a method to acquire exactly one RF period of an average BPM signal in the form of a time-series sampled at (virtually) any desired sample rate. The number of points in such a time series is directly proportional to the number of beam harmonics captured. The only limit to the frequencies captured is the analog bandwidth of the BPM buttons, any analog front end electronics, and the employed ADC.

BPM SIGNAL PROCESSING

In order for BPM signal processing to be as efficient as possible, the ADC sample rate is a critical parameter that has implications for window averaging filter design and memory requirements.

Digital Filters and Signal Processing

At FRIB, BPM signals are sampled by ADCs at 119 MHz, which is phase-locked with the bunch rate of our machine, and uses the same 80.5 MHz REF clock that the RF accelerating cavities are synchronized with. This sampling frequency was chosen to allow hardware efficient window averaging filters while suppressing unwanted frequencies and cancelling all other beam harmonics. The ADC clock of 119 MHz is phase-locked at a frequency ratio of 34/23 relative to the 80.5 MHz clock. This means that exactly 23 full periods of 80.5 MHz will be sampled by exactly 34 points.

The ADC data is processed by a digital board utilizing a Xilinx Spartan-6 FPGA. After demodulation at 161 MHz, in-phase quadrature (IQ) data can be easily filtered to reject frequencies outside of baseband by cascaded window integration (CIC) filters, which are essentially moving window averages. The first window integration has length of 34

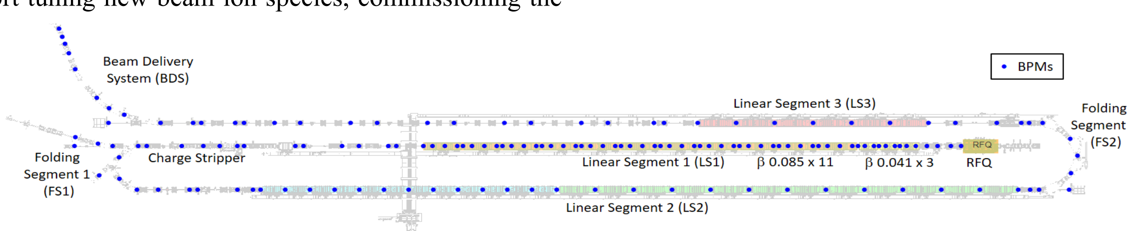

Figure 1: Overview of FRIB linac with BPM locations.

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samples. Since this corresponds to exactly one full period, summing this number of IQ data points nullifies all other beam harmonics and modulation products, as can be seen in Fig. 2. The frequency response of the 34 samples long CIC filter is shown, along with locations of all the beam harmonics. The 2nd harmonic is passed, while all others are nullified. The Nyquist portion of the spectrum is shown below, where 161 MHz signal is aliased to 42 MHz when sampled by 119 MHz.

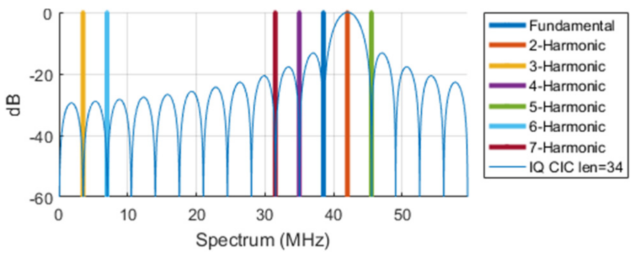

Figure 2: ADC sampling at 119 MHz, aliasing of beam components, and first CIC integration filter.

Standard BPM Signal Processing

The standard BPM signal processing chain take this IQ data and passes it through additional CIC filters and decimates at 1 MS/s. This fast data is stored in local memory on the FPGA board as a circle buffer, continually acquiring up to 1-second of IQ data for each button at 1 MS/s. This buffer can be paused and read back for detailed study, however for typical BPM diagnostics, the IQ data is further averaged and decimated to 100 Hz in the FPGA prior to being passed to a CPU for further averaging. The CPU takes the 100 Hz data and implements a 1-s moving window average, reporting BPM readings at 5 Hz rate.

This BPM system provides a very responsive real-time monitoring of position, phase, and intensity for each BPM. Figure 3 plots the BPM intensity magnitude and X, Y positions displayed as a stem plot for the first 73 BPMs. The BPM signal magnitude increases just before entering the accelerating linac, at BPM #5, and then gradually decreases as beam velocity increases and transit time through the BPMs decrease. At the time Fig. 3 was taken, beam transport was being tuned to a beam dump at the first folding segment, FS1. At that time, BPMs show beam centered within ±5 mm, however this was later improved to ±1 mm by the time beam tuning was complete.

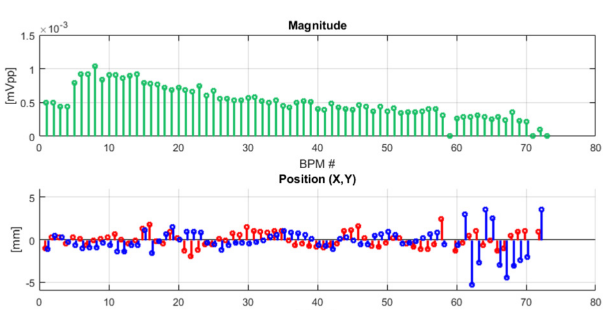

Figure 3: Stem plots showing 73 LS1 BPM's position and intensity.

ALTERNATIVE BPM PROCESSING

By utilizing the same ADC data, a completely independent method of BPM signal processing is possible to implement in parallel. The method described here, called time-interleaved sampling (TIS), takes advantage of the periodic nature of BPM bunch signals and the phase-locked ADC sample clock to repeatedly sample a set of phases within the bunch frequency period. This method effectively samples the BPM waveform at many times the actual ADC sample rate. The BPM electronics that we designed and deployed for the LS1 section support a digitization bandwidth up to 500 MHz. The time-interleaved sampling method described here is designed to captures all the available beam harmonics in an efficient manner.

Time-Interleaved Sampling Waveforms

With the high-bandwidth digitizing boards, there is additional harmonic frequency information available, however the standard DDC IQ processing only uses a single frequency. By choosing the ADC sampling rate as a rational fraction of the beam bunch rate, 80.5 MHz, all of the beam harmonics can be recorded in a hardware efficient manner. In our case, the 119 MHz ADC sample rate was chosen such that 34 consecutive clocks will sample exactly 34 discrete phases of the 80.5 MHz bunch rate. In FPGA firmware, 34 accumulators are implemented in order to store this 34-sample waveform for each BPM button. Each RF sample is binned and added to one of 34 accumulators as it arrives. For each BPM button, the hardware resource requirements are minimal: 34 registers of 36 bits, and a 36 bit + 14 bit adder (assuming a 14-bit ADC). With only these resources, it is possible to bin and sum an entire second of 119 MS/sec data into a 34-point waveform which represents the average BPM button response, sampled at the equivalent rate of 80.5 MHz × 34 = 2.737 GHz. This method is very similar to random interleaved sampling (RIS), in which multiple ADC acquisitions would be used to sample a signal with different sub-sample time delay offsets. This approach is described in [5].

This 34-point time-interleaved sampled waveform contains frequency information for the beam fundamental and all harmonic frequencies, which are the only frequencies we are interested in. Our BPM analog front end incorporates a lowpass filter with cutoff around 500 MHz, so up to the 6th beam harmonic is recorded in the TIS waveform (6 × 80.5 MHz = 483 MHz). Conveniently, a 34-point FFT of these waveforms will result in 34 complex values which contain the magnitude and phase information of each beam harmonic.

Figure 4 shows the TIS functional implementation, where an ADC sample is only used when beam is active, and the waveforms are collected every 100 Hz into a 1-s sum waveform. Figure 5 shows an actual BPM response, including spectrum. The bipolar waveform reflects the capacitive nature of the BPM button pickup.

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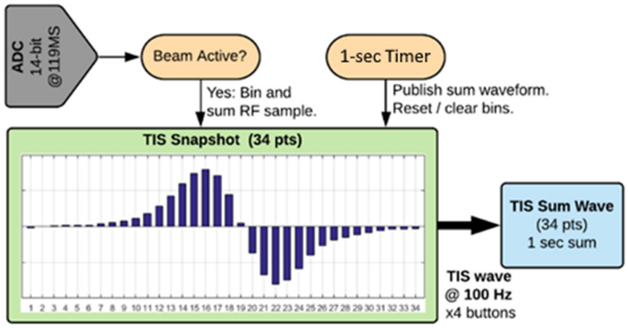

Figure 4: TIS functional implementation diagram.

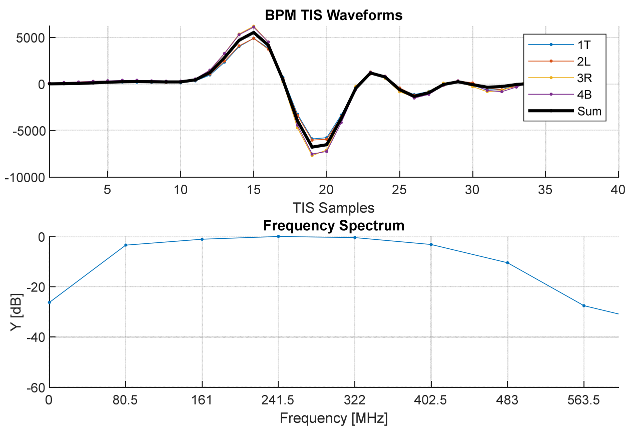

Figure 5: Single BPM TIS RF waveforms and sum (top) and spectrum in dB (bottom).

Bunching Effect on BPM Waveforms

As the beam is accelerated through the linac, the particles are also bunched, compressing them into shorter bunch lengths. Decreased bunch length and increased velocity both result in increased BPM signals from higher-order harmonics. This effect is illustrated in Fig. 6 below, which shows BPM waveforms taken during FRIB tuning activities. The five BPM waveforms correspond to different locations in the first accelerating segment, LS1. Beam energy began at 0.5 MeV/u and exited LS1 at 18.2 MeV/u.

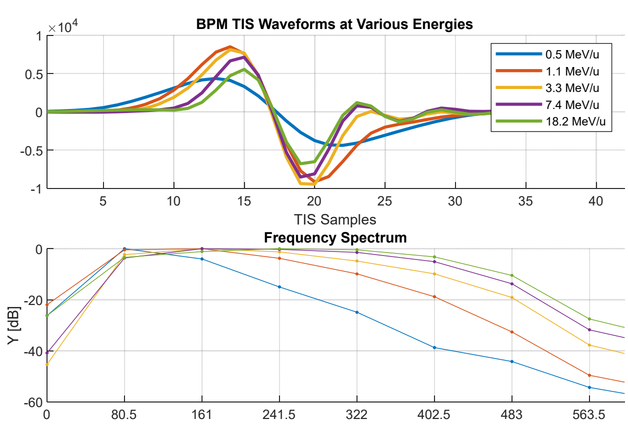

Figure 6: TIS waveforms and spectra at different energies.

TRACKING MULTIPLE CHARGE STATES

After a recent BPM firmware upgrade, we doubled the number of points in our TIS waveforms, from 34 to 68. This was done to capture 40.25 MHz bunch information. At this point in FRIB commissioning, we are achieving high transmission efficiency by bunching beam at 40.25 MHz rather than 80.5 MHz. This means every other 80.5 MHz bucket is empty, as can be seen in Fig. 7. We have future plans to increase throughput by transporting two different charge states in alternating buckets. The beam transport dynamics will be slightly different for each charge state, which may be reflected in these TIS waveforms.

The standard approach to BPM processing would not support independent tracking of these two charge states in alternating buckets. However, with the expanded 68-point TIS waveforms, we will capture the waveforms for both charge states. This will lead to independent X, Y position, phase, and intensity readings for each charge state at each BPM location.

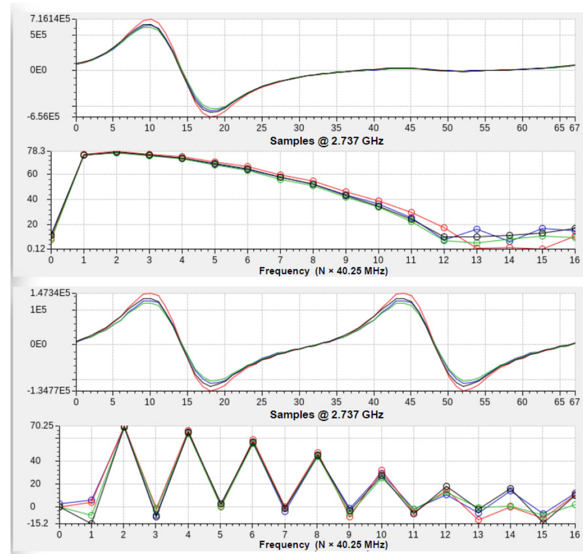

Figure 7: Two 80.5 MHz buckets shown with 40.25 MHz prebuncher on (top) and off (bottom).

CONCLUSION

The time-interleaved sampling approach to BPM signal processing is quite powerful and requires relatively little FPGA resources. Expensive FPGA operations which are normally part of the DDC approach to BPM signal processing could be eliminated. There is no need for CIC filters, IQ data conversion, etc. A small amount of waveform data can be sent to a CPU periodically to run a Fast Fourier Transform (FFT) and perform remaining BPM algorithms for position, phase, and magnitude.

In future applications, the additional frequency content of the BPM signal may also be leveraged for more insightful and useful diagnostics from the BPM system.

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