DEVELOPMENT OF A 500 MHz DIRECT RF SAMPLING LOW-LEVEL RF SYSTEM FOR ALBA AND ALBA-II

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Abstract

ALBA Low-Level RF (LLRF) system has provided over a decade of reliable operation and has been adopted by other synchrotron facilities. To meet the evolving requirements of ALBA and ALBA-II, a new LLRF system has been developed. This system features FPGA and ADC/DAC μTCA boards designed by Safran, enabling direct 500 MHz signal sampling without down/up-conversion. These enhancements reduce system complexity, minimize noise, and simplify maintenance. Safran also supplies peripheral modules and the Tango device server generator, while ALBA implemented it and developed a new GUI. Upgraded Digital and RF signal front-ends complement the new hardware. The legacy VHDL code has been updated to improve readability and functionality, incorporating advanced features such as octant selection and a harmonic direct feedback selection method. The latter, based on IIR filtering, isolates positive and negative revolution harmonics in the I/Q domain, feeding them back to amplifiers to effectively mitigate transient beam loading caused by the storage ring bunch train gaps. This upgraded LLRF system delivers enhanced performance and greater flexibility to address the future needs of ALBA and ALBA-II.

INTRODUCTION

The ALBA Digital Low-Level RF (LLRF) system development project began two decades ago, with initial commissioning aligning with ALBA's operational launch in the early 2010s. The system was built around FPGA and ADC/DAC boards designed by Lyrtech (later Nutaq), complemented by in-house-developed RF and Digital front-end hardware [1-5]. This architecture has since been adapted and deployed in slightly modified configurations at several international particle accelerator facilities, including IFMIF-EVEDA, Diamond Light Source, MAX IV, SOLARIS, Sirius, CLS, and Bessy II [6-12].

Evolution and Modernization

Although the system achieved full functionality by 2012, continuous development expanded its capabilities through gateware updates and hardware optimizations. However, reliance on legacy Virtex-4 FPGAs (programmed via Xilinx ISE, discontinued in 2013) necessitated modernization. To leverage newer tools like Xilinx Vivado and integrate advanced features, ALBA initiated a transition to Zynq UltraScale+ SoCs. This platform consolidates the control server onto the embedded ARM processor, streamlining device-server development while maintaining compatibility with existing RF front-end designs.

New Digital Low-Level RF specification

The new ALBA Digital Low-Level RF is based on the RF direct sampling then both input and output (control) signal to/from ADC/DACs are 500 MHz and no down/up-conversion is being used. The system then is more compact and less prone to non-linear effects. The FPGA and ADC/DAC boards are designed by Safran Electronic & Defense Spain S.L.U. in a μTCA.4 standard, distributed on AMC and RTM boards connecting to μTCA chassis, back-to-back. Safran also provided the FPGA peripheral modules to receive/send the input/output RF signals in I/Q format and to read/write GPIO pins and write to memory for fast data logger and provide the tango device server generator for the control system.

System Architecture

The new LLRF system comprises three sections, Fig. 1:

1. Hardware:
   - FPGA and ADC/DAC Boards: Safran-designed Zynq UltraScale+ ZU6EG-based μTCA modules.
   - RF Front-End: Handles input/output RF signals from cavities, amplifiers, circulators, and couplers and to RF amplifiers.
   - Digital (GPIO) Front-End: Receive interlocks, vacuum thresholds, timing trigger, and send control signals to the tuner motor controller.
2. Gateware:
   - ALBA LLRF VHDL Core: Custom-developed gateware to monitor and control RF cavities fields.
   - FPGA Peripheral Entities: Vendor-provided interfaces for ADC/DAC and communication.
3. Software (Control):
   - Tango Device server for the Control system

Hardware – FPGA and ADC/DAC Boards

The LLRF hardware platform is designed and tested by Safran as part of the upgrade program for the ALBA Synchrotron Light Source in Barcelona. It is based on a modular μTCA architecture and includes five dual-channel, 16-bit analog-to-digital converters operating at 160 Msps, two 16-bit DACs, and a Zynq UltraScale+ FPGA from Xilinx. The system is equipped with 32 general-purpose I/O ports, 8 GB DDR4 memory for data storage and postmortem analysis, and various timing and communication interfaces. It also features precision PLLs for internal clock

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generation, RF monitoring with up to nine inputs, and dual output channels to independently drive two cavity's RF amplifiers, each with its own amplifier and band-pass filtering, Fig. 2. Precision measurements show amplitude stability down to 0.03% and phase accuracy better than 0.05° at 0 dBm input levels. Jitter figures are also outstanding resulting in a total added jitter of only 170 fs.

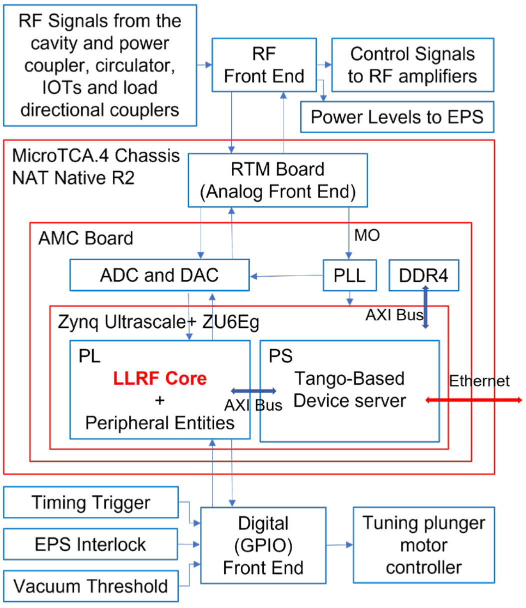


Figure 1: Digital LLRF layout.

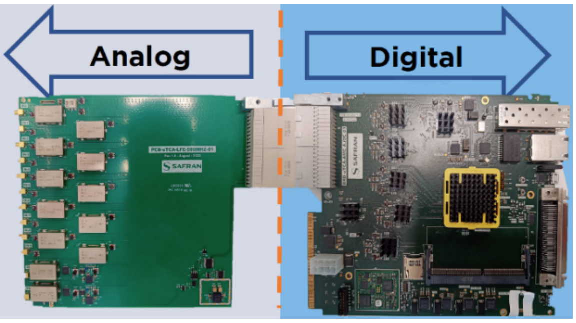


Figure 2: Safran AMC and RTM boards includes FPGA and ADC/DACs.

Hardware – RF and Digital Front-Ends

The RF Front-End receives all the RF input signals from the cavity pick-up antenna and all the directional couplers installed on cavity coupler, circulator, load and IOTs. The RF Front-End sends the power level to EPS system and provides BNC ports for real-time monitoring and signal routing to ADC. The Front-End also receives the control signals from DAC, sends them to RF amplifiers and includes RF pin diode switches to stop the RF immediately. It also provides master Oscillator (MO) signal to ADC/DAC and FPGA boards to produce all the required frequencies though PLL. The Digital (GPIO) Front-End, developed in ALBA, receives the timing trigger, EPS Interlock, Vacuum Threshold (for RF conditioning) and HW stop signals and send them to FPGA. It also receives cavity tuner motor controller signal and HW stop out signals from FPGA and send them to related devices, Fig. 3. Figure 4 shows the in-operation new LLRF system.

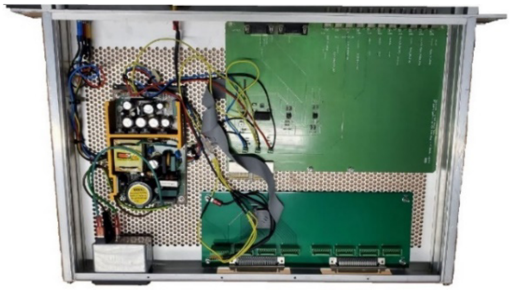


Figure 3: Digital (GPIO) Front-End.

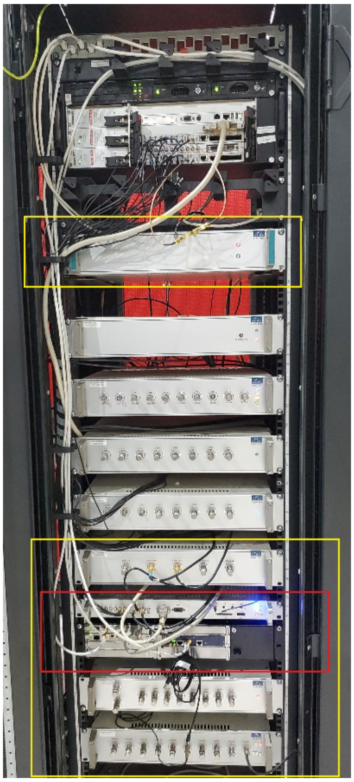


Figure 4: New and old LLRF systems. Yellow shows the new LLRF system which includes AMC/RTL boards and Digital front-end (red) and the shared RF front-ends.

Gateware

In the ALBA LLRF Core, written in VHDL, the main tasks are performed. It was developed initially on 2010s and different features added to it in the past decade. It monitors RF signal inputs and it has PID loops and a tuning loop to produce the RF control signals and to control the cavity tuner [1, 2]. It also features an RF trip compensation mechanism [3], RF cavity auto-recovery, RF conditioning and a simple direct feedback mechanism. It was developed for 80 MHz FPGA frequency which received 20 MHz RF signals using I/Q sampling method. Since the new FPGA works on 160 MHz and the input 500 MHz signals are direct-sampled by 160 MHz ADCs, the non-I/Q sampling method is used to translate the RF signals to I/Q domain. To upgrade for the new LLRF system, the whole VHDL code was reviewed and matched to the new frequency and the new sampling method. A top module for the LLRF core was developed to connect it to all peripheral modules, provided by Safran. Direct Feedback mechanism was upgraded significantly and 1st and 2nd revolution frequency harmonics feedback were added. Figure 5 shows the new direct feedback mechanism. Due to the transient beam loading induced by non-homogenous filling pattern, revolution frequency harmonics appear in the cavity. The goal of the new direct feedback system is to reduce these components inside the cavity and to mitigate the PTBL instabilities that appear in the double RF system. Two IIR bandpass (0.3 MHz BW) filters were designed to filter out first and second harmonics in 1.115 MHz and 2.231 MHz. Then they are multiped to a complex gain and added to the control signal. General direct feedback is also provided which mainly act on the main frequency (zero mode), since its contribution is much higher than other frequencies. The direct feedback system can separate the positive and negative harmonics. A new equation was derived, Eq. (1), to separate the positive and negative harmonics in I/Q domain. Ω represents the harmonic angular frequencies which are 2π(1.115) and 2π(2.231) MHz for the first and second harmonics, respectively. Preliminary tests show its effectiveness [13].

$$\begin{cases} I^{\pm} = \frac{1}{2}\left(I \pm \frac{dQ}{d(\Omega t)}\right) \\ Q^{\pm} = \frac{1}{2}\left(Q \mp \frac{dI}{d(\Omega t)}\right) \end{cases} \tag{1}$$

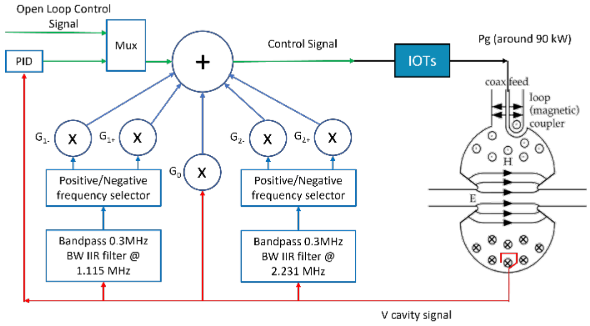


Figure 5: The new direct feedback mechanism with revolution frequency harmonics feedback.

Software

The Tango-based [14] device server is running on the ARM core of the Zynq UltraScale+. The LLRF Device Server Generator, developed by Safran, automates the creation of Tango device servers from a structured Yaml [15] configuration. It defines attributes with their names, types, memory addresses, and optional formulas for converting raw FPGA register values into readable formats. By combining these configurations with a Jinja2 [16] template, the generator produces consistent, maintainable Python code with minimal manual effort. It supports multiple data types and clearly distinguishes between writable and read-only attributes. Conversion formulas are automatically applied during read/write operations, and while the "tab" field is ignored by the device server, it is retained for GUI use to maintain consistency between backend and frontend components. The LLRF Control GUI, see Fig. 6, built with Taurus [17], loads the same Yaml file dynamically and organizes attributes into tabs. It splits writable and read-only attributes into separate panels and groups I, Q, Amplitude, and Phase values into matrix views. The GUI can reflect Yaml updates without reinstallation and includes a shortcut to display raw FPGA values, offering both intuitive control and deep diagnostics.

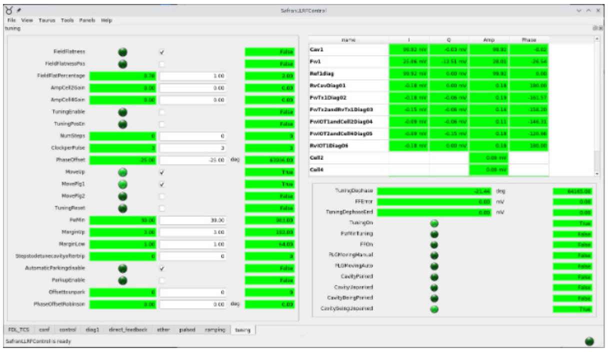
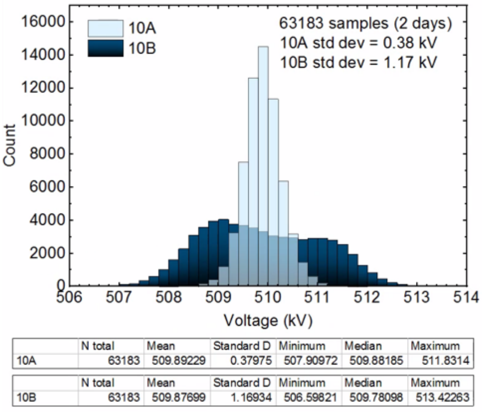


Figure 6: The designed GUI to communicate with device server for the control room operators.

Operation

The new Digital LLRF is in operation in two out of the six ALBA main cavities since December 2024 and May 2025. The plan is to replace all main ALBA cavities LLRF systems until the end of this year. The new LLRF system passed all the tests including trip compensation. It also shows a better field stability in the closed loop operation in comparison to the old LLRF system. Figure 7 shows the long-term voltage stability inside the cavity, comparing the new LLRF system to the old LLRF system. The new ALBA LLRF system voltage stability is 0.07% in comparison to 0.23% in the old LLRF system. And the cavity phase stability in the new LLRF is 0.04° in comparison to 0.07°.



	N total	Mean	Standard D	Minimum	Median	Maximum
10A	63183	509.89229	0.37975	507.90972	509.88185	511.8314

	N total	Mean	Standard D	Minimum	Median	Maximum
10B	63183	509.87699	1.16934	506.59821	509.78098	513.42263

Figure 7: Long-run cavity voltage stability with new (light blue) and old (dark blue) LLRF systems.

CONCLUSION

The new LLRF system has proven successful in operation, delivering better cavity field stability. It is planned to replace all the current LLRF systems in ALBA, including those for the main cavities and the upcoming third-harmonic cavities operating at 1.5 GHz.

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