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Power distribution over the wafer-scale monolithic pixel detector — MOSAIX for ALICE ITS3

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Abstract: For the LS3 ALICE ITS3 upgrade the detector material budget reduction has been pushed to the limit by proposing a system composed almost exclusively of silicon wafer thinned down to 50 µm. This improves performance, but adds complexity to the ASIC design. It requires a wafer-scale module with embedded power delivery network and on-chip data transfer, which were usually done through flexible printed circuit cable.

This contribution covers different aspects of the power delivery network design for a wafer-scale detector. It describes the difficulties, shows possible solutions and presents the power scheme design of the full-size ITS3 sensor prototype MOSAIX.

Keywords: Particle tracking detectors (Solid-state detectors); Very low-energy charged particle detectors; Voltage distributions; Large detector systems for particle and astroparticle physics

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1 Introduction

The ALICE Inner Tracking System 3 (ITS3) upgrade aims to minimize the detector material budget by using ultra-thin (50 µm) silicon wafers as the primary component of the tracking layers [1]. For the ITS3, the MOSAIX detector serves as a full-size monolithic pixel detector prototype, designed using a 65 nm technology node, employing 1D-stitching to create a wafer-scale chip measuring 26.6 cm by 1.95 cm. It features a sensitive region divided into 144 independent tiles, each comprising a 444 x 156 pixel matrix ($22.8 \times 20.8\ \mu m^2$ pixel size). Each tile has a self-contained analog front-end and reads out pixel data through a double-column priority encoder with zero suppression. Pixel hit data is transmitted over 26 cm on-chip at 160 Mb/s to a data aggregator at the left endcap. Data is sent off-chip via 8 high speed current mode logic (CML) links, each running at either 10.24 Gb/s or 5.12 Gb/s [2]. The size of the device introduces challenges in power distribution, yield management, and power grid validation, as covered in this paper.

2 Power distribution challenges in MOSAIX

Distributing power over the device is a critical aspect of any modern large-scale design. It is especially difficult for the MOSAIX detector due to the ITS3 mechanical constraints, which restricts connections to the short edges only: Right End-Cap (REC) and Left End-Cap (LEC) [3]. This configuration requires power to be spread over 26 cm of Repeated Sensor Unit (RSU) using only on-chip metal layers made available by the sensor technology. Despite extremely low power consumption ($< 40\ mW\ cm^{-2}$), without any mitigation the significant IR drops from this setup could severely compromise the device performance, making efficient power distribution a key challenge.

Another important aspect of a wafer-scale chip design is the yield assessment. With only five MOSAIX chips per wafer, only a few shorts between power rails scattered across the wafer can lead to significant manufacturing losses. This becomes even more pronounced taking into account the size of the ITS3 layers, which require multiple (from 3 to 5) neighboring MOSAIX chips to form a

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complete layer. For this reason the detector must be designed in a way that minimizes the probability of critical faults but also is resilient to manufacturing defects.

3 Power network design

The power network for the MOSAIX detector is designed to address the two major challenges highlighted in section 2, yield and voltage drops. In order to independently tackle specific issues the chip powering scheme is composed of two layers (as shown in figure 1): the global power grid and the local power grid.

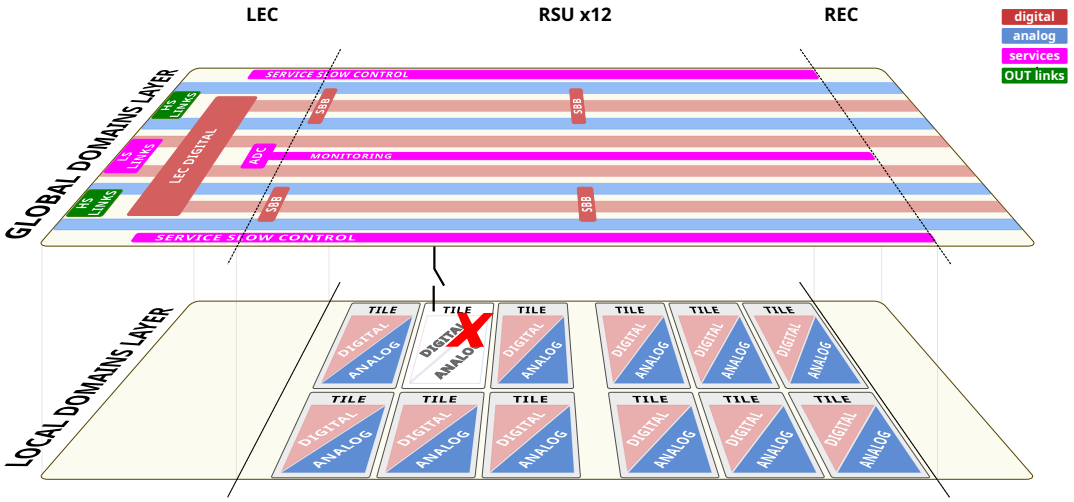

Figure 1. MOSAIX power network overview.

3.1 Global power grid

In MOSAIX there are four global power domains, that are supplied externally, out of which three spread along entire chip: two main ones, separate for the analog and digital circuitry and an independent one for the services enabling the chip configuration. The global power grid's primary role is to distribute power from the edges of the chip across its 26.6 cm long side. For this reason it utilizes two topmost metal layers, with the highest conductivity. It is designed in a very robust way, with large spacings (order of 10 µm) between different power rails, to reduce risk of lateral shorts. To further minimize the probability of shorts between global power rails the circuitry directly powered with the global supply is restricted only to the on-chip data transmission and chip configuration.

3.2 Local power grid

The MOSAIX readout circuitry is grouped into 144 self-contained design units, called sensor tiles. Each tile is composed of the pixel matrix, biasing circuitry and readout periphery, which are supplied with their own local power grid, that can be disconnected from the global one. This has two major benefits:

- Fault tolerance and defect isolation:

  In case of a manufacturing defect or short circuit in a particular tile, the tile can be isolated from the global power grid, ensuring that the rest of the chip remains functional. This design limits the impact of defects to an increase of dead area by 0.7 %.

- Suppressed impact of the global IR-drops:

  Non-uniformity over the power supply heavily impacts the analog performance of the MOSAIX detector (pixel threshold shifts by $1.5\,e^-/mV$). Thanks to the segmentation one can independently adjust settings between the tiles to compensate for the IR drops over the global network, keeping the high uniformity requirement only for the local power grid.

The local power grid is designed using two intermediate metal layers and is connected to the global grid by power switches located at the left edge of the tile. The switches location is particularly important for the local power grid uniformity, since it defines the coupling of global network IR-drops into a local network. They are implemented on both supply and ground rails in order to make a tile completely detachable. Switches are designed as a small units distributed uniformly along the tile edge that are steered by a common enable signal per tile.

3.3 Custom design rules and burnout strategy

To improve yield by minimizing the risk of shorts, custom Design Rules Checks (DRC) were introduced. These rules enforce larger spacings and widths of the metal routing, as well as check for multiple-cut vias and enlarged metal enclosures around them. To avoid constraining the entire design, all the MOSAIX sub-blocks are divided into three categories based on the impact in case of their failure and for each category different safety factors are applied. For example, the least critical blocks are required to respect routing widths and spacings 1.4 times the minimum one, which is further increased to 3 times for the most critical blocks. Since shorts between the power nets are particularly harmful, the power grid has been further constraint to ensure even larger spacing between different power rails which is checked with the connectivity aware DRC rules.

Additionally, the power grid is designed to recover from certain types of short circuits by delivering enough power to burn-through them. With previous prototypes it was observed that one needs to provide about 100 mA to the affected region to burn-out the short and restore normal operation, thus the power grid was designed to be able to deliver that current to any location [4].

3.4 IR drop over global supply

In order to cope with the IR drops over the global power network MOSAIX is exploiting the supply voltage operation margins of 10 % around the nominal 1.2 V. Figure 2 illustrates the worst case voltage drops over the global supply rails across the long chip edge (the z-coordinate), assuming supply connections only at the left and right end-caps and external supply voltage of 1.3 V It shows that despite extremely low power consumption ($< 40\,mW\,cm^{-2}$) drops can reach up to 100 mV on each rail, resulting in 1.1 V of the effective supply in the middle of the device. This is still within the acceptable limits, but implies a strong requirement on the circuitry to be fully operational in a wide range of supply voltages.

4 Power grid simulation

For the wafer-scale chip the IR drop simulation of the entire device requires too much computing resources to be executed, thus to validate the design and ensure that specifications are met a simplified model was used. Presented results are obtained with extracted view of the power network together

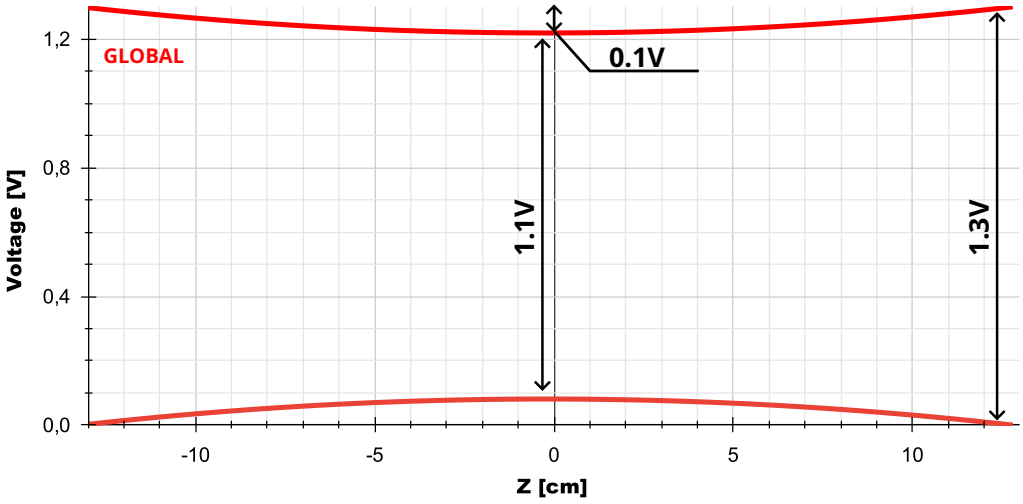

Figure 2. Worst case IR drop estimate.

with a dummy tile that loads the power grid with the uniformly distributed consumption expected from each sub-block.

Figure 3 shows the worst-case IR drop map of the global analog ground under high consumption conditions. As one would expect it shows a good vertical uniformity, and a horizontal parabolic pattern with the maximum in the center of the device reaching 94 mV. Similar results have been obtained for the other power rails, proving that the global power grid is in line with the initial estimates and design goals.

Similar analysis have been performed for the local power grids. In figure 4 the result for the local analog ground is shown as an example. In case of the local supplies, the results depend on the position of the tile, thus two extreme cases are shown: a tile in the middle of the device (left), and a tile next to the end-cap (right). In both cases there is a clear left to right pattern, reflecting the switches being located at the left edge of the tile. But for the tiles close to the end caps there is an additional pattern appearing. In case of the local analog ground these are two minima located at the left edge, at around 1/4 and 3/4 of the tile height. These are caused by the residual vertical non-uniformity of the global power grid related to the positions of the supply pads. This non-uniformity directly couple to the local power grid through the power switches.

Despite this effect, local analog supply achieves excellent uniformity, with less than 1 mV variation over the tile. The digital local grid exhibits slightly higher variation (up to 4 mV), but this is still within acceptable limits.

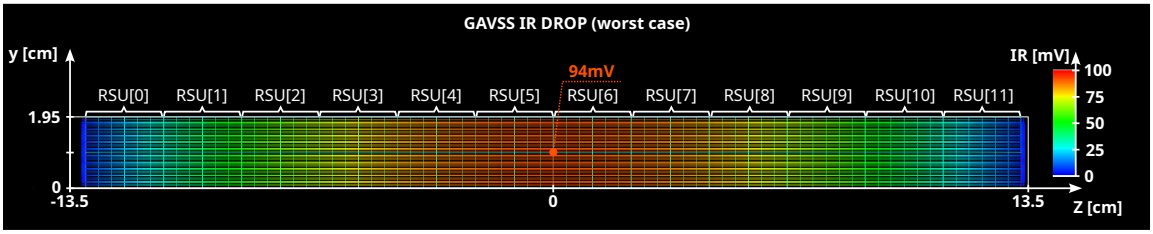

Figure 3. Worst case IR drop simulation result for the global analog ground.

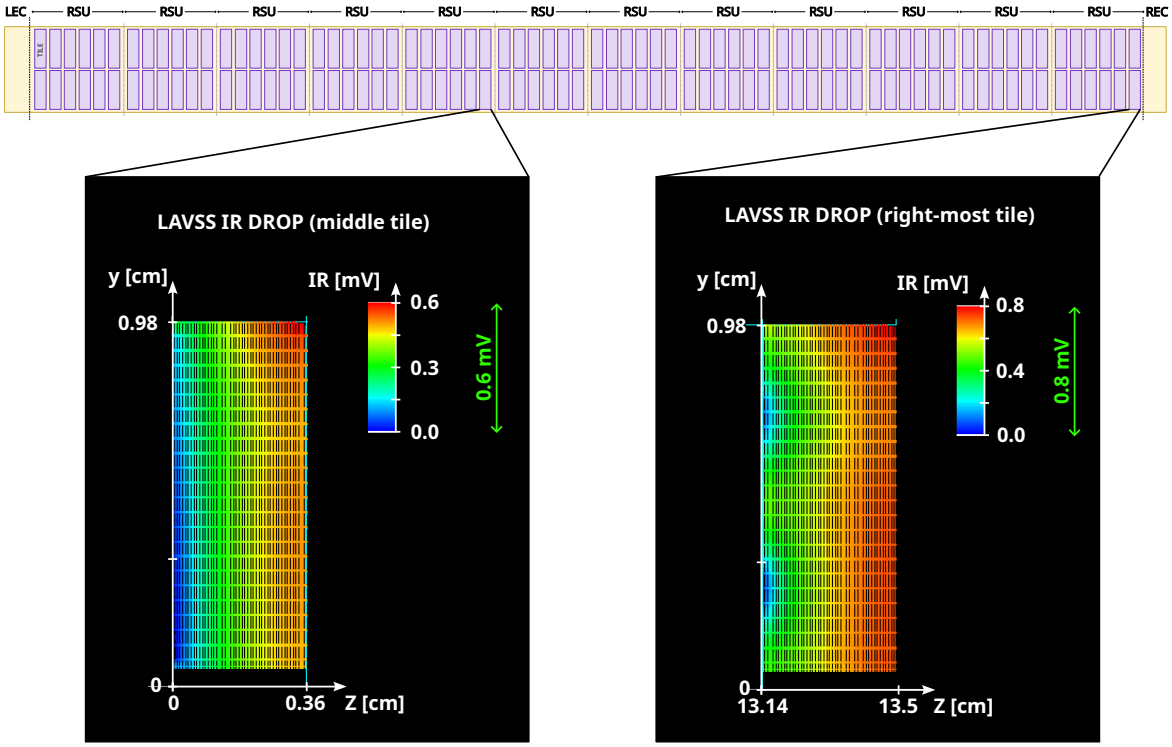

Figure 4. Worst case IR drop simulation result for the local analog grounds for two extreme cases: tile located in the middle of the device (left) and tile next to the endcap (right).

5 Conclusion

The MOSAIX power distribution network successfully addresses the challenges of wafer-scale chip integration for the ALICE ITS3 upgrade. By combining a robust global grid, segmented local grids, and fault-tolerant design features, MOSAIX achieves uniform local power distribution with minimal IR drops and maximizes the probability of high yield. The design is resilient to defects, ensuring reliable operation even in the presence of shorts, making it a viable solution for the ALICE ITS3 detector.

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