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TRANSPONDER FOR REMOTE READOUT AND CONTROL OF EXPERIMENTAL APPARATUS

ABSTRACT

A parallel-to-serial technique permits the position of a remote electromechanical device such as a collimator jaw, with either potentiometer or revolution-counter readout, to be transmitted to the control room on a single coaxial cable. The same cable is used to change the position of the device. Position and control information are transmitted as a 1 MHz pulse train of variable length. Specific "control" and "device" modules which we have constructed and tested at SLAC are described in detail. They provide numeric, analog and computer readout of the device in the control room and cost about $350. per device.

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1. INTRODUCTION

Experiments at particle accelerators usually involve the remote readout and control of several items of electromechanical equipment such as collimators, movable scintillation counters, etc. The position-measuring device may be a linear potentiometer or, where greater resolution or stability are required, a revolution counter or other digital device. The problems of controlling the device position and transmitting, displaying, and presenting the position information to a computer for data-logging are traditionally handled in an ad hoc manner, leading to a profusion of hardware systems. Our device represents an attempt to solve these problems once and for all for a wide range of applications, drawing heavily on the medium-scale-integration (MSI) technology which has been developed for the counter and digital panel meter trade. Since the transponder is rather complicated, we will discuss it at three levels: What it does (Section 2); the general principles of operation (Section 3); and a detailed discussion of a specific circuit which we have designed to handle a variety of applications (Section 4).

2. GENERAL DESCRIPTION

One printed circuit (PC) module is required at the remote "device" and another at the "control" station, for each degree of freedom to be controlled (for example, each jaw of a slit). The two modules are very similar in a fundamental sense, although the exact implementation at each end is different. For instance, the "device" end does not usually require the digital display or computer interface. The two modules are connected by a single coaxial cable, eliminating the cost of multi-conductor cables over large distances. Data are swapped between the device and the control, encoded as the number of pulses in 1 MHz train. First a number is sent from the device to the control representing the position of the device and the status of its limit switches (if any). Then a number is sent from the control to the device representing a command for no motion, up motion, or down motion, plus a code for motor speed. This conversation goes on continuously.

At the control end, the information is latched, displayed on a numeric readout, and made available to a computer data bus, so that the position information from the most recent exchange of information is continuously available for data-logging. The latch eliminates the need for synchronizing the computer readin with the transponder conversation. At the device end, the numerical information is converted to a voltage level and stored in an "analog latch" to set the motor speed.

The circuit includes protection against momentary power failure; restoration of power after power failure at either end will not cause the device to move inadvertently. Similarly, the device will not move if the signal line is broken. If power is restored after a power failure, data transmission will automatically resume provided there is no other problem.

Each pair of modules costs about $350, including everything but some simple unregulated power supplies which can be shared by many modules. As described here, the system is not multiplexed; a pair of modules is required for each device. One can undoubtedly design a multiplexed scheme (such as a scanning DVM) to handle any large array of identical devices at a lower cost per device. On the other hand, the present scheme is an inexpensive way of performing all the indicated functions (analog or digital readout, complete ground isolation, numeric display, motor speed control, computer interfacing) for any single device, and has the great virtue of being standard; control and device modules are all identical even if the devices being controlled differ. It will represent the best solution whenever an experiment uses a variety of devices each differing slightly from the others. The possibility of multiplexing the control module to several device modules, and the savings that might be realized, are discussed in Section 6.

3. PRINCIPLE OF OPERATION

Very briefly, a 1 MHz clock at the device is counted locally. After each count, the counter is compared with the status of the digital device being read out (or with a voltage level for analog readout). When they are equal the clock is stopped. Thus the information is encoded as

the number of pulses in a train, and can be reconstructed by a similar counter at the receiving end. This is perhaps the simplest method of paralled-to-serial conversion, and permits analog operations to be carried out easily in parallel with digital ones leading to considerable flexibility. Of course this method is also very time-consuming, but we have assumed that, in controlling the sort of electromechanical device we are discussing, a data-transmission time somewhat shorter than human response times is adequate.

3.1 Main Time Sequence

For a more detailed discussion of the operating cycle we turn to Figure 1, a block diagram of what each module would look like if it were fully implemented, and Figure 2, a timing diagram. The timing elements are all monostables except for a single bistable which defines the module as being in the "receive" (REC) state when set and in the SEND (= $\overline{\text{REC}}$) state when cleared. To be specific, let us assume that our module is located at the device being controlled, whose readout is a four-digit decimal revolution counter employing a one-in-ten code for each digit, and that we are currently in the SEND state. The retriggerable signal detector one-shot stays fired (generating SIG) as long as it is receiving pulses at approximately 1 MHz. It times out about 1.5 microsec after the last pulse. After each pulse increments the local counter, the new counter state is decoded to one-in-ten and passed through the switches of the revolution counter. When an output is received from all four digits in coincidence, a digital comparison circuit produces the "digital equality" (DEQ) signal which shuts off the local clock and fires pulse A. When pulse A times out it fires pulse B which resets the counter. When pulse B times out it complements the REC bistable (so that we are now in REC). Our module is now in a stable "waiting" state. Some time later it begins to receive a 1 MHz pulse train from the 50 ohm cable. The first pulse of this train triggers the signal detector setting SIG. The pulse train is, as before, counted by the counter. When the pulse train ends, SIG times out and fires pulse A. Pulse A in coincidence with REC causes the contents of the counter to be latched; then pulse B clears the counter as before. (Usually there is no

need for a digital latch at the device end so it can be omitted.) Timeout of B causes the bistable to complement (putting us back in SEND) and the REC to SEND transition fires pulse C. Pulse C determines a waiting period after which the 1 MHz clock is started, completing the cycle.

The REC and SEND states are very similar. In particular, the SIG detector always triggered by the pulse train and the counter always counts the pulse train whether the pulses are coming from the local or the remote module. Pulse B always resets the counter. In fact, there are only two points of difference between the SEND and REC states:

a) SEND is terminated by digital equality at the local module whereas REC is terminated by the cessation of the 1 MHz pulse train.

b) In REC, pulse A is used to latch or "remember" the transmission just received, whereas in SEND, pulse A is ignored.

3.2 Purpose of Pulse C

If the 1 MHz train were started immediately upon putting the bistable in SEND, the other module might still be in REC because of slight timing differences, so that it might not count the first few pulses. Pulse C, which fires only on the REC to SEND transition of the bistable, is used to introduce a pause before transmitting to get around this problem. We have deliberately introduced timing differences into Figure 2 to show how this feature works.

3.3 Behavior on Missed Code

The digital device being encoded may be of the sort that occasionally misses the code entirely. For instance, it may have break-before-make contacts which happend to be in the open position when the "correct" count is reached. Therefore, the SEND state is terminated either when DEQ is attained or when the counter overflows, Similarly, if an overflow count is received by a module in the REC state, the latch cycle is ignored (that is, the memory keeps the last count received properly) and an OVF bit is set to indicate that the data are not fresh. This bit is cleared by the next latch operation (that is, as soon as the data are replaced).

3.4 Transmission of Analog Data

To explain the analog mode of operation, let us now assume that the position-measuring device is a linear potentiometer producing a DC voltage which slowly changes as the device is moved. The module is equipped with a current integrator which generates a slowly rising ramp while SIG is asserted; this is the analog of the digital counter. The ramp is compared with the input voltage by a comparator. The STOP level which turns off the 1 MHz clock may be caused by analog equality (AEQ) between the ramp and the signal instead of by DEQ. Thus the analog signal is converted to digital (essentially by the "single-ramp" technique) and the resulting pulse train is sent along the cable. The ramp generator is reset by pulse B just as the counter is. The analogy between the analog and digital halves of the circuit is completed by the presence of an "analog latch", a condenser on which the final value attained by the ramp during the REC phase can be stored until the next transmission, before the ramp is reset to zero. Some applications of this uninterrupted analog version of the received signal (analogous to the stored digital version of the signal) will be given later.

The transponder thus transmits analog data in digital form, reconstituting it at the receiving end. Moreover, the 1 MHz pulse train may be transformer-coupled, so that the ground sides of the two modules need not be connected. These features may facilitate analog readout in high-noise ambients.

3.5 Mixed Analog and Digital Data

Finally, we discuss a technique for transmitting mixed analog and digital information. Assume, for instance, that the device has the linear potentiometer but also has two limit switches whose states we wish to transmit. The limit switch state is encoded as the most significant portion of the transmitted count. For instance, suppose that the analog part of the information corresponds to 1833 counts. If neither limit is on, we transmit 01833 or 1833 pulses; for the low limit on, we transmit 11833 pulses, and for the high limit, 21833. There are two reasons for this choice of code: a) It is very easy to implement as we shall see and; b) since these "digital"

states are usually off (if they represent limit switches or motor up/down commands) the overhead of transmitting all those extra pulses is not encountered during "normal" readout. The scheme is implemented by resetting the analog ramp (but not the digital counter) whenever the counter is between the 8K and 10K states; if a 1-2-4-8 synchronous counter is used, this can be done simply by shutting off the charging current and clamping the ramp whenever the 8K line is high. In addition, we require AEQ and DEQ before ending the transmission. Figure 3 illustrates the sequence of ramps and pulses involved in sending out the 21833 code. Of course, "DEQ" in this context simply means equality of the 1×10^4 and 2×10^4 outputs of the counter and two TTL levels reflecting the state of the limit switches; the rest of the counter is ignored by the DEQ circuitry.

3.6 Choice of a Clock Frequency

The rather low clock rate of 1 MHz was chosen for two reasons:

a) It allows the wires connecting the module with the digital device to be fairly long, permitting us to pass the decoded levels directly through the device contacts instead of having to condition gates located on the board. This simplifies the DEQ circuitry.

b) It simplifies the design of the analog portion of the circuit by requiring, for instance, only a moderate slew rate of the comparator.

Assuming each device is putting out a maximum train of 100K counts (which is unlikely) the 1 MHz clock rate still yields a complete cycle time of only 0.2 sec.

4. DETAILED DESIGN DISCUSSION

The detailed design discussion refers to a specific pair of modules for which printed circuit cards have been fabricated at SLAC. They were designed to handle variety of control and readout applications. The "device end" module (Figures 4a and 4b) is SLAC PF-036-002-01 and the "control end" (Figures 5 a-d) is PF-036-002-02.

4.1 Specifications

Our discussion refers to a definite set of specifications but the modules will, of course, also be useful in applications which may differ slightly from those specified. For instance, they may be used to actuate a reversible AC motor instead of a DC motor; everything but the motor speed control circuit will still be applicable. A careful reading of section 4 will reveal just how much the existing modules may be "stretched" to cover non-standard applications.

4.1.1 Device

The "device" is assumed to be driven by a reversible electric motor. A motor speed control is incorporated for small permanent-magnet motors, as well as on/off and reversing relay contacts which should cover most other cases. The device may have two limit switches, one at each end of its normal travel; lights at the control end will indicate when these are activated. The position of the device may be given either by a linear potentiometer of about 50KΩ maximum resistance or by a revolution counter with electrical readout, 1-in-10 code for each digit. Four digits may be read out if the limit switches are also used, or five digits if they are not. The readout contacts may be non-shorting although shorting contacts are preferable. Of course, the transponder may be used to read out the position of (or voltage generated by) an arbitrary remote device even if it is not controlled by the transponder; a dummy control-to-device transmission is then used to keep the cycle going.

4.1.2 Control

The control module consists of a single printed circuit board with display Nixies mounted at the front and contact fingers at the rear for miscellaneous connections and the computer bus. This bus is relatively low-speed and may be physically long; control modules may be distributed about the control room as human engineering dictates. Various switch and display options are brought out to the rear contact fingers and the corresponding switches etc. may be arranged as desired on the front panel.

4.2 Module At Device

4.2.1 Supply Regulators (Figure 4b)

Since several devices may be clustered near a given location it seems reasonable to use common power supplies. However, it would be most undesirable to have the calibration of each module depend upon an external supply since the calibration would then change if the supply were ever changed. Therefore at least one accurate voltage reference on each board is needed and in fact it is convenient to regulate all supplies on-board allowing the use of unregulated external supplies and the neglect of voltage drops in the supply wiring. The +5 and +15 volt regulators track the -15 volt reference so only the latter need be adjusted. At the present writing, we have provided room for the +5 volt pass element (the MJE 521) on board, but (for insurance) brought out the necessary connections to contact fingers in case the power dissipation (a few watts) heats the board too much.

4.2.2 Digital Circuits (Figure 4a)

The digital circuits should be self explanatory in conjunction with the description of section 3; however, explicit definitions of the logic conditions for some of the levels and transitions may help. The CLAMP level, affecting the condenser in the analog ramp generator, is asserted whenever there is (no SIG and no pulse A) or when the 8×10^3 line is high. The latter provision allows for mixed analog and digital information as discussed in sub section 3.5. The former condition removes the clamp whenever there is signal (permitting the ramp to rise whenever the digital counter is counting) and holds off the clamp during pulse A in case one wishes to latch the final value attained by the ramp before resetting it. The output filter of open-collector IC23 removes a transient which would tend to assert CLAMP briefly after SIG times out and before Pulse A is asserted.

The CHARGE level to the analog section is asserted whenever there is a SIG level and no 8×10^3 level.

The LATCH level is asserted during pulse A when the module is in the REC state, unless the digital counter has overflowed (indicated by a carry level from the final decade), which would indicate that no code match was reached at the sending end and therefore, that the last valid transmission should be retained.

The 1 MHz clock consists of IC's 6, set to 100 nsec, and 7, set to 900 nsec connected in a feedback loop. It is started on the condition (no pulse A and no pulse B and no RECEIVE and no pulse C); pulse C, it will be recalled, is the "wait before sending" time which allows the other module to prepare to receive. The clock is stopped by a STOP level asserted when AEQ and DEQ are attained, or when the digital counter overflows (which means the desired code has been "overshot" for some reason). Since the 74121 one-shot IC7 has better time stability than the 74122 one-shot IC6 it might seem desirable to extend the 900 nsec period at the expense of the 100 nsec. There is a pitfall in this: The synchronous counter must receive a clock pulse wide enough to ensure carry propagation through all decades while the clock is still high. That is, the counter is synchronous only in the sense that the four outputs from each chip change state simultaneously; the minimum clock width specified in the data sheets for a single chip will not work if it is applied simultaneously to several chips cascaded. In our circuit the minimum length necessary for five decades appears to be a little over 50 nsec. The stability of the 1 MHz clock is of no importance anyway if digital information is being encoded; it does matter in the analog mode, but a number of factors conspire to limit the stability to a few parts per thousand, and a rather complete redesign might be necessary to improve it much. Digital encoders should be used in any applications requiring very high stability.

4.2.3 Analog Circuits (Figure 4b)

The heart of the analog section is an integrator IC29 generating a ramp which is continually compared to the input voltage by IC33. The comparator output is not used by the digital section, however, unless the module is connected in the analog mode and is in the SEND state, in which case the level AEQ (Analog Equality), asserted when the ramp exceeds the input voltage, stops

the 1 MHz clock. The nominal integrator current is 50 μamp (15 volts/300K ohm) which together with an integrating condenser of nominally .05 microfarad causes the ramp to rise at 1 mV per microsecond.

The integrating condenser C11 is one of the few critical components. It is shorted out for about 200 microsec (roughly the sum of the B and C pulses) by the FET Q6, before the start of each transmit or receive cycle. The final levels attained by the alternating ramps associated with the transmit and receive cycles, which depend on the data being exchanged, may be quite different. Now condensers suffer from "dielectric soakage", an effect which may cause the rate of rise of a ramp to depend slightly upon the past electrical history of the condenser (for instance, upon the amplitude of the previous ramp). If a charged condenser is shorted for a while, and the circuit then opened, a small voltage will gradually reappear across the condenser, due to non-equilibrium charge distributions persisting in the dielectric while the condenser is shorted. In our circuit one will observe that the time required for the ramp to reach a given level during the SEND cycle, which is reflected in the encoded value of the input voltage, depends upon the size of the previous ramp (which reflects the data, usually the motor speed setting, being set the other way). Ceramic condensers are known to be very bad in this respect. We have found that silver-mica condensers appear to be better than mylar dielectric condensers (Electrocube). With the 47,000 picofarad silver-mica condenser specified for C11 the dependence of the encoded analog output on the height of the previous ramp is only about 0.1% in the worst case and this may be due to other effects.

The analog latch is activated by a 100 microsecond pulse (pulse A gated with REC) after the ramp has reached its maximum value (that is, just after the pulse train has dropped out in the REC state); after this the ramp is reset. During latch time a 1 microfarad condenser C12 is connected to the ramp generator through a buffer amplifier IC30 and a junction FET. The FET is cut off at other times by holding its gate negative; diode D3 prevents IC30 from also driving the source negative which would turn the FET on at an inappropriate time. The 10 ohm resistor in series with C12 limits the charging current and thus reduces high-frequency transients in IC30 when

the FET is turned on, allowing it to settle faster. Non-linearity in the FET is canceled by a feedback loop involving voltage follower IC31, which also isolates the storage condenser from the external load so that moderate currents (a few mA) may be drawn without discharging C12. The amount this condenser can be charged or discharged during any single latch period is limited, so if the transmitted signal changes very rapidly the latched signal may take a few steps to catch up; this raises no problems in the applications we have in mind.

A 748 op amp is used as a comparator instead of the more usual 710, because:

a) The 710 uses inconvenient supply voltages

b) The 748 slew rate is adequate (we have measured a transition time of about 1 μsec from V^- to V^+ at the output of the comparator)

c) The low input bias current (80 na typ.) of the 748 makes it possible to use a fairly high-resistance linear potentiometer without requiring an additional buffer amplifier.

We occasionally observe high frequency oscillation of the 748 output near V^-. This does not pass through the level converter Q7 and does not seem to cause any problems.

4.2.4 External Analog Components

A fundamental limitation of our technique is that zero or negative numbers cannot be transmitted; therefore the device being read, be it analog or digital, must be so set up that a state which would require transmission of 0 cannot be reached. Moreover, the electrical offset permitted by the OFFSET adjustment is always positive.

It will be simplest to discuss the choice of external components in terms of a concrete problem. Let us assume the signal source is a 30K linear

pot having a scale marked from 0" to 4" with 0" corresponding to electrical zero. Relabel this pot from 1" to 5"; using the OFFSET and SLOPE adjustments it will now be possible to calibrate the transponder so that the number displayed in the control room will correspond exactly to this new scale, reading 5.000 at 5" etc.

The OFFSET and SLOPE adjustment components are chosen as follows: Since the nominal rate of rise of the ramp is 1 mV per microsecond and the nominal clock frequency is 1 MHz, the nominal calibration is 1 count per millivolt. (We will plan to set the -15 volt reference and the 1 MHz clock to their exact values and then use the SLOPE adjustment to compensate for the fact that the values of C11 and R20 are slightly off nominal.) Thus the 30K linear pot, representing 4" of travel, should drop 4 volts; a current of 0.1333 mA is indicated. This current is supplied by the SLOPE adjustment (fixed plus variable parts) connected across 15 volts, fixing this at about 113K ohms; a reasonable arrangement would be a 100K fixed and a 25K variable 10-turn trimmer for the SLOPE adjustment. The OFFSET resistor should have about a 1 volt drop (for 0.1333 mA) to correspond to the "missing" "1". This leads to 7.5K for the offset resistor; use a 10K 10-turn trimmer. Final adjustment of the OFFSET and SLOPE pots is discussed in Section 7.

4.2.5 Protection Against Inadvertent Motion

In the course of a lengthy experiment it is to be expected that AC power will fail and be restored from time to time. It would be extremely annoying if, every time this happended, inadvertent motions of the various electromechanical devices connected with the experiment were to result. Accordingly a relay RL1, in series with the coil of the "device motion" relay, is provided. In addition to the 1 MHz pulse train, a DC level is transmitted along the connecting cable to actuate RL1. This level is derived directly from the up/down motion switch in the control module; it does not depend upon the state of any mono- or bistables in the control module, but only on the switch state. Its rise and fall are slow so that the start or end of the level will not be counted as a pulse. RL1 also ensures that the device will not move if the cable is broken, no matter what the state of the IC's

in the device module may happen to be. This approach is simpler and safer than trying to ensure that all the critical IC's will come back on in a standard state after power failure and restoration.

Relay driver Q25 is arranged so that RL1 must be closed and either the 1×10^4 or 2×10^4 lines must be latched high to actuate the master relay. This goes far towards ensuring that the modules are swapping valid data. RL1 is a relay rather than a transistor to permit isolating the device and control modules.

4.2.6 Mode Selection

The module can be used three differenct ways: a) readout of analog device plus two limit switches; b) readout of 4-digit decimal device plus two limit switches; c) readout of 5-digit decimal device. Mixed analog and limit-switch data are transmitted as described in Section 3.5, the LO limit being encoded as 1×10^4 and the HI limit as 2×10^4. The mode is determined by a 14-pin patch plug "IC28" wired according to the following Table:

Pin #	Analog Limit Switches	4 Digit Limit Switches	5 Digit
1	7 (330)	7 (330)	14 (330)
2	"	14 (1K)	14 (1K)
3	"	"	"
4	"	"	"
5	"	"	"
6	14 (1K)	7	7
9	8	8	14 (1K)
11	10	10	14 (1K)

An entry "7" means connect directly to pin 7. An entry 7 (330) means connect to pin 7 through 330 ohms.

Wiring of Mode Selection Plug "IC28"

In analog mode, IC's 10-14 may be left out.

4.2.7 Motor Speed Control

The voltage transmitted from the control to the device module and latched there can be used to control the speed of the motor moving the device. Small DC permanent-magnet (PM) motors, typically drawing 0.5 ampere at 24 volts are suitable for many devices. Variable speed can be very useful if, for instance, a device with a travel of a few inches is to be positioned to a few thousandths. Now a PM motor connected to a current source will deliver constant torque, so that the speed will very with the friction in the device. At low current, performance will be very erratic, and the device will be difficult to set especially when the motor cannot be heard. The use of a voltage source instead of a current source will improve matters somewhat; in this case one must build in current limiting or the motor will burn out if stalled. However, in the case of a PM motor it is not difficult to regulate the speed itself, yielding smooth operation over a wide range of motor speeds, and such a regulator is included on the board.

The principle is this: If the EMF applied to the armature is removed during a brief "SAMPLE" period, the motor will coast due to inertia and a back EMF, proportional to the coasting speed, will remain across the winding. This EMF is compared to a set value and the difference used to determine the duration of the next "POWER" pulse applied to the motor. Thus SAMPLE periods, of fixed 5 millisec duration, alternate with POWER periods during which full DC power is applied; the POWER period may range from much less than 5 millisec (approaching 0% duty cycle when the load is light) to much more (approaching 100%). If the motor suddenly encounters a large resistance, full power will be applied even when the set speed is very low; thus the motor can crawl its way through a variable frictional load.

At the heart of the circuit is a timing condenser C17 whose negative charge at the end of each SAMPLE period determines the duration of the subsequent POWER period. During the SAMPLE period C17 charges negative an amount determined by the difference between the back EMF (applied to the base of Q23) and the set EMF (base of Q22). For instance, if the back EMF is more negative than the set EMF (motor too slow), more of the current supplied by Q24 to Q22 and Q23 is steered to the collector of Q22 and C17 reaches

a more negative level. Q15, the other current source connected to C17, is cut off during the SAMPLE period, whose duration is determined by the monostable comprised of Q19 and Q20 (Q19 conducting, Q20 off).

When this monostable times out, power is applied to the motor through the Darlington pair Q16, MJE 371, and Q24 is cut off so that the base voltage of Q23 does not affect C17 during the Power pulse. Simultaneously, the constant current source Q15 is turned on, charging C17 positive at a fixed rate; when C17 reaches the positive level determined by the bias resistors R41 and R45, the SAMPLE monostable triggers again, ending the POWER pulse. The duration of this positive-going phase will depend on how negative C17 was at the start, which was determined by the back EMF during the previous SAMPLE period.

There are a few details to the circuit which do not concern the basic principle. Q17 is a level shifter to drive Q24 from the monostable. Q18 isolates the timing condenser C17 from the input impedance of the monostable. Q21 provides a low-impedance path to recharge C16 (which, in conjunction with R43, determines the duration of the SAMPLE period); this allows the SAMPLE monostable to recover quickly, allowing the power pulses to be short compared to the SAMPLE period and thus permitting very low speeds at light motor load. A filter (R50, C18) whose time constant is much less than the 5 millisec sample period reduces large voltage excursions at the base of Q23, resulting from brush noise in the motor. (In this connection, we have also found that a foil condenser, about a microfarad at a few hundred volts, connected across the brushes near the motor, will reduce electronic noise back at the module.) Finally, a potentiometer R49 in conjunction with a fixed resistor R48 sets the scale of the control voltage at the base of Q22 by determining what fraction of the reverse EMF is to be compared with it; this depends upon the characteristics of the motor and the desired maximum speed and should be set so that +5 volts (a good value for the maximum control voltage) applied to Q22 results in the maximum speed desired.

There are many speed regulator circuits in the literature, some of them simpler than this. Most of them use the same principle of observing the reverse EMF to determine the duration or duty cycle of power pulses;

many use an SCR to determine the period during which the motor is connected to a floating AC line. In defense of our somewhat complicated circuit let it be said that it works very smoothly at low speeds (where some controls tend to chatter); can be controlled by a voltage referenced to ground; and uses DC referenced to ground for the motor supply which works out conveniently for the motor-control relays and limit-switch detectors and allows many motors to be powered by the same supply. The motor power (+36 volts in the drawing) need not be regulated or even particularly well filtered; however, it should not dip below +20 volts.

4.3 Module at Control End

The power regulators and analog section are identical to those in the device module. The digital timing section is identical except for circuits connected with the motion control switch, the latch mode, and provisions for indicating when the transponder is stalled and for restarting it automatically after power failure. These features will be discussed below. The control module operates in the mixed analog and digital mode discussed in Section 3.5, the analog portion of the signal representing the motor speed and the digital portion representing a command for no motion, up motion, or down motion. (Throughout this writeup, we take "up" motion as being the direction of increasing numeric output and the "hi" limit as being the corresponding limit switch. It will eliminate a great deal of confusion if all devices are set up consistently in this regard.)

The control module does not have the decode and compare logic found in the device module, since it is always in analog mode; it does, however, have a full digital latch, decoder/driver circuits, and NIXIE display tubes. About $30 can be saved by not loading the decoder/drivers (74141) and NIXIES, making the control module "blind"; we do not advise this, since it makes the device harder to debug and the module less generally useful. A decimal point can be displayed by grounding the appropriate pin of patch plug "IC 35".

4.3.1 "ACTIVE" Bit, Automatic Restart (Figure 5a)

If power is interrupted and restored, it may happen that both modules turn on in their stable "REC" state and the conversation does not

start. The output of an ACTIVE monostable, normally retriggered by (SIG and REC) is wired to the computer bus; the absence of this bit will indicate to the programmer that the conversation has stopped (or, that the particular device being addressed is not connected to the bus at all). A light emitting diode (LED) connected to the same monostable will light when the transponder is stalled. When the transponder is stalled, a unijunction oscillator (Q17) tries to restart it every half second or so by forcing the REC flip-flop into SEND which causes a pulse train to go out; as soon as power is restored at the device, the device module will respond and the conversation will resume. Because the condition for ACTIVE is (REC and SIG), the ACTIVE level will remain off while the control module tries to resume communication and will not be asserted until at least one pulse is received from the device.

4.3.2 Up/Down Motion (Figure 5a)

The up/down switch circuitry allows for two pushbuttons or an SPDT neutral-center switch (the latter is shown in the Figure). The switch must set appropriate bits for the digital part of the transmitted data (we use 1×10^4 for up, 2×10^4 for down) and turn on the DC level to actuate RL1 in the device module. The level is applied by a current source Q1 to avoid affecting the termination of the transmission line. C2 in conjunction with the equivalent resistance of R2 and R3 in parallel conditions the rate of change of this level so that it will not be misconstrued as a pulse. Since only two bits need be encoded, the two ex-or circuits (IC 17) and the single 7400 section (IC 15) make up the entire DEQ circuit.

4.3.3 Latch Mode (Figure 5a)

Normally one wishes to retain only the information sent from the other end. However, since the entire latch and display machinery is already available, it is convenient to facilitate debugging by latching and displaying the data being sent by the control module instead of the data being received. The counter may be latched in either the REC or SEND state by grounding an appropriate contact finger. This and the automatic restart circuitry makes it possible to debug the entire control module in a stand-alone fashion, since it will cycle itself and display its own output.

Used in this fashion, the module becomes a stand-alone digital voltmeter with a range of 0 to +8 volts, sampling rate of about twice per second, and stability of a few parts per thousand, interfaced to the computer via CAMAC. It is not seriously suggested that it be used as a DVM but this might be useful as a temporary expedient.

4.3.4 "OLD DATA" Bit (Figure 5a)

Whenever the 10^4 carry output indicates that the counter has overflowed, latching is suppressed and an "OLD DATA" bistable is set. This indicates that the device module has passed through the "correct" code without stopping, as when the digital revolution counter has non-shorting contacts. (Measurements on a typical unit indicate that this happens about 10% of the time when the counter is moving.) The bistable is cleared at the next valid latch cycle. Thus the OLD DATA bit indicates to the programmer that the number does not correspond to the most recent transmission but is probably nearly correct. There is a pitfall in this interpretation: If the device is left in such an "open" position permanently, the number will be nearly correct only as long as power stays on at both ends, since the transponder now has no way of refreshing its information. Therefore the device should always be jogged off this position before leaving it at its final set point; an LED may be connected to the OLD DATA bit as a front-panel warning. Some such problem is, of course, inherent in any encoder with non-shorting contacts, although in a different circuit, only that decade which happened to be open might be affected.

4.3.5 Limit Switch Lights (Figure 5b)

When the transponder is used to transmit limit switch status, 1×10^4 is used for the LO limit and 2×10^4 for the HI limit. NIXIE 5 and IC 34 (its decoder/driver) may be left out. Front-panel LED's may be connected to the appropriate contact fingers to give limit-switch readout. Preferably, the circuitry at the device should be arranged so that power always goes to the limit switches even when the device is not being moved (that is, the motion relay should be on the ground side of the limit switches

as shown in Figure 4b) giving continuous front panel and computer indications when the device is set at a limit. Rectifiers D5 and D6, rated at AC line voltage, permit the limit detectors to operate from DC, pulsed DC, or AC motor power.

4.3.6 Computer Output (Figure 5c)

We envisage a system where up to 64 control modules, scattered throughout the control room as human engineering dictates, are bussed into a single CAMAC module addressable by the computer. All the necessary circuitry is provided although these circuits have not been debugged (nor has the CAMAC module been designed) at this writing. The data bus has six address bit inputs, a WRITE pulse input which causes the addressed module to inhibit latching and place its data on the bus, and 24 data outputs. In addition it has a LATCH output (essentially Pulse A, not inhibited) brought both to the bus and to contact fingers for possible future use in synchronizing an external device with the module; this signal might be useful for multiplexing a single control module to several device modules, but is not used for normal CAMAC readout.

All bus inputs to the module are buffered with Utilogic 380A inverters so as to draw low current; all outputs are open-collector; all inputs and outputs are low-true. The WRITE input and LATCH output are transmitted through wires whose neighbors are grounded to secure a better-defined characteristic impedance and less crosstalk. Physically the bus uses the 3M Scotchflex system with #3365, 40 conductor, 28 AWG stranded flat cable. The impedance in a ground-signal-ground configuration is 95 ohms, capacitance 15 pf/ft, delay 1.4 ns/ft.

The address of each control module is defined by a 14-pin patch plug "IC 47" where each of pins 1 through 6 (according to the code given in Figure 5c) is connected to pin 7 if the corresponding address bit is supposed to be true (low) and to pin 14 otherwise. Pins 8 and 9 should also be connected for normal LATCH inhibition.

During module readout, the sequence of events is as follows: The CAMAC module sets up the six address bits, then after waiting a short settling time asserts the WRITE level. At this point the output of IC 39 will go negative, gating the data onto the bus and inhibiting the digital latch generator IC 6. This avoids changing the data during the read operation. The latch output from IC 6 is only 50 nsec long so the possibility that latching may just be in progress when WRITE is asserted may be taken into account by waiting a short time after WRITE before asserting the CAMAC Q response. (A settling delay would be necessary anyway.)

The data format is clear from Figure 5c. If the 10^4 decade is not used as such, bits 1 and 2 stand for LO limit and HI limit respectively. We repeat that "OLD DATA" means that data were not latched on the last cycle, and may therefore be incorrect; the absence of ACTIVE means that the module is not connected or that hardware or power failure is preventing automatic restart. The top two gates have inputs connected to the contact fingers and may be used for anything; if for instance the control-room limit circuit (Section 5) is used these bits may signify that up and/or down motion is enabled.

5. RELATED CIRCUITS

5.1 Power Supply (Figure 6)

The following table gives the approximate current in mA drawn by each module at each voltage:

Supply	Control Module	Device Module
+15	13	14
+5	800	700
-15	40	40
+170	10	---

This assumes the IC's are all loaded. The power supply shown in Figure 6 will power any mixture of four modules. The supply is completely straightforward and many different components might be substituted for the ones

shown. Though the control module does not require +36 volts and the device module does not require +170 we recommend that both be included in all supplies for interchangeability. The current drawn at +36 volts will depend upon the DC motor and load; the supply will deliver 2 amperes continuously.

5.2 Remote Motion Limit (Figure 7)

The analog latch at the control end might seem superfluous. It was left in because a meter indication of device movement is sometimes convenient; the circuit shown in Figure 7 illustrates another application. It may not be convenient or possible to put limit switches directly at the device being driven (for instance, when it is operating in vacuo or in an explosive atmosphere). The motion limit circuit can be installed in the control room next to the control module; it enables the up/down switch in the control module only when the analog output of the module (corresponding to the device position) is between set limits which are screwdriver adjustable. A pushbutton next to each limit adjustment allows the limit setting to be read on a meter to the same scale as the device position.

When this circuit is used instead of real limit switches, the usual limit bits to the computer will not work. However, the spare bits brough out to the contact fingers of the control module (Fig. 5c) may be connected as indicated to the up/down switch contacts to indicate to the programmer when the device is at limits.

6. MULTIPLEXING THE CONTROL MODULE

It is tempting to consider multiplexing the control module to many device modules, at a potential saving of almost half the cost of a large system. Each device to be controlled would still have its own device module connected to the control room by its own transmission line. Thus each device would still be isolated from the others, and the devices might operate in different modes (analog or digital) since the control module is always the same. In the simplest scheme, one would simply bring all the transmission lines to a single patch panel in the control room where the control module might be plugged into one of them. However, the ones

not in use would not be read out by the computer and in fact, there would be no way the programmer could tell which device was being read unless channel selection were done by a switch whose position was also read.

An N-Channel multiplexed system in which all the data are available to the computer would require a set of N latches each driving bus gates (essentially the circuitry of Figure 5c plus the latch, for each channel). The channel selector which selected the transmission line would also steer the transponder output to a corresponding latch. Each latch could have its own arbitrarily defined address so that, to the computer, the system would be indistinguishable from a non-multiplexed one. Since each device can be moved only when the transponder is connected to it, its latch would always contain the current status of the device.

However, a momentary power failure would destroy the contents of all the latches. The operator would have to be reminded to scan through all the devices (without actually moving them) when this happened, which would be a real nuisance and very apt to be overlooked. Alternatively, all channels might be scanned automatically in this event, while manual channel selection was inhibited. In this case, however, it would be necessary to return control to the channel that was selected prior to failure, since in the course of an experiment the operator might well become accustomed to assuming the multiplexer was wherever he last left it.

We have estimated the cost of multiplexing the control module (primarily the cost of the latch, computer gate and associated circuits) as about $50, to be compared with $185 for the complete control module. Adding an overhead of some $800 for the transmission-line switching, scan logic etc., and considering the conceptual difficulties just discussed, we find the multiplexing scheme unattractive. Ultimately the relatively high cost of the transponder modules may be offset by their reusability for different devices and in different experiments.

7. SETUP AND CALIBRATION

The device module is meant to be mounted in a simple chassis incorporating the necessary relays, connectors etc.; Figure 4b shows a typical arrangement of external components. The choice of values for the position readout potentiometer and the SLOPE and OFFSET adjustments has been discussed in Subsection 4.2.4. Similarly, the control module is mounted in a rack panel which permits viewing the NIXIES, has a toggle switch or pushbuttons for up/down motion control, a single-turn potentiometer for motor speed adjustment (when applicable), and LED indicators for HI LIM, LO LIM, OLD DATA, and STALLED. The mounting should also allow easy access to the computer output bus. A typical arrangement of the external components for the control module is included in Figure 5a.

Module checkout may be greatly facilitated by a test rig which includes a mode selector, digital switches to simulate a revolution counter, pushbuttons to simulate limit switches etc., as well as the necessary power supplies. It should also include a mounting box with convenient front-panel switches and LED displays for the control module. This box may be used both for checking out control modules and later, as a portable control box for setting up the devices to be controlled.

7.1 Control Module

This module is the easier to check out since it has its own display, can latch on send, and can cycle by itself. First install only IC's 53, 54 and 55 and Q15, Q16 and the external MJE 521 - that is, the power-supply regulator components. Adjust -15 volts (R67) and make sure that +15 and +5 are within a few percent of their correct values (they should track -15). Plug in the remaining IC's and transistors (this procedure avoids damaging them in case there was a power supply fault). Set the module to latch on SEND. Adjust the clock frequency to 1 MHz by means of R15. This need not be very accurate; indeed, it can be used as a fine adjustment later on to make the analog latch output of the control module agree with the input voltage of the device module. After this adjustment has been made the NIXIE display should vary approximately between 50 and 5,000 (representing 50 mV to 5 volts) as the front panel MOTOR SPEED pot is turned.

7.2 Device Module

Again, the power supplies should first be checked with only those IC's and transistors plugged in. A functioning control module should be connected to the test rig to aid in checkout (left to itself, the device module will go into the REC state and stay there). The 1 MHz clock should be adjusted with an oscilloscope; its absolute value is not too important unless the modules are meant to be completely interchangeable. The remainder of the checkout procedure essentially consists of exercising all the options available in the test rig.

7.3 Device Setup

There are no setup adjustments if digital readout is used. If analog readout is used, the SLOPE and OFFSET pots (external to the module) must be adjusted to obtain a convenient relationship between the numeric output and the scale markings (for instance, 1" to 5") on the device. First adjust the SLOPE pot so that a movement of exactly 2" (for instance) produces a 2,000 unit change in the readout. Then adjust the OFFSET pot so that the NIXIES read 3,000 when the device is set at 3". It may be convenient to have the linear pot mechanically freed from the device while making these adjustments.

If a DC permanent-magnet motor is used the MOTOR SPEED pot R49 should be set so that a 5 volt input to Q22 (which may be obtained using the motor speed control in the control box) produces the maximum motor speed desired. After this, make sure that a small voltage into Q22 produces a low motor speed; high settings of R49 may cause chatter at low motor speeds with some motors.

ACKNOWLEDGEMENT

The general idea for a device of this sort evolved during a conversation with Dave Gustavson, who also contributed many excellent suggestions during subsequent discussions. Indeed, chatting with Gus about the electronic state of the art was one of the pleasures of working at SLAC. Conversations with Dan Porat and Mike Browne were also very stimulating. Justin Escalera did a workmanlike job on the prototype, and Frank Generali and the SLAC Electronics Shop (particularly Robert Woolston who designed the layouts) on the final PC boards. Finally, I would like to thank Dave Ritson for inviting me to work with Group F during my sabbatical year.

NOTES FOR FIGURES 4 AND 5

1. Resistors:

   5% carbon composition ex. as noted

   1/4 watt ex. as noted

   1% means precision metal film

2. Condensers:

   25 volt disc ceramic ex. as noted

   Polarity signs indicate Sprague 150 D tantalum or equivalent; 47/6 means 47 μf at 6 WVDC, etc.

   SM means silver-mica; value given in Pf

   All condensers equal to 1 μf or greater which are not polarized, are "monolythic" type.

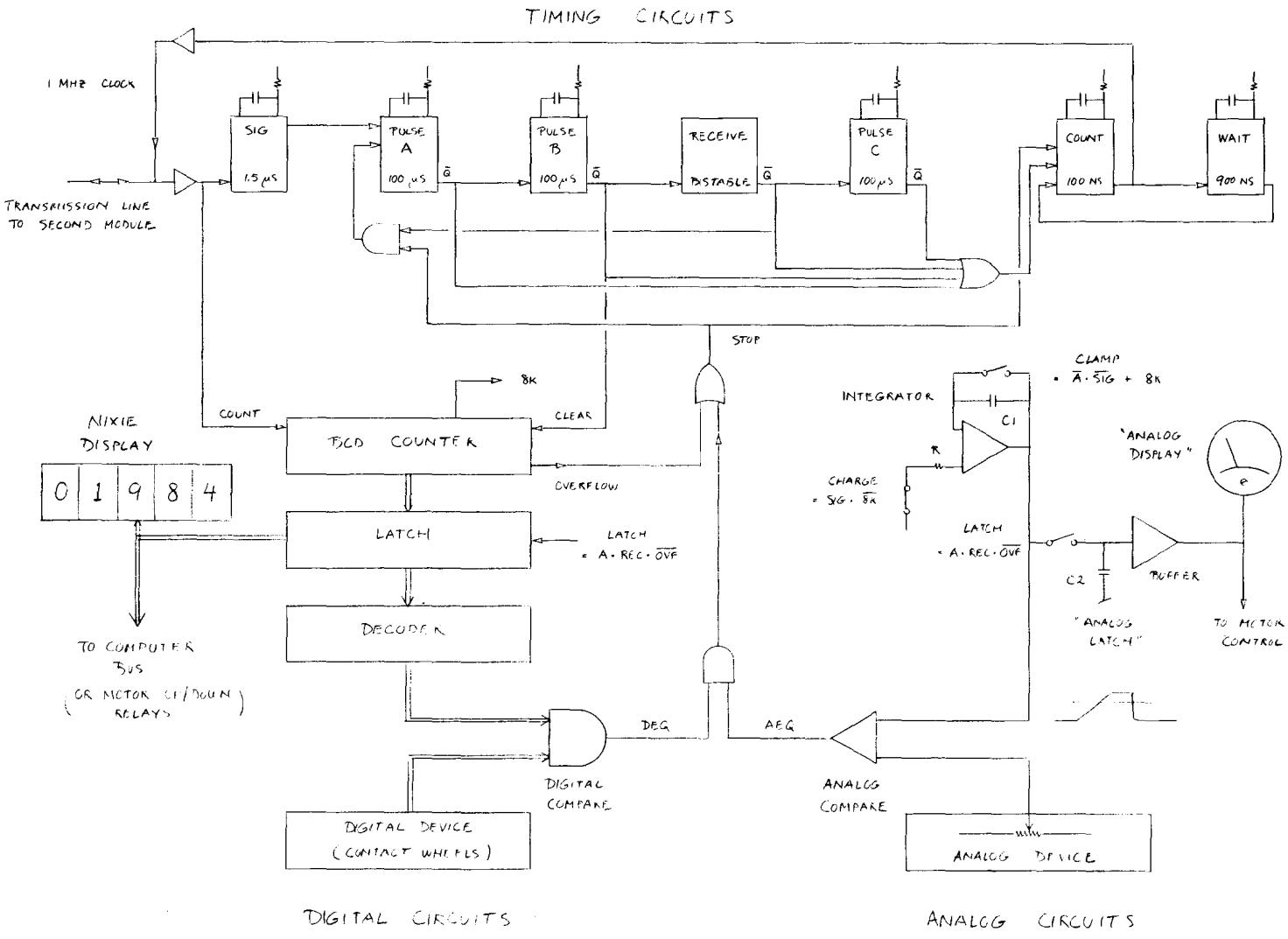
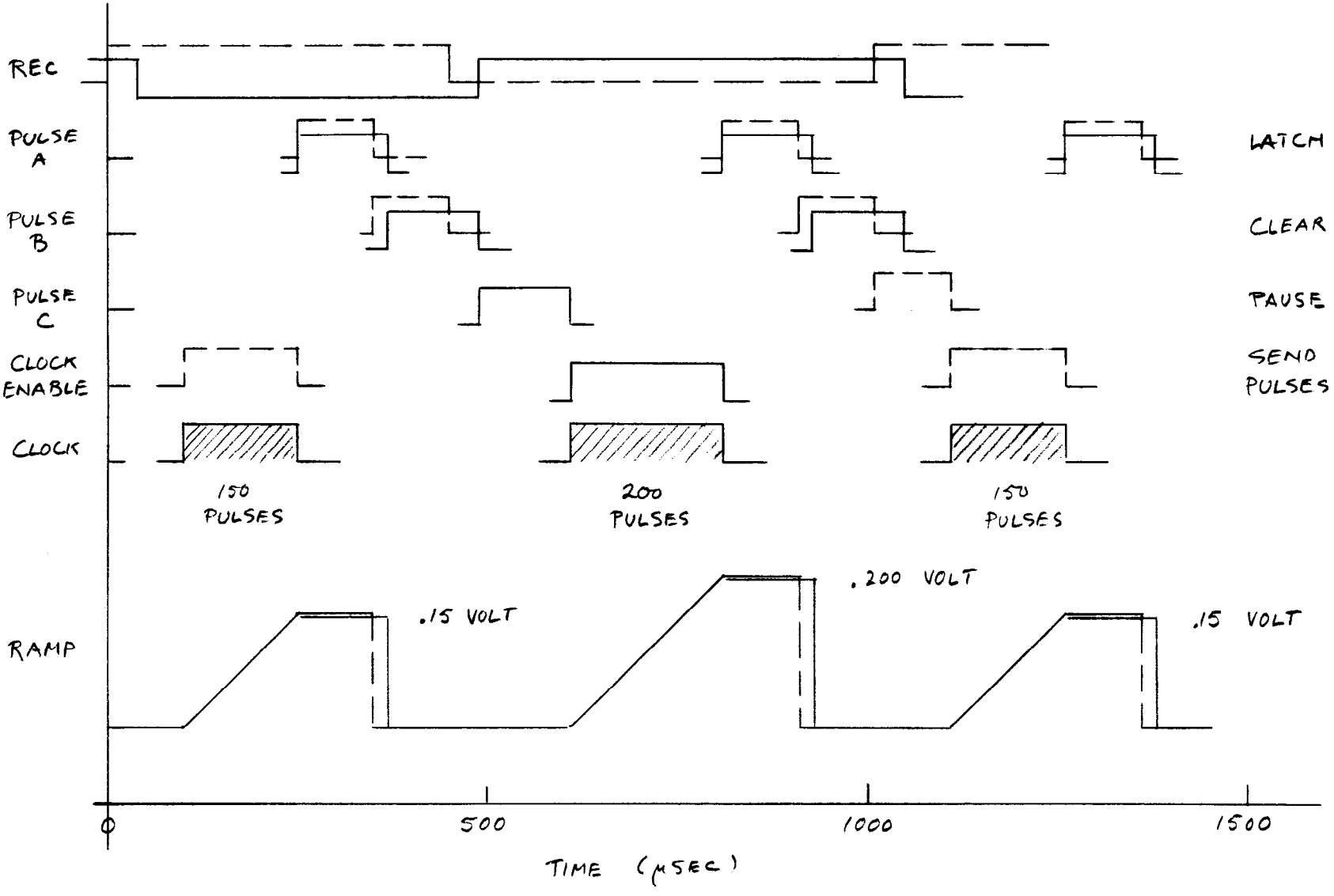


FIGURE 1 - FULLY IMPLEMENTED TRANSPONDER MODULE

BG 8/4/72



— — — = DEVICE SENDING "150" ; A, B, C = 100 μSEC

——— = CONTROL SENDING "200" ; A, B, C = 120 μSEC

CABLE AND IC PROPAGATION TIMES ARE NEGLIGIBLE.

FIGURE 2 : TIMING DIAGRAM

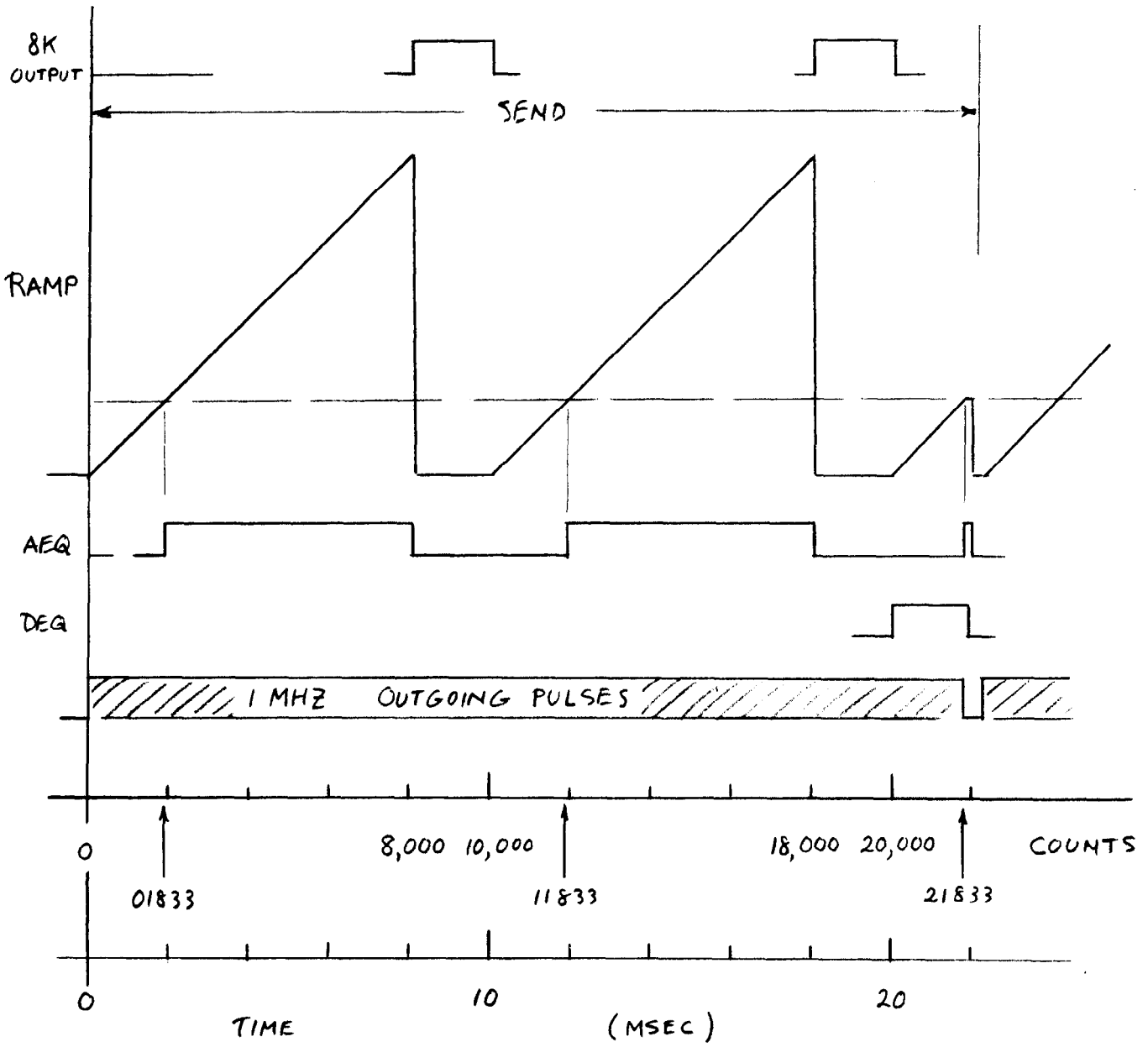


FIGURE 3 : MIXED ANALOG AND DIGITAL DATA TRANSMISSION

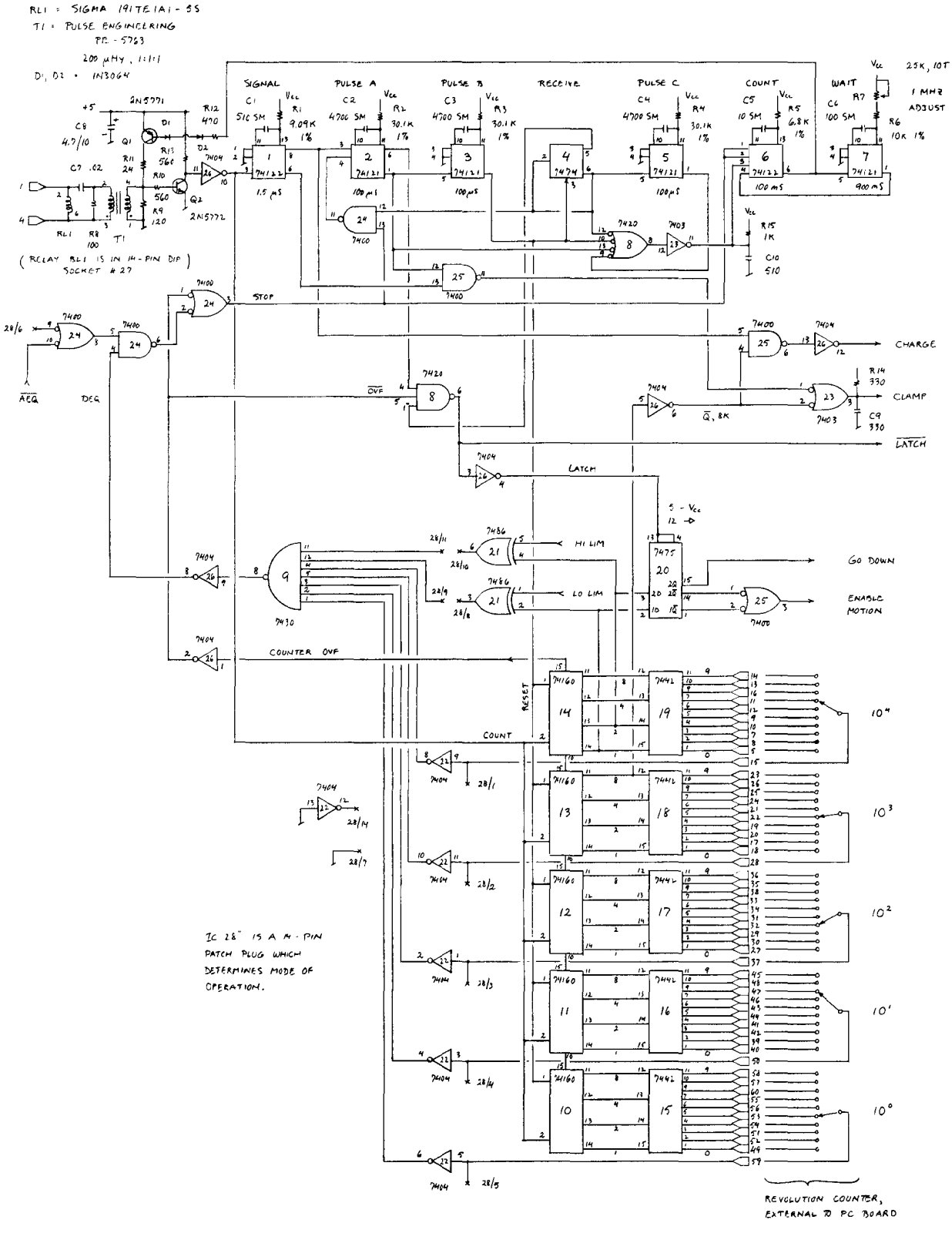


FIGURE 4a: CONTROL TRANSPONDER, SHEET 1 (DIGITAL CIRCUITS AT DEVICE END)

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DG 5/30/72

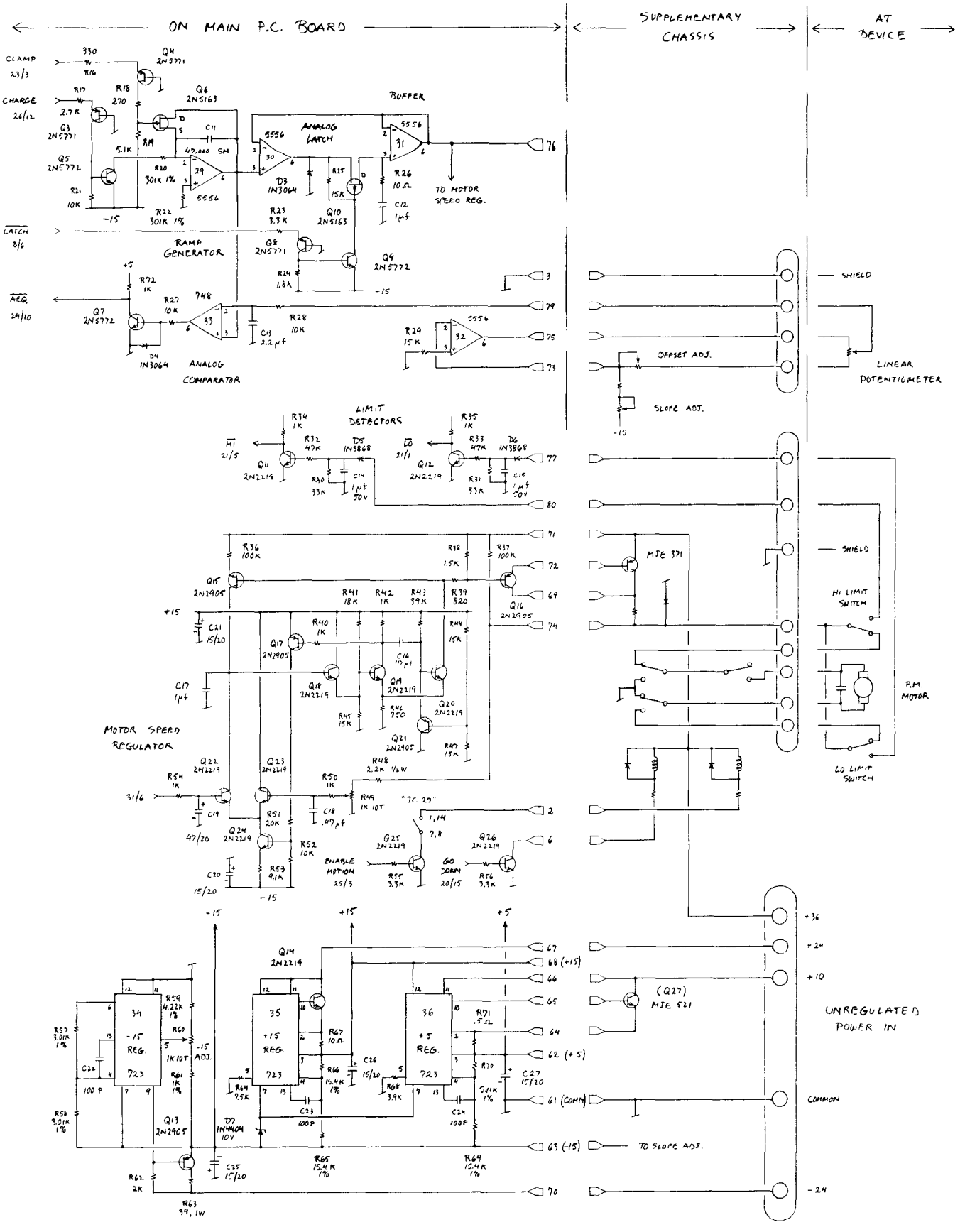

FIGURE 4b: CONTROL TRANSPONDER, SHEET 2: MISC. CIRCUITS AT DEVICE

BG 6/7/72

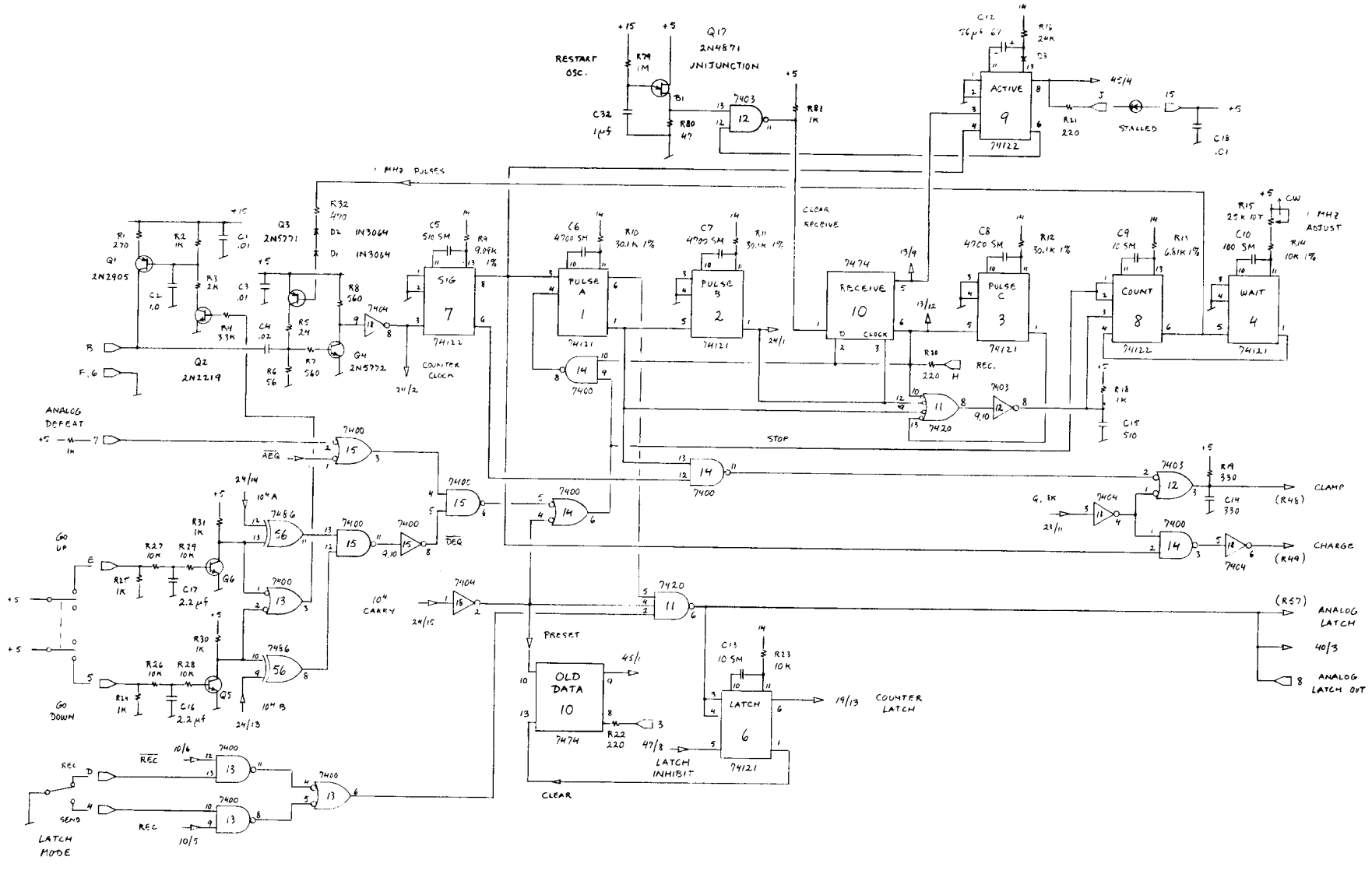

FIGURE 5a : CONTROL TRANSPONDER – CONTROL END

TIMING CIRCUITS

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SHEET 1 OF 4

BG 6/15/72

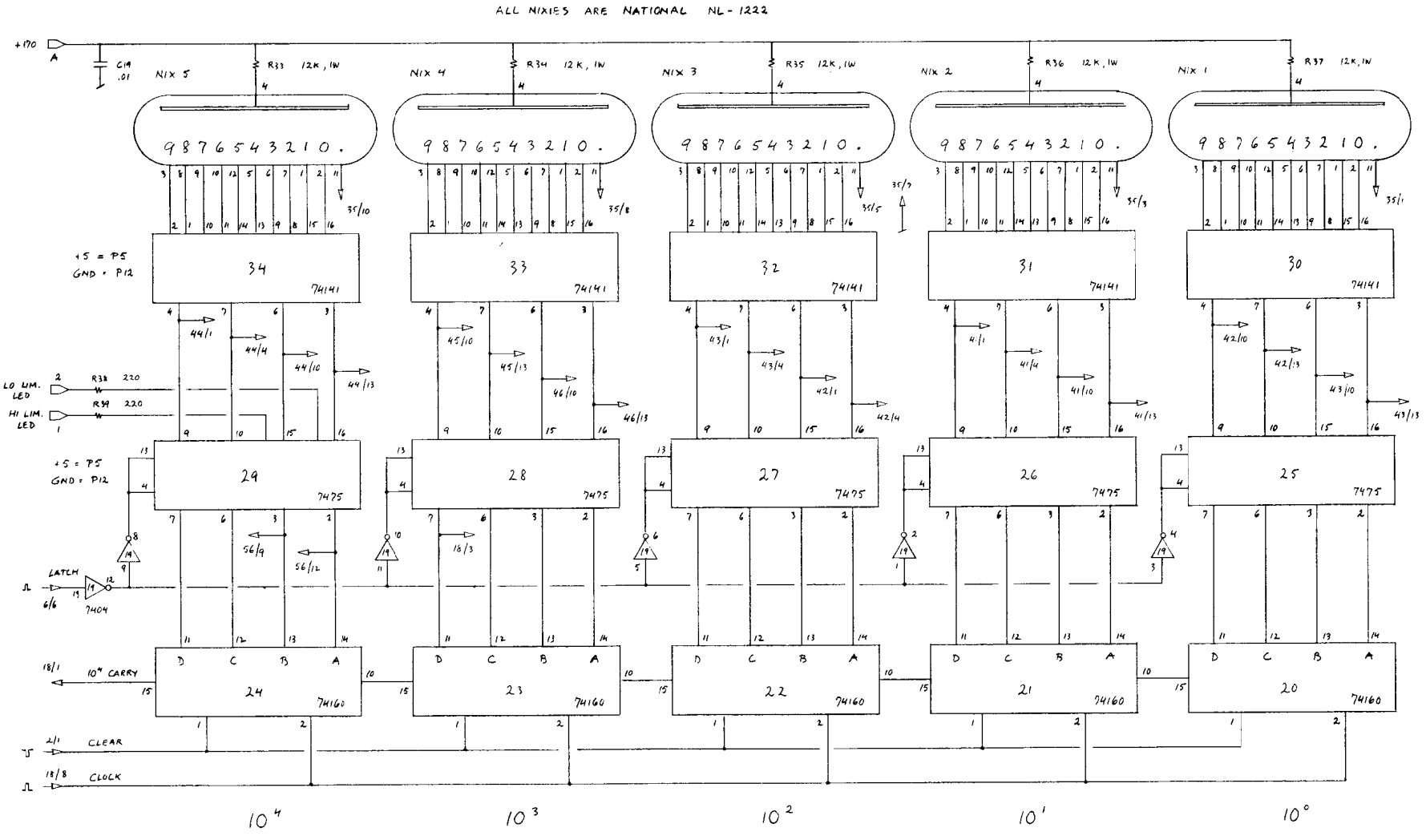

FIGURE 5b: CONTROL TRANSPONDER - CONTROL END

COUNTER, LATCH, DECODERS, DISPLAY

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SHEET 2 OF 4

BG 6/15/72

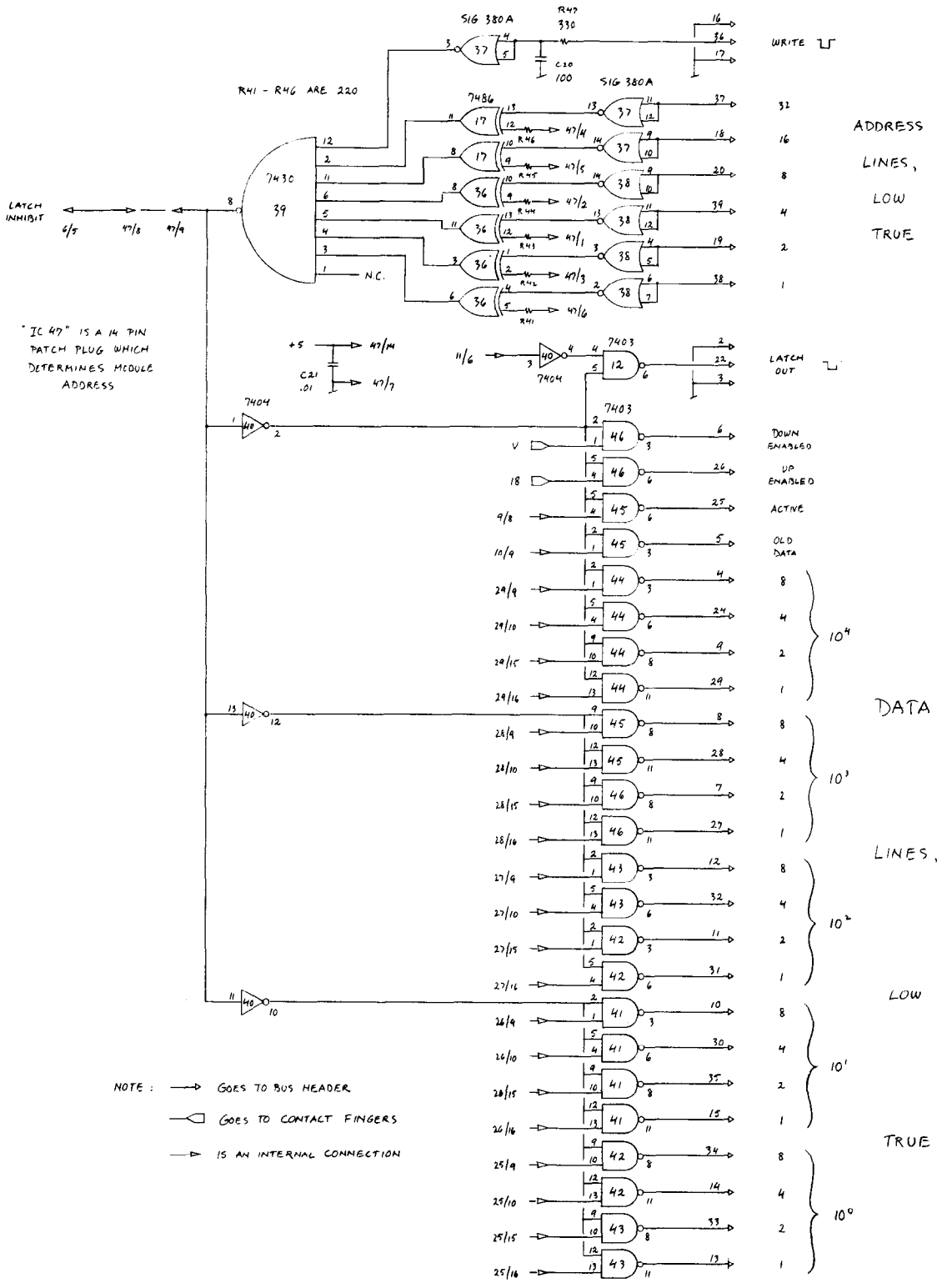

FIGURE 5c : CONTROL TRANSPONDER – CONTROL END

DATA OUTPUT TO COMPUTER

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SHEET 3 OF 4

BG 6/15/72

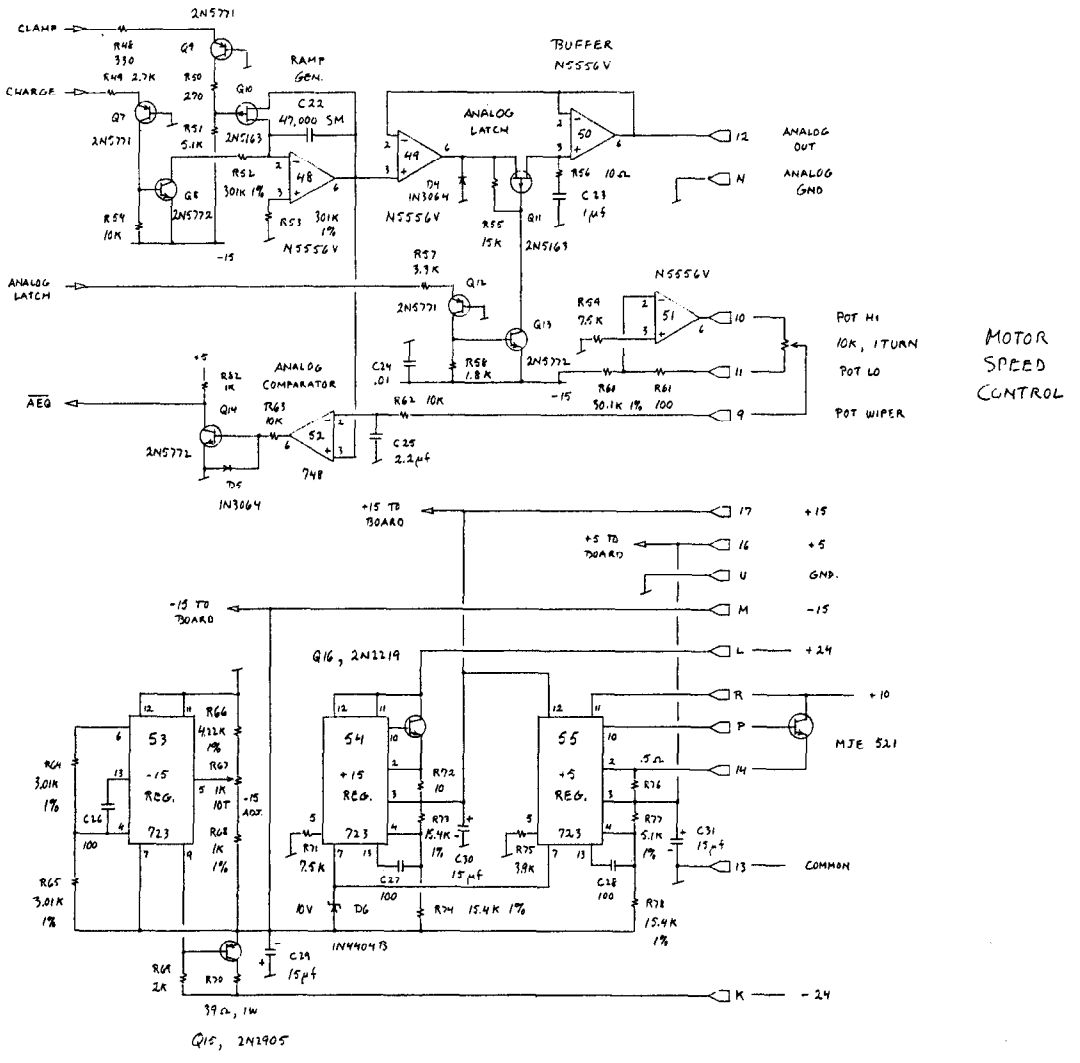

FIGURE 5d : CONTROL TRANSPONDER - CONTROL END

ANALOG CIRCUITS & POWER REGULATORS

SD-036-002-02-R0
SHEET 4 OF 4

BG 6/16/72

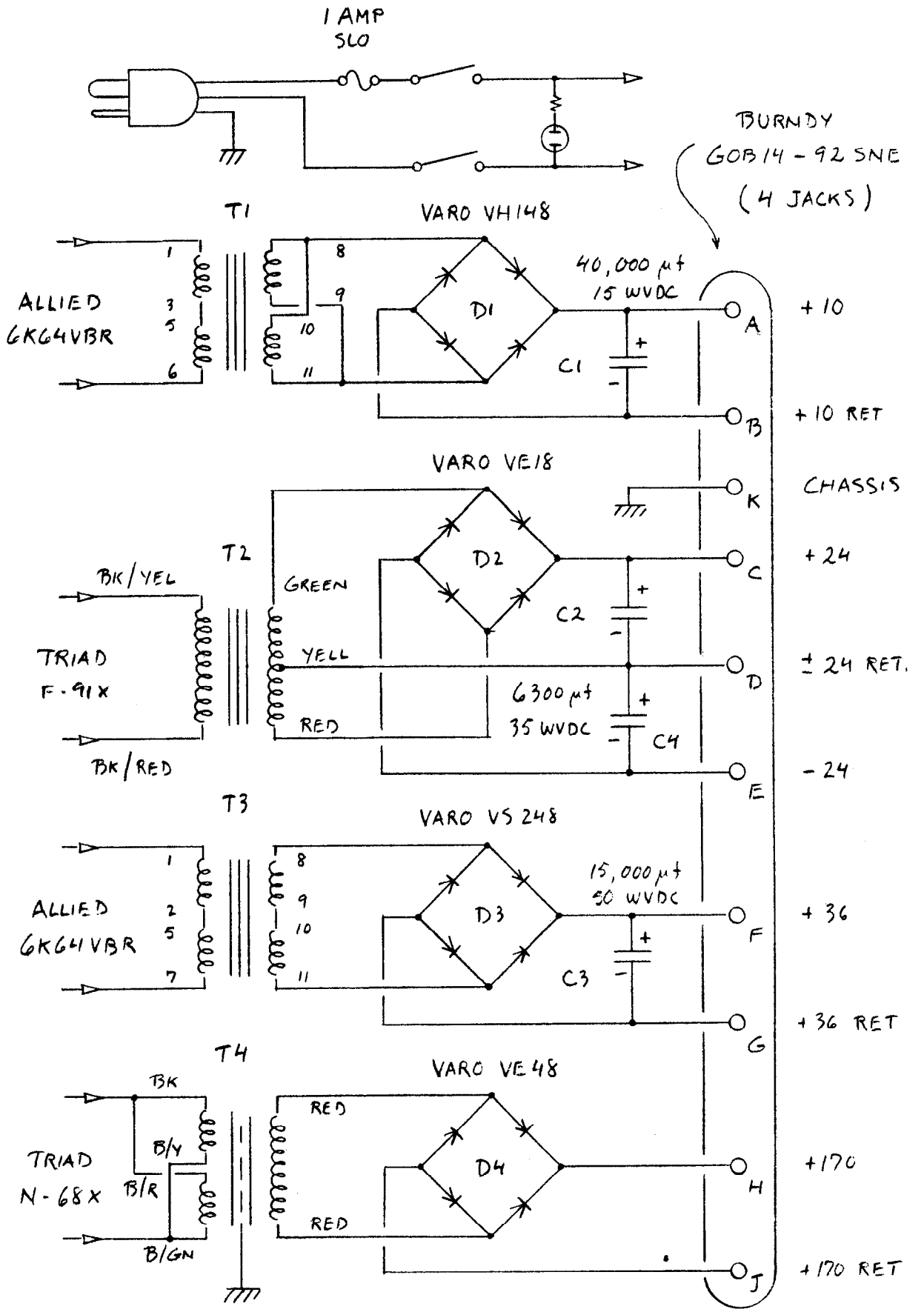

FIGURE 6 POWER SUPPLY

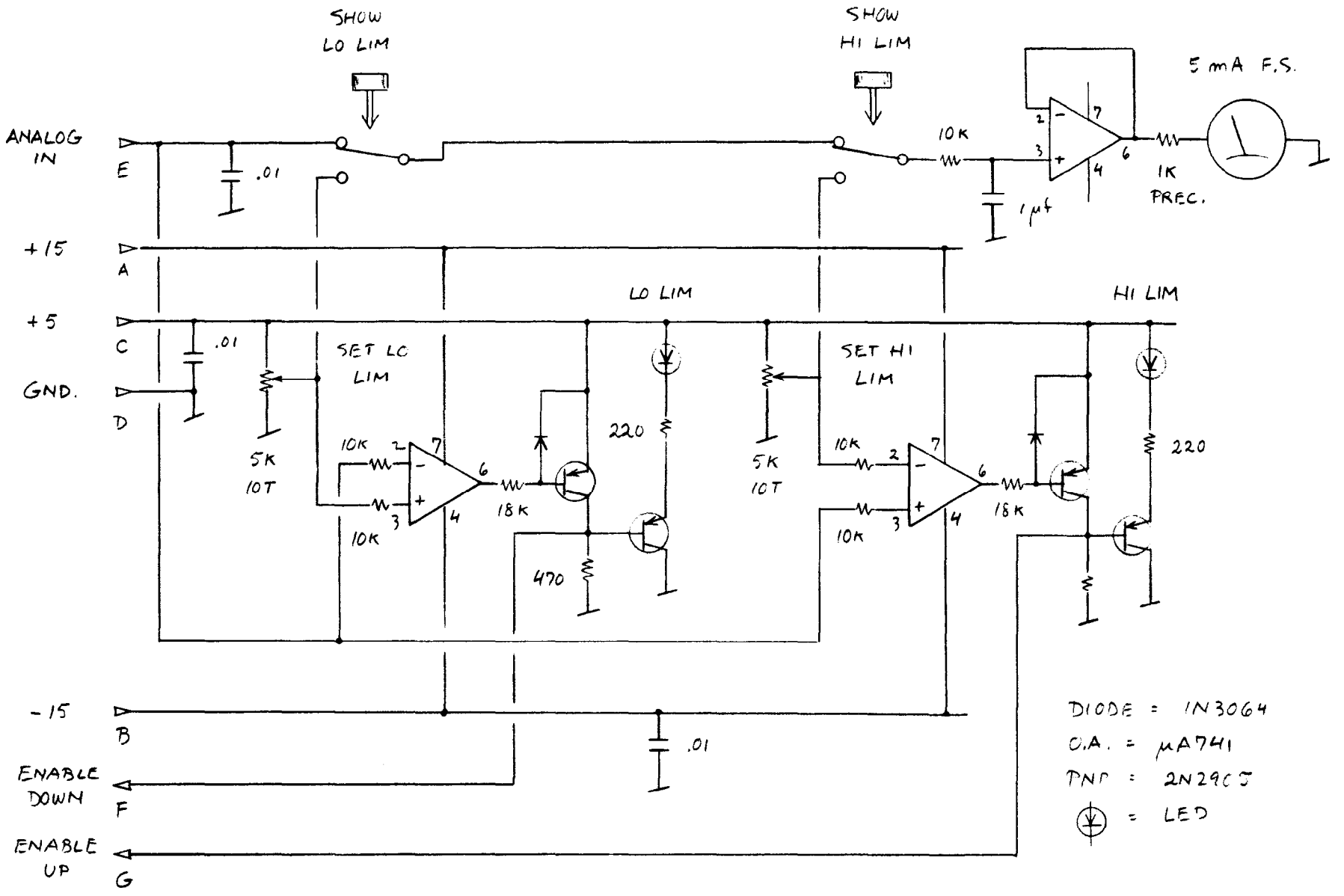

FIGURE 7 : REMOTE MOTION LIMIT CIRCUIT