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Development of low noise pixels and readout architectures for scientific applications in a 180 nm CMOS image sensor process

I. Sedgwick,* S. Benhammadi, N. Guerrini and B. Marsh

UKRI-STFC Rutherford Appleton Laboratory, Harwell Campus, Didcot, Oxfordshire, OX11 0QX, U.K.

E-mail: iain.sedgwick@stfc.ac.uk

Abstract: Noise values of below $1e^-$ for CMOS Image Sensors are now regularly reported for pixels with high conversion gain. This has allowed advances in many fields of imaging. However, there are also scientific applications where other properties such as radiation hardness are required alongside good noise performance. The layout changes required for this however, often lead to a reduction in conversion gain, making achieving the noise performance more challenging. In this paper, we present PRECISE, a test chip designed to apply the techniques of low noise imaging to pixels for other scientific applications, particularly those requiring radiation hardness. The design of the chip will be discussed, and first test results presented on some of the pixel types on the chip.

Keywords: Detectors for UV, visible and IR photons; Photon detectors for UV, visible and IR photons (solid-state)

*Corresponding author.

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Contents

1 Introduction

Progress in the performance of CMOS Image Sensors (CIS) in recent years has been extremely rapid, especially in the area of low noise, where values below $1e^-$ are now commonly reported [1–3], allowing new science and improved performance in many fields.

However, there are also areas of scientific imaging (electron microscopy, x-ray imaging, proton therapy, FEL and synchrotron detectors) where low noise is required alongside other performance parameters such as radiation hardness, high dynamic range, large area or high frame rate. Achieving this performance means taking advantage of these developments in noise performance, and applying them to pixel designs which also have other desirable properties.

With these goals in mind, we undertook the development of a test structure containing the blocks needed to develop sensors for these applications. This chip is called PRECISE, and contains several flavours of 3T and 4T pixels targeting different application areas. Some are optimised for low noise, others implement radiation hardened architectures, and some show high dynamic range performance. The chip also implements a capacitive Programmable Gain Amplifier (PGA), a Sigma-delta ADC and can perform on-chip Correlated Double Sampling (CDS) and averaging of multiple samples. These features are crucial for the integration of the low noise pixels in real systems. The goal of the chip is to demonstrate the performance of the various "building blocks" needed for a larger scientific detector. Suitable blocks can then be combined with the desired pixel type for best performance. The chip also contains a 5 Gbps serialiser, which is not covered here, but will be the topic of a future publication.

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2 Chip overview

The chip was fabricated in a 180 nm CMOS Image Sensor process, and is shown in figure 1 along with a top level diagram of the pixel arrangement. Two flavours of the chip were produced — one containing 4T type pixels with pinned photodiodes [4], and the other containing 3T pixels using standard N-well type diodes. These N-well diodes are now typically out of use in commercial image sensors, but still have use in scientific applications due to their higher radiation tolerance.

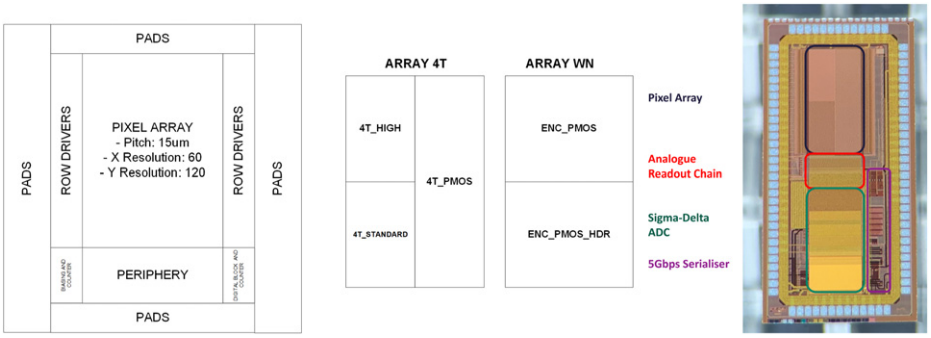

Figure 1. Top level diagram illustrating the contents and layout of the two chips, and a photograph of the fabricated device.

The periphery contains the standard signal chain for this type of sensor of a Programmable Gain Amplifier (PGA), followed by an averaging stage and Sigma-delta ADC. The following sections describe the circuitry of the chip, following the signal path from pixel to periphery.

2.1 Pixels

As stated above, the two fabricated arrays contain several types of pixel:

- 4T_STANDARD: a 4T pixel of standard design and conversion gain.
- 4T_HIGH: a 4T pixel designed by the foundry to have a significantly higher conversion gain than usual.
- 4T_PMOS: a 4T pixel based on 4T_HIGH, but having a PMOS source follower. This was selected because it has been shown to have the potential for lower noise [5].
- ENC_PMOS: an N-well diode type pixel used Enclosed Layout Transistors (ELTs) and gated diode, similar to [6]. The goal of this pixel is improved radiation hardness
- ENC_PMOS_HDR: an N-well diode type pixel as above, but with the addition of an overflow transistor and capacitor for higher dynamic range [7–9].

2.2 Analogue chain

The analogue chain is identical for both the 3T and 4T flavours, and is shown in figure 2. The purpose of the PGA is to reduce the input referred noise of the following stages. Its gain level is

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selectable to allow noise to be traded against full well. When operated with a gain of 1, the PGA is bypassed to avoid introducing unnecessary noise into the measurement.

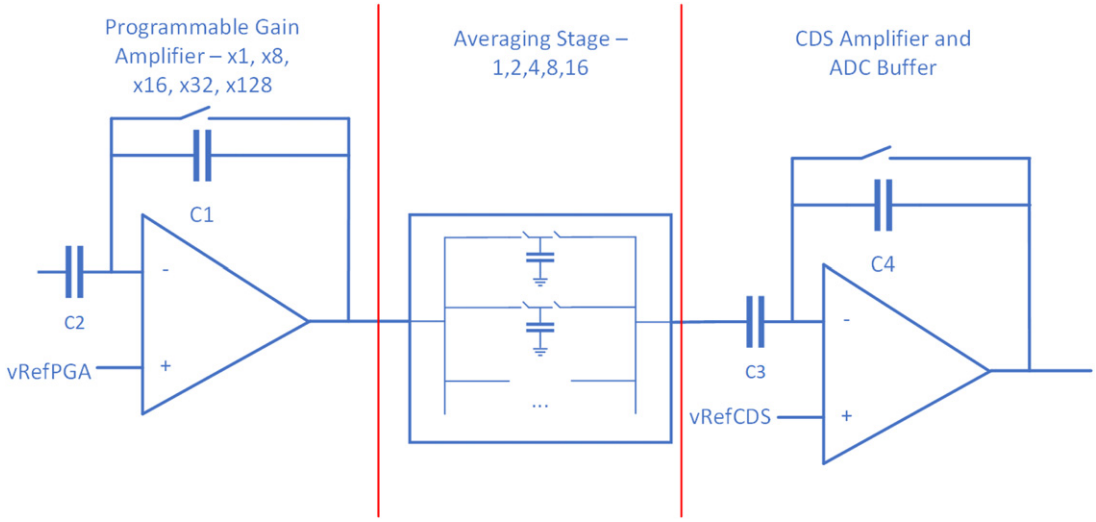

Figure 2. Top level diagram illustrating the contents and layout of the two chips.

The averaging stage allows the reduction of noise coming from the PGA and preceding signal chain by averaging samples. It is designed using the minimum possible number of capacitors following the scheme in [10].

Following the averaging stage is a second amplifier which functions as a buffer for the ADC input stage, and can be used to perform the Correlated Double Sampling (CDS) function in cases where the PGA is bypassed.

2.3 ADC

The output voltage of the analogue chain is passed to an Analogue-to-Digital Converter (ADC). This converts the result of the readout and CDS operation into a digital value. The ADC selected for this application is of the Sigma-delta type, and is operated in a column-parallel manner. Sigma-delta ADCs achieve good noise performance by oversampling their input signal, noise-shaping the result, and using a low pass filter to remove the noise which has now been shifted to high frequencies. This is illustrated in figure 3.

Sigma-delta devices are well suited to the application under consideration here due to their highly digital nature. Variation in the performance of the analogue section is strongly mitigated by the effects of the digital control loop. This makes it very suitable for chips using column-parallel ADCs, where many thousands of devices might be present, and there will be considerable analogue performance variation from ADC to ADC. Similarly, simple designs can be used for the analogue section, reducing design area, since the loop helps compensate for low performance. The point over which most care must be taken is the distribution of the DAC voltages, in order to avoid the risk of cross-talk between ADCs.

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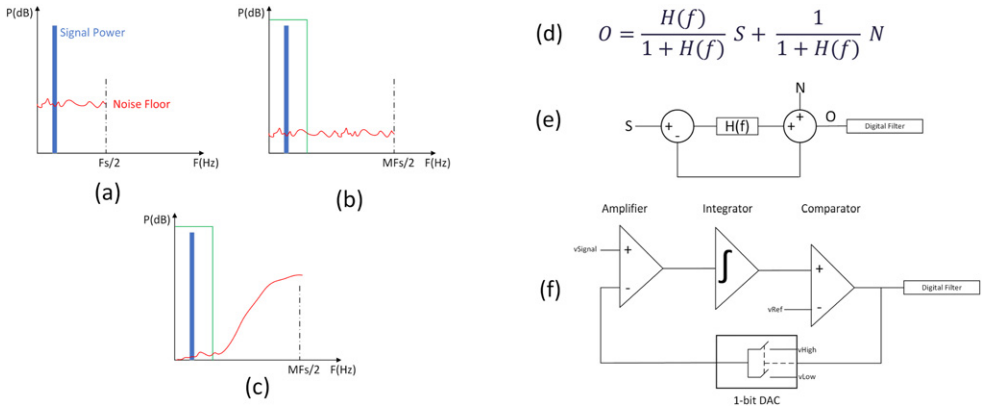

Figure 3. Simple illustration of the operation of a sigma-delta ADC. The figure on the left illustrates how noise in the target band (a) is first spread over a wide band by oversampling by a factor M (b). This could then simply be filtered (green line), but additional reductions can be achieved by noise shaping the result (c). The figure on the right illustrates the transfer function needed to generate this noise shaping effect (d), the required control system (e), and a typical implementation (f).

The sigma-delta device implemented on this chip is an incremental second order feed forward type, described more fully in [11]. Its default bit depth is 12. Since the approximate formula for Effective Number of Bits (ENOB) as a function of oversampling ratio M is ENOB $= 2\log_2(M) - 1$, this requires approximately 91 clock cycles to complete a conversion. Using 100 cycles, and a default clock speed of 100 MHz, this leads to a conversion time of 1 MSPS. However, the maximum bit depth of the ADC is 17 bits, and the clock speed can be varied, meaning it can be adapted to a wide variety of situations.

3 Testing

The devices described in the previous section have undergone characterisation, and in this section we report the results. Here, we follow the opposite order to the previous section, and report results working backwards along the signal chain from ADC to pixel, establishing the functionality at each stage. The ADC and analogue chain can be tested separately by injecting test voltages as shown in figure 4.

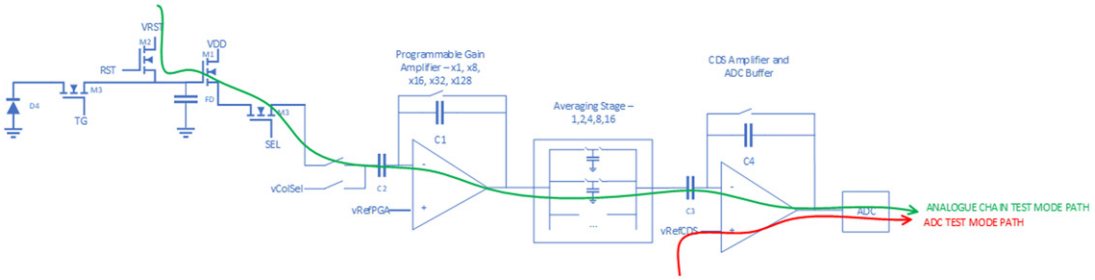

Figure 4. Illustration of how test voltages can be injected into the chip, and the resulting test paths for characterising the ADC and analogue chain.

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3.1 ADC

Testing was first carried out on the ADC, initially in the default mode, generating a 12 bit conversion. Owing to a beat frequency between clocks in the readout section generating additional noise, best performance is obtained running slightly faster than the 1 MSPS target, so results were acquired at 1.2 MSPS and are shown in figure 5.

Quantity	Unit	Value
Max Gain	ADU/V	2515.72
Min Gain	ADU/V	2439.02
Average Gain	ADU/V	2474.92
Gain Standard Deviation	ADU/V	21.09
Max DNL	ADU	1.24
Min DNL	ADU	-0.82
Max INL	ADU	2.26
Min INL	ADU	-7.53
Average Noise	uV	322.99(0.83)

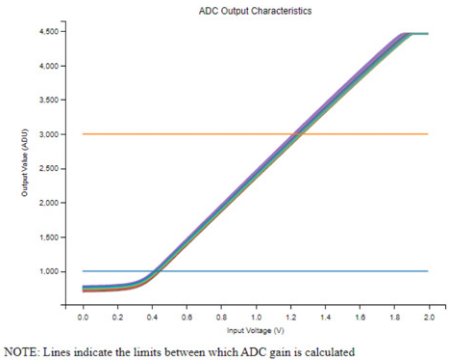

Figure 5. Performance of the ADC at 1.2 MSPS.

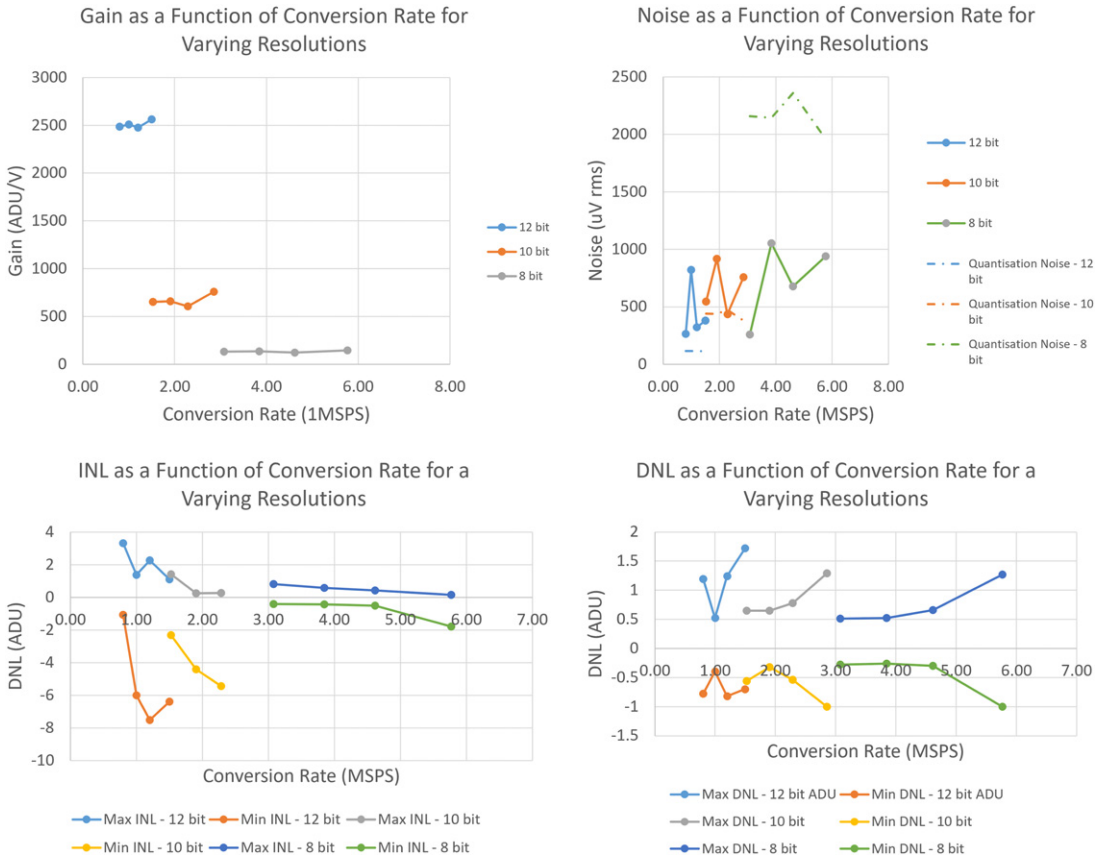

Figure 6. ADC gain, noise, INL and DNL over a range of bit depths and sample speeds.

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As can be seen both by eye and in the measurements in the table, the gain variation in the ADC is very low, which was one of the expected benefits of this architecture.

The ADC was also tested for a wider range of speeds and bit depths. The results of these tests are shown in figure 6. They demonstrate that the ADC can be operated at almost 3 MSPS at 12 bits before the minimum DNL decreases below −1 LSB, and missing codes begin to appear. At 8 bits, the speed can be extended to almost 6 MSPS. Another interesting point can be observed from the noise plots. Sigma-delta devices should be able to achieve a noise below the quantisation noise (see [12] for a tutorial introduction to these devices), which is also plotted in the noise plot in figure 6. We can see that this occurs at 8 bits, but not at the higher resolutions. This is because, as shown in figure 4, the test path for the ADC also includes one of the preceding amplifiers, and this imposes a floor on the noise, which is above the quantisation noise at 10 and 12 bits. At 8 bits, the quantisation noise is higher, and we are able to see the effect of the sigma-delta loop reducing the noise below the quantisation level.

3.2 Analogue chain

Similar testing was carried out for the analogue chain. Here we are mostly concerned with establishing how the noise and gain of the chain varying with different nominal PGA gains. The results of this testing are shown in figure 7.

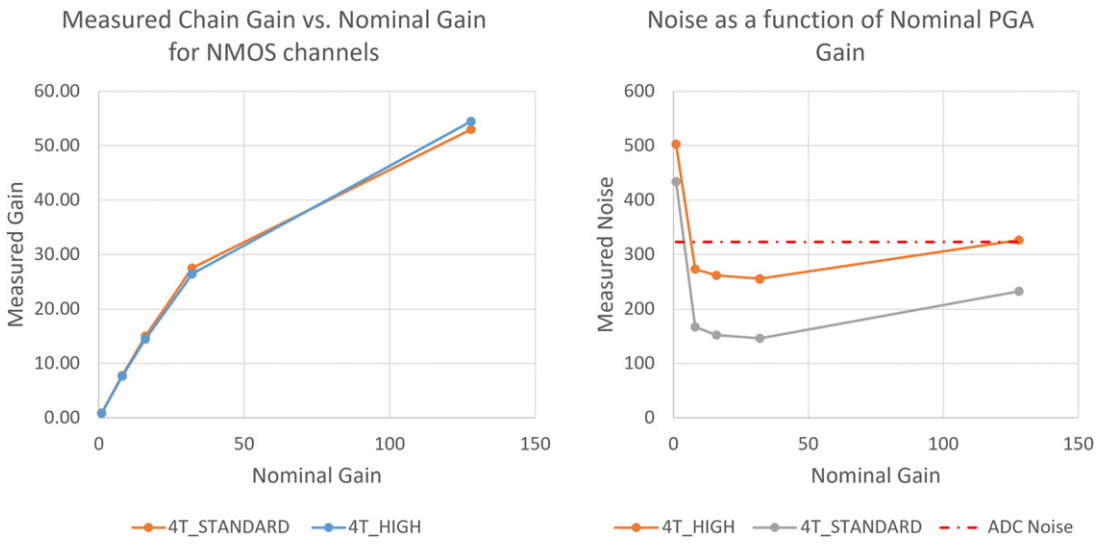

Figure 7. Analogue chain gain and noise as a function of nominal PGA gain.

From these results, we can see that the measured gain is approximately 0.9× the nominal gain until the highest value, at which point it drops off further. The 0.9 factor can be explained as the impact of the NMOS pixel source follower (only the NMOS side has been characterised so far). The drop off at higher gain appears to be an artefact of the way the test voltage is injected, since it does not appear in pixel measurements, as will be shown in section 3.3. These results also show the decrease in input referred noise with increasing gain—again with the caveat that the incorrect

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measurement of the higher gain makes the noise appear to rise. The ADC noise is also plotted in this graph in order to demonstrate the positive effect of employing a PGA. The two different NMOS pixel types show different noise levels due to differences in their source followers. It will be seen in section 3.3 that the higher voltage noise of the 4T_HIGH pixel is compensated for by its higher gain, leading to a lower input referred noise.

3.3 Pixels

In this section we describe Photon Transfer Curve (PTC) measurements of the pixel performance. Both the standard and high gain 4T pixels are studied. Also, since the goal of this work is to apply these techniques to lower gain pixels with other useful properties, results from the ENC_PMOS device will also be presented. In this section, we also employ the averaging stage to reduce the noise further.

Figure 8 shows the noise performance of the 4T_STANDARD and 4T_HIGH pixel, which are measured to have conversion gains of 80 and 168 $\mu V/e^-$ respectively. As can be seen from the noise measurement, the averaging stage has less of an effect on the high gain pixel than on the standard one, which might imply that another noise floor in the system is being reached.

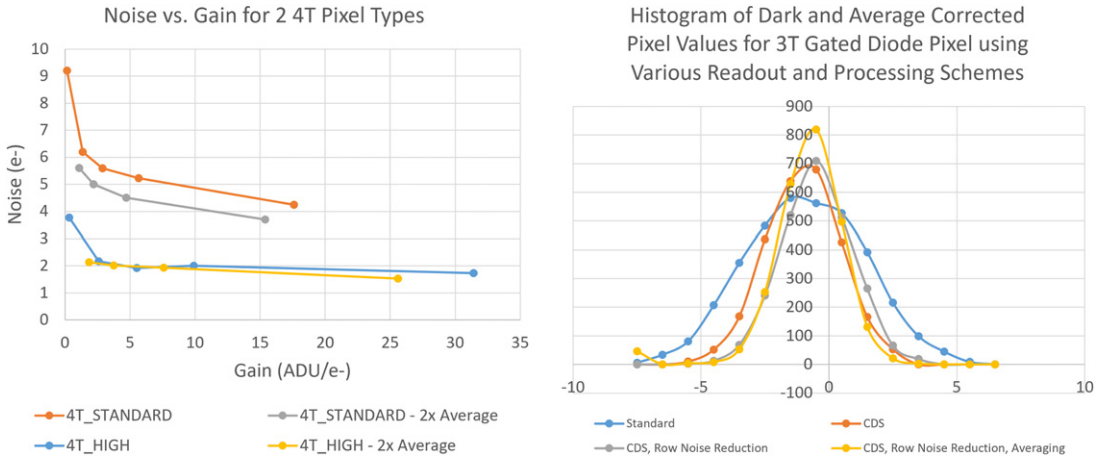

Figure 8. Noise of 4T_HIGH and 4T_STANDARD pixels with and without two level averaging. Note that the uptick in noise from the analogue chain measurements does not appear in the pixel measurements.

All these techniques can also be applied to lower gain pixels. For example, compared to the 4T pixels, the ENC_PMOS pixel has a much lower conversion gain of 22 $\mu V/e^-$, which leads to a noise of 42e^-. However, if CDS, row noise removal and the averaging stage are employed, a significant noise reduction is possible, as shown in figure 8. Employing these techniques reduces the noise to 30.7e^- — a reduction of 27% on the starting figure.

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4 Summary

In this paper we have described PRECISE—a testbed for circuit blocks to be used in future image sensors. These blocks have been described, and their tests results reported. Results have been reported for a pixel with a noise as low as $2e^-$, and the techniques used to achieve this have also been used to reduce the noise of a radiation hardened pixel by 27%. Future work will include testing the remaining pixels, and attempts to further improve the noise performance.

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