A real time system for energy spectrum measurement in nuclear pulse processing application

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Abstract

A real time VHDL algorithm has been developed and hardware implemented on FPGA to measure the energy. A digital trigger and timing (RC-CR^2) filter developed is used for trigger generation. A digital trapezoidal filter is developed for shaping of pre-amplified output of radiation detector for high resolution energy measurement. ADC digitized data is processed by this algorithm. Timing information (trigger) is used to find region of interest of radiation detector output. Energy of pulse in the region of interest is measured using the digital trapezoidal filter. Processed data is transferred to computer over 1 Gbps Ethernet for data archiving. Software is developed to plot energy spectrum. This algorithm has been tested on a FPGA kit for a real time test data up to a clock rate of 100 MHz.

Introduction

In high resolution radiation spectroscopy, the electrical charge pulse generated by a pulse radiation detector is acquired and analyzed to measure gamma-ray energies. It is required to estimate the time of arrival, amplitude of pulse and the energy spectrum of the received pulse. Traditionally, estimation is performed by analog systems [1] such as Multi-Channel Analyzers (MCA), Charge integrating ADC (QDC), Time to Digital Converters (TDC), Discriminators etc., however, they are often noisy. A fully digital data processing approach is proposed in this work in order to overcome noise inherent in analog processing and because of several other advantages of digital system over an analog system as well [2].

In this work a real time FPGA based digital pulse processing module is developed and hardware implemented. This module measures energy of particle and time of arrival information and give energy spectrum. Output of preamplifier is directly given to this module to extract the energy and the time stamp information. This work includes a digital trapezoidal shaping filter for the energy measurement with high resolution and a digital RC-CR^2 trigger and timing filter for the time stamp measurement [3]. System is run time programmable for different detector. It will give best result with HPGe detector because of HPGe detector inherent high resolution [4].

Hardware implementation setup

A 12-bit high speed analog to digital convertor kit is deployed for digital conversion of pre-amplifier data. The acquired output of ADC is given to FPGA for digital processing. The FPGA process the data and finds the energy and the time stamp information and this information is transferred in a packet form [Fig:1] to the computer for data archiving over 1 Gbps Ethernet link. Each packet contains 121 event data (8 byte time stamp 4 byte energy per event). Software is developed to plot energy spectrum using received packet data.

Field	Data Type	Position	Description
Message Header	BYTE	1	Rise Time
	BYTE	2	Flat Top
	BYTE	3	Threshold
	BYTE	5	Width
	BYTE	6	Baseline
	BYTE	10	Peak mean width
	BYTE	12	Reserve Bit
Message	Reserve Byte 8 byte		
	Time 8 Byte		
	Energy 4 Byte		
	Time 8 Byte		
	Energy 4 Byte		
	. . . . .		
	Time 8 Byte		
	Energy 4 Byte		

Figure 1 Data packet format transferred to UDP/IP[Packet length 1472 Byte]

Digital trapezoidal filter algorithm

Impulse response of the proposed trapezoidal filter is described by the following equation:

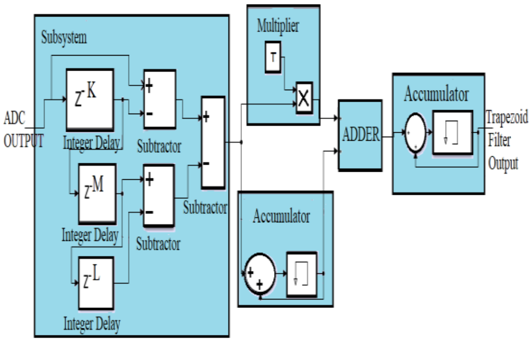

Figure 2 Simulated diagram of hardware implemented Digital trapezoidal filter.

$h(n) = h(n-1) + t(n) + \tau w(n)$

Where $w(n) = \delta(n) - \delta(n-k) - \delta(n-m) + \delta(n-k-m)$

$t(n) = {}^{n}\sum [\delta(j) - \delta(j-k) - \delta(j-m) + \delta(j-k-m]$

τ : Decay time constant of input exponential
h(n) : Trapezopidal filter impulse response
k,m,l : Arbitrary constant(Determine resolution)

IIR filter in recursive form is implemented for computation efficient implementation[Fig:2]. When h(n) operates on exponentially decaying output of preamplifier it generates trapezoidal pulses. Flat top, rising edge, width of pulse all are run time programmable according to the detector used. Height of trapezoidal pulse after baseline restoration gives energy information.

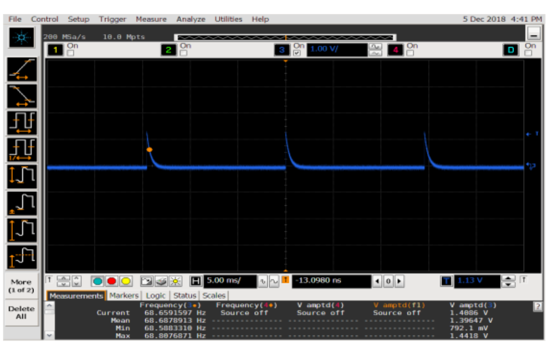

Figure 3 Test data input generated from arbitrary function generator.

Result

Figure 2 shows the hardware implementation of proposed algorithm in simulation. For testing arbitrary function generator is used [Fig.2]. Figure 4 shows the energy spectrum plotted with test data.

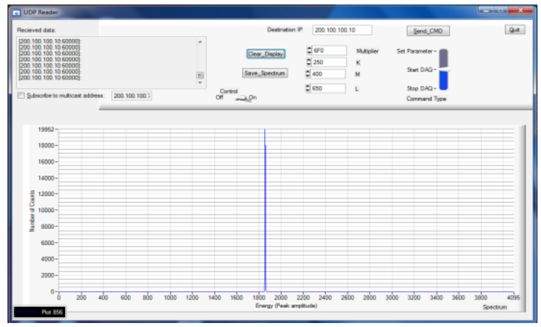

Figure 4 Energy spectrum plot with real time processing of test data on developed system.

Conclusion

Efficient algorithm for time stamp and energy measurement of nuclear pulse has been developed and implemented on FPGA kit. This algorithm operates at 50/100 MHz rate and gives pulse amplitude independent trigger with jitter value of two clock cycle with respect to pulse arrival. Based on this event identification, further processing of data for energy was carried out. Energy spectrum is plotted for test input.

References

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