FPGA based Time-to-Digital Converter

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A high resolution, wide dynamic range Tim-to-Digital Converter (TDC) is implemented in a low power Flash-based Field-Programmable Gate Array (FPGA). The TDC uses Vernier ring oscillator technique to achieve high resolution and wide dynamic range with less FPGA resource consumption. The presented TDC achieved 160 ps resolution (LSB) over the dynamic range of 0 – 1.3 µs.

1. Introduction

High-resolution Time-to-Digital converter (TDC) is one of the crucial blocks in High-energy nuclear physics time of flight experiments. The contemporary time interval measurement techniques rely on employing methods like Time-to-Amplitude Conversion, Vernier method, Delay Locked Loops (DLL), Tapped Delay Lines (TDL), Differential Delay Lines (DDL) etc. Recently, FPGA based TDC designs with merits of low cost, fast development cycle and re-programmability are reported [1]. The TDC implementation in FPGA have design challenges and issues like, lack of direct control over the propagation delays, unpredictable Place & Route (P&R) delays and delay variations due to Process, Voltage & Temperature (PVT) variations.

In the TDC design presented here, the resolution below the minimum gate delay is achieved by employing differential (Vernier oscillator) technique. The predictable P&R is achieved by manual P&R of the critical elements and avoiding the use of digital synthesis tools. Further, in order to compensate for the delay variations due to PVT, a calibration methodology is developed and implemented. By implementing the design in a Flash-based FPGA, the low power design objective is achieved.

2. Design Principle

The heart of the design is two precise retrigger-able ring oscillators of very slight difference in periods ($\Delta\tau$). These oscillators are used to measure the time difference between two pulses START and STOP, as shown in Fig.1. The slow oscillator (period T_1) is triggered by START and the fast oscillator (period T_2) is triggered by STOP. Now, as $T_2 < T_1$, and STOP arrives later than START, eventually the rising edge of the fast oscillator will coincide and lead the rising edge of the slow oscillator, which is detected by a phase detector. In this scheme, both the oscillators serve as a clock to their respective counters and the clock pulses are counted as shown in Fig.1. Both the counters stop counting when the phase detector detects the phase coincidence of the oscillators.

If $\Delta\tau = T_2 - T_1$, n_1 and n_2 are respectively the number of counts in coarse and fine counter, then the relation of the Time interval ($T_{start\text{-}stop}$) is determined by Eq.1.

$$T_{start\text{-}stop} = (n_1 - 1)\,T_1 - (n_2 - 1)\,T_2 \qquad \text{Eq.1}$$

$$= (n_1 - n_2)\,T_1 + (n_2 - 1)\,\Delta\tau \qquad \text{Eq.2}$$

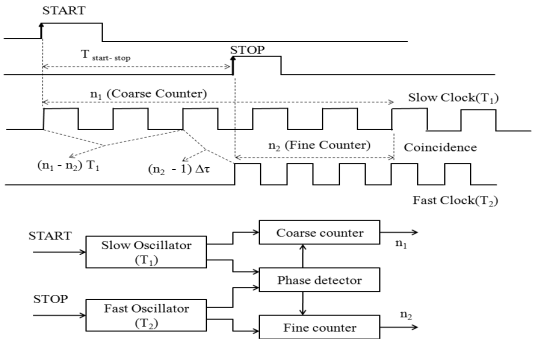

Fig. 1 Timing and block diagrams

3. Circuit Implementation

The critical blocks of the TDC are ring oscillators, phase detector and fast counters. The two ring oscillators with slight difference in period are realized as shown in Fig.2. The

oscillator design incorporates features like trigger synchronized starting & stopping and retrigger-ability. The very slight and precise difference in periods is obtained by carefully balancing the place & route delays in both oscillator circuits and by changing the feedback load as shown in Fig.2. In this scheme, the slow oscillator's And-Or-Invert gate has a fan-in of two and larger delay, where as the fast oscillator's NOR gate has a fan-in of one and lesser delay. This creates the slight difference in periods. Two long duration counters employed in calibration determines the exact difference in periods and calibrates the TDC.

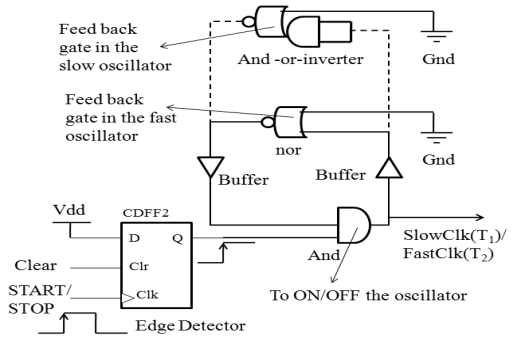

Fig. 2 Circuit for Slow and Fast Oscillators

The Phase Detector (PD) circuit shown in Fig.3, provides information regarding the phase change between slow and fast oscillators. The D-FF1 is introduced to reduce the probability of meta-stability by providing sufficient settling time of one fast oscillator period (T_2) to D-FF2 [2]. The conversion process is completed when PD outputs logic 'High'. On this event, both the counter values are latched, both the oscillators are stopped and an end of conversion (EOC) signal is generated.

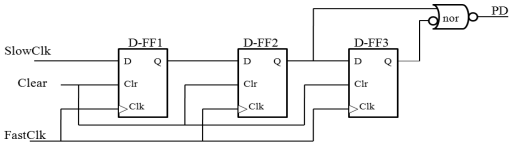

Fig. 3 Circuit for Phase detector

4. Test Results

The TDC is tested using Phillips Scientific 7120 time interval pulser.The test resluts of the TDC are tabulated in Table 1. The linearity (between 0 to 70 ns) and histogram (input time 120 ns) plots are shown in Fig.4.

Table 1: Tabulated values of the test results

Specification	Value
Slow oscillator period (T_1)	6.02 ns
Fast oscillator period (T_2)	5.86 ns
Resolution $\Delta\tau = (T_1 - T_2)$	160 ps
No.of bits in the coarse counter	8
Maximum no. of counts in fine counter $k = T_1 / \Delta\tau$	38
Dynamic range $DR = (2^8 - k) * T_1$	1.3 µs
Number of bits	13
Differential non- linearity (DNL)	3.4 LSB
Integral non- linearity (INL)	5.1 LSB
Pricision (σ) of the measurments	~ 0.6 LSB
Logic resource consumption	199 tiles

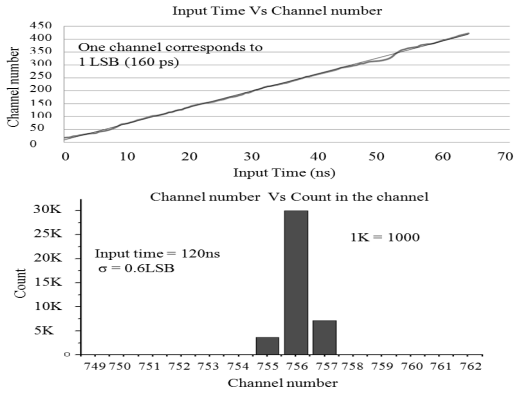

Fig. 4 Linearity and histogram plots

5. Conclusion

The TDC is achieved high resolution, wide dynamic range in low power Flash-based FPGA and consumed less FPGA resources. However, multi channel TDC design in FPGA is critical because of place and route difficulties.

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References

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[2] Application Note AC308.