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TESTING ASPECTS OF THE CERN BEAM INTERLOCK SYSTEM PRIOR TO INSTALLATION IN THE ACCELERATOR

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Abstract

The Beam Interlock System (BIS) is the backbone of the machine protection system throughout the accelerator complex at CERN, from LINAC4 to the LHC. After 15 years of flawless operation, a new version of the BIS is currently being produced and will be installed in the LHC, SPS and North Area during CERN's Long Shutdown 3 (LS3), planned to start in 2026. Overall, more than 3,000 Printed Circuit Boards will be produced and assembled outside CERN. In addition, more than 120,000 lines of firmware and supporting scripts are written to implement the critical and monitoring functionalities of the BIS.

Both hardware and firmware need to be thoroughly tested before installation and operation to guarantee the high levels of reliability and availability required by the operation of the accelerators. In this paper we present the testing methodology including the development of dedicated testbeds for hardware validation, the use of comprehensive simulation and continuous integration for firmware development, and the implementation of automated tests for system-level functional validation.

INTRODUCTION

The CERN BIS is a highly dependable communication system that provides the interface between user systems, e.g. power converters, warm interlock controllers, vacuum, beam loss monitors, and various actuators, e.g. injection or extraction kickers, beam dumping systems, or beam intercepting devices [1]. This system has been in operation for more than 15 years throughout the CERN accelerator complex and is now becoming obsolete. The new version of the BIS is currently being developed [2]. Due to its required high levels of reliability and availability, testing the BIS electronic boards and functionalities is crucial to the success of its future deployment in the machine in LS3, planned to start in 2026 [3].

BEAM INTERLOCK SYSTEM INVENTORY

The BIS is composed of two main types of boards: the User Boards, that provide the interface for the user systems to connect to the BIS, and the VME-based boards, installed in the BIS crates, that provide the interlocking functionality.

More than 3,000 custom-made boards will be produced between 2024 and 2026. The BIS hardware inventory is summarized in Table 1.

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HARDWARE VALIDATION

Several board types are of prime importance to the safety of the machine, by the role they have in the BIS, and/or the quantity of boards deployed in the accelerator. This is the case for the BIS user interface single/double connected via copper cables (CIBU$_{S/D}$), the BIS user interface connected via optical fibres (CIBF), and the BIS manager board (CIBM).

Hardware test beds have been developed to detect any issue that may occur during the production of the Printed Circuit Boards, the assembly, or the transport.

Example of the CIBU Hardware Test Bed

The CIBU boards are tested using a specific test bench based on National Instrument PXI Platform [4]. This crate connects to a Test Controller Card (TCC), that interfaces with the Device Under Test (DUT). The TCC and its dedicated probes designed to test the CIBU$_{S/D}$ are presented in Fig. 1.

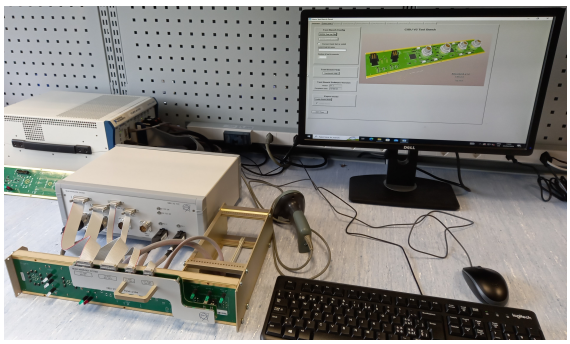

Figure 1: CIBU$_{S/D}$ test bed.

The test bench is coded in C language and uses the National Instrument Labwindows CVI framework to interface between the Graphical User Interface and the PXI modules.

The test bench software allows both experts and operators to test boards. In the password-protected expert mode, the user has the possibility to run tests manually. This can be used when debugging a board and easily identify hardware issues. In the operator mode, the test sequence is protected and is executed in an automatic manner.

In operator mode, the test sequence is as follows:

- test bench initialisation of PXI modules
- power CIBU
- ramp User Permit
- program the CIBU FPGA with test firmware
- test FPGA interfaces (oscillator, EEPROM, PSU diagnostics, communications, ADC, LEDs)
- program the CIBU FPGA with the production firmware
- generate a test report

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Table 1: BIS Inventory of Custom-made Boards

Board	Description	LHC	SPS	PSB LINAC4	North Area	Spares	Total
CIBM	Manager board	76	36	22	18	32	186
CIBG	Generator board	4	5	3	2	10	24
$\text{CIBFI}_{RX/TX}$	Fibre optics controllers	14	41	1	19	26	101
CIBDS	LHC Beam Dumping System re-trigger	2	0	0	0	4	6
CIBAB	Actuator board	8	12	10	6	10	46
$\text{CIBU}_{S/D}$	User interface (copper)	175	123	95	36	56	485
CIBF	User interface (fibre)	12	19	1	13	17	62
CIBFX	User interface x10 (fibre)	4	39	0	19	17	79
CIBD	User board power supply	382	362	192	136	128	1200
CIBSFP	Mezzanine card for optical interfaces	16	58	1	32	34	141
$\text{CIBP}_{L/S}$	Rear panels for LHC and injectors	21	19	11	9	16	76
$\text{CIBE}_{S/D}$	Extender boards for BIS crates	210	190	110	90	70	670
Total							**3076**

Example of the CIBM Hardware Test Bed

Another example of a hardware test bed, is the CIBM TCC that was developed to perform hardware tests of the CIBM after production, see Fig. 2.

This test bench is coded in Python and is based on JTAG ProVision. A specific CIBM TCC and rear-panel boards have been developed to communicate with the DUT. JTAG ProVision uses Boundary-scan technology to test the interfaces of the devices connected to the JTAG chain. In the case of the CIBM tester, the aim is to perform electrical tests of all the interfaces of the two FPGAs on the board.

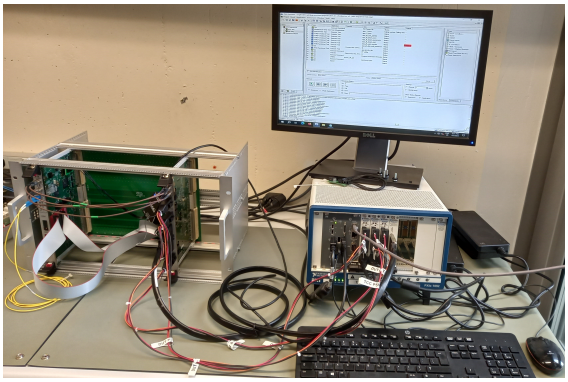

Figure 2: CIBM test bed.

Hardware Validation During Production

All 485 $\text{CIBU}_{S/D}$ (single/double interface) have been produced, including 20 radiation tolerant CIBU_S, 400 standard CIBU_S and 65 CIBU_D. As of April 2024, 205 have been correctly tested. Several assembly or manufacturing errors have been detected, in particular bad solder joints, malfunctioning LEDs and damaged connectors.

In addition, 1200 CIBD (User Board power supplies) have been produced, out of which 190 passed the tests.

A subset of the boards successfully tested have been deployed in the SPS during CERN's Year End Technical Stop 23/24 (YETS) [5].

FIRMWARE VALIDATION

All BIS boards contain between 1 to 3 FPGAs, all configured with different firmware. Two main types of firmware are implemented on the BIS: critical and non-critical. Critical firmware is deployed in most boards, this groups all the functionalities that are critical to the safety of the accelerators, for example making sure that a beam dump request is generated when a user raises an interlock, ensuring that redundant critical paths are always triggered, etc.

Firmware Simulation

Extensive simulations of the firmware are mandatory to ensure its correct functioning. Numerous test benches have been written to validate the behaviour of low-level as well as top-level modules.

As an example, one core module in the BIS aims at monitoring the Beam Permit Loop (BPL) frequency. The BIS architecture is based on multiple Beam Interlock Controllers that are chained together using optical fibres and SFP [6]. The BPL 'TRUE' frequency is generated by the CIBG and either forwarded by each controller if no interlock is raised, or replaced by the 'FALSE' frequency in case of an interlock. One firmware module is responsible for detecting if the BPL is 'TRUE' or 'FALSE' in order to send a beam dump request in case of an issue.

The simulation test bench of this module must ensure that the module detects any loss of BPL 'TRUE' frequency, while allowing a certain tolerance on BPL frequency deviations. These might arise due to variations in measurement windows or degradation of transmitter optical power, receiver sensitivity, or fibre attenuation.

To this end, the test bench generates several frequencies and triggers errors in case of unexpected behaviour.

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This basic example is fully deterministic, i.e. if the module under test or the test bench do not change, then the results will always be the same. More complex simulations are run where the test bench introduces uncertainties, for example by generating random delays.

Firmware Continuous Integration

Continuous integration is extensively used in the development process of the BIS firmware. Using Gitlab CI/CD together with custom-made dockers, non-regression tests are run every night on all boards' firmware. Three main categories of tests are run: linting, simulation, and synthesis.

The linting tests aim at ensuring that all developed firmware meet the same coding guidelines. Static checks on the VHDL code are run and aim at finding basic errors that developers might make.

The simulation tests aim at detecting behavioural errors in the code. These might happen following a code change of the module under test, but can also happen following an update of the generic sub-modules that are shared between all the BIS firmware.

The synthesis test aims at ensuring that each firmware can be synthesized and implemented successfully. They also include static timing analysis to detect potential timing violations as early as possible.

The implementation of continuous integration allowed detecting numerous mistakes, either basic ones like missing design files, or more subtle ones like unexpected module behaviour.

SYSTEM-LEVEL FUNCTIONAL VALIDATION

System-level functional tests aim at validating the behaviour of the BIS as a system. These tests aim at detecting functional errors that designers might have overlooked during the development stages.

BIS Test Platform

A Test Platform for the BIS has been developed to test the behaviour of the system under different scenarios. The Test Platform uses all BIS boards and tests the behaviour of each board by running various test cases.

The Test Platform crate is presented in Fig. 3.

Test scenarios include the opening of the Beam Permit Loop via software permit, user permit on CIBU or CIBF, or beam permit linking feature. In addition, the software pulls the diagnostics of all the boards at the start and stop of the test, and detects if any unexpected error counter incremented during the duration of the test. Finally, data from the FPGA embedded ADC, board ADC, and SFP are collected occasionally to draw waveforms and detect any unexpected values.

The test platform software is also run automatically by Gitlab CI/CD which programs the boards connected via JTAG, launches the test scenarios outside of working hours, totalling 108 hours of test per week, and reports any error.

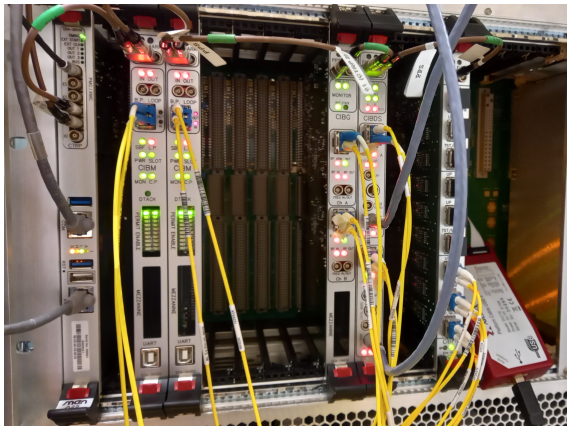

Figure 3: BIS Test Platform crate.

These automated tests helped detecting several issues, including rare events that would likely have been unnoticed without extensive robustness tests.

LHC Test Bed

Further to the tests performed in the laboratory, a test version of the new BIS is foreseen to be deployed in the LHC during CERN's YETS 24/25. It will consist of a 27-kilometer double optical loop in parallel to the operational BIS. It will use local permits provided by the operational BIS and will allow analysing the behaviour of the new version of the BIS over the last year of the Run 3 of the LHC.

CONCLUSIONS

Numerous tests are being performed on the BIS boards' hardware and firmware prior to installation in the machine. A combination of electrical and functional tests is necessary to guarantee the required high levels of reliability and availability of this system.

Automated robustness tests developed and ran during the prototyping phase allowed discovering several design issues that were fixed in the final version of the boards. After production, several issues have been found due to assembly and transport. Thanks to extensive testing, these were discovered early and mitigated before installing the equipment in the accelerator.

In addition to the laboratory tests, hardware commissioning tests will be performed during and after the installation of the new BIS in the accelerator during CERN's Long Shutdown 3.

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