

Optical ranging and data transfer development for LISA

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Abstract.

In order to implement optical inter-spacecraft ranging and data transfer for LISA, the carrier of the laser link must be phase modulated with pseudo-random noise sidebands. The data acquisition and delay estimation are then implemented in the phasemeter as back end processing. This work presents a proposed demodulation scheme with submeter ranging accuracy and several kilobytes data rate. Its functionality is demonstrated both in a software simulation and in a FPGA-based hardware implementation.

1. Introduction

The Laser Interferometer Space Antenna is an international space project to detect and observe gravitational waves on the frequency range from 0.1 mHz to 100 mHz. LISA is a cluster of three satellites forming an equilateral triangle and separated by five million kilometers communicated via three bidirectional laser links. The primary quantity to be measured is the pathlength variation between the free-floating test masses onboard two different spacecraft by means of heterodyne interferometry with a required sensitivity of $1 \text{ pm}/\sqrt{\text{Hz}}$. It must be taken into account that, due to relative movements between the spacecraft, the distance of the interferometer arm is expected to change approximately $\pm 1\%$ over one year orbit ($\simeq 50.000 \text{ km}$). As consequence, the resulting unequal arm configuration of LISA turns laser frequency into excess noise added to the measured phase, which could spoil the scientific performance of the mission. One of the three methods planned to reduce the influence of laser frequency noise is time-delay interferometry (TDI). This consists in post-processing the data on ground to make LISA work virtually like an equal arm interferometer, suppressing the frequency noise contribution up to seven orders of magnitude. However, TDI is based on the knowledge of the absolute distances between the satellites with meters resolution and hence any error in this ranging measurement will turn into an error in the TDI post-processing scheme. To achieve the mentioned accuracy, a pseudo-random noise (PRN) sequence can be modulated on the phase of the laser link. The PRN sequence in the remote laser phase can be measured by the local phasemeter system (PMS) [1, 2] and its correlation with the local PRN can be performed as phasemeter back-end processing, delivering the light travel time τ between the satellites.

2. Architecture and system modelling

Each of the six lasers in the LISA constellation has to be phase-modulated with a different PRN codes that minimise the correlation with the other five for any given delay and with himself for delays different of zero. The set of six PRN sequences implemented shown in Figure 1 have been obtained by numerical optimisation and with selected correlation properties. This way, the correlation peak serves as a timestamp if the start of the PRN is synchronized with the clock of the remote spacecraft.

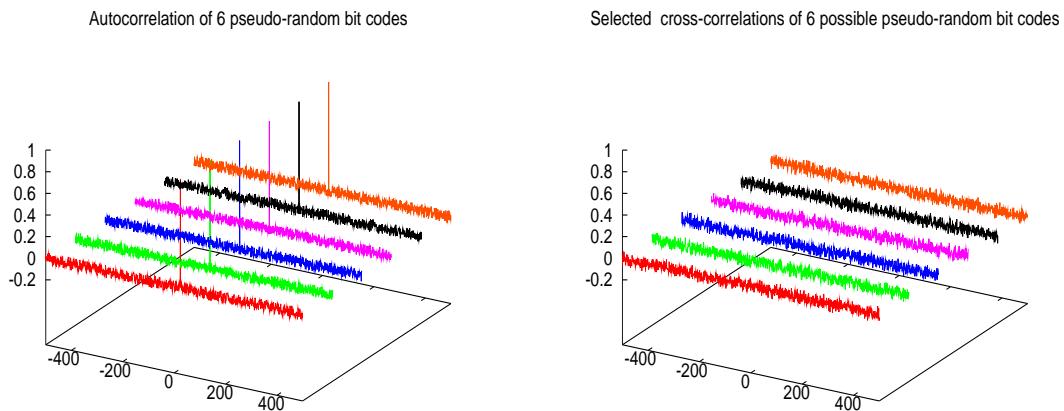


Figure 1. Autocorrelation and crosscorrelation between a possible set of pseudocodes

The proposed scheme uses a digital delay-locked loop (DLL) architecture[3] to track the correlation peak (see Figure 2). The delay-locked loop is based on the correlation of the input signal with three versions of the same reference PRN: a punctual, an early and a late. The early and late version are delayed by one chip¹ between each other and the punctual version is remained equal than the PRN transmitted. The punctual correlator is responsible for the data recovering and peak detection whereas the early and late correlators provide the tracking between the incoming and local PRN. The difference between early and late correlators can be used as error signal in a control loop to update the delay of the code generator to the input signal.

¹ One code bit of PRN is also called as chip

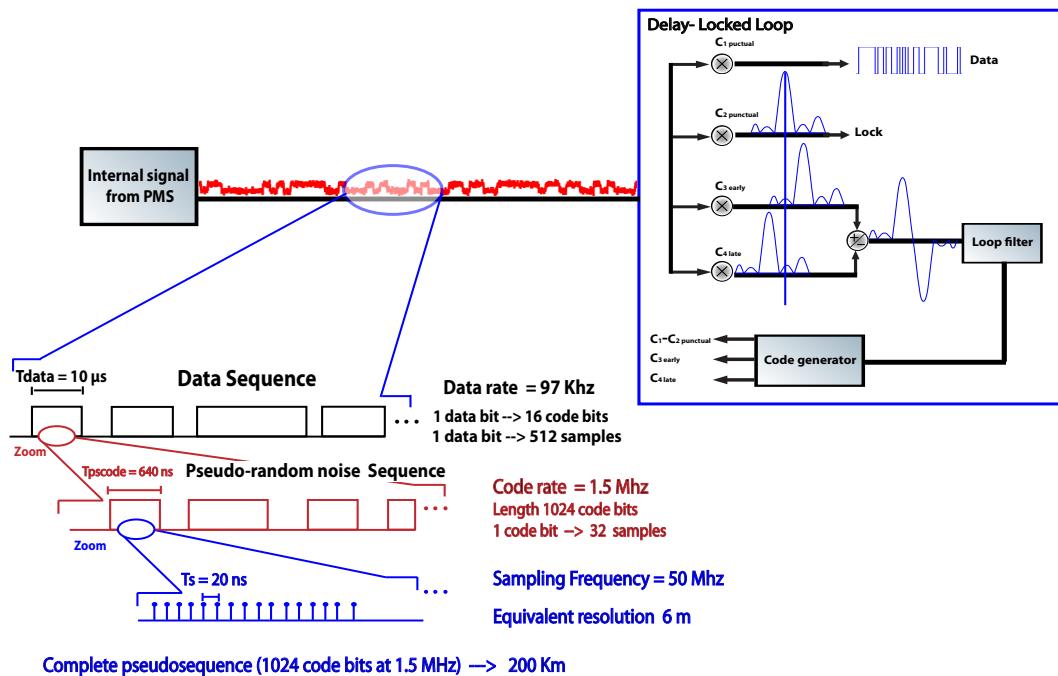


Figure 2. General block diagram of the delay-lock loop implemented in the same board than the phasemeter and design parameters for DLL implemented in the simulation and FPGA prototype

3. Simulation and hardware implementation

In order to demonstrate the functionality of the DLL, a software simulation was developed previously to the implementation on FPGA-based hardware. The design parameters for both of them are also shown in Figure 2: the bottom time series represents the phasemeter output sampled at 50 MHz. A pseudo-random noise (PRN) sequence is encoded on this phase signal at a chipping rate of 1.5 MHz, as shown in the middle time series. The PRN code-length of 1024 results in a code repetition every 200 km armlength, and the chipping rate is selected to optimise the ranging accuracy and robustness. The top part of the figure shows the data sequence, encoded on top of the PRN at 97 kHz.

Figure 3 summarises the current implementation running on the phasemeter board[4]. The processing unit is provided by a single FPGA (field programmable gate array) and the input signal to the DLL is internally synthesized. The DLL features two possible working modes:

- **Acquisition mode:** In this mode, the delay between the incoming signal and the local PRN is estimated with one chip resolution ($T_c = 640$ ns) without any previous information. To this end, the incoming signal is correlated during a complete period of the local PNR ($\simeq 1.5$ kHz) using the punctual branch. The process must be repeated for all possible delay values. The resulting delay after this stage can be written as ($\tau = N \cdot T_c$), with N going from 0 to 1024.
- **Tracking mode:** Once the PRN chip of the incoming code has been identified, the early and late branches are used to correlate the incoming signal with a partial PRN-sequence (256 chips for the current implementation). This way, the delay between the incoming and local PRN-sequences can be estimated with nanoseconds accuracy.

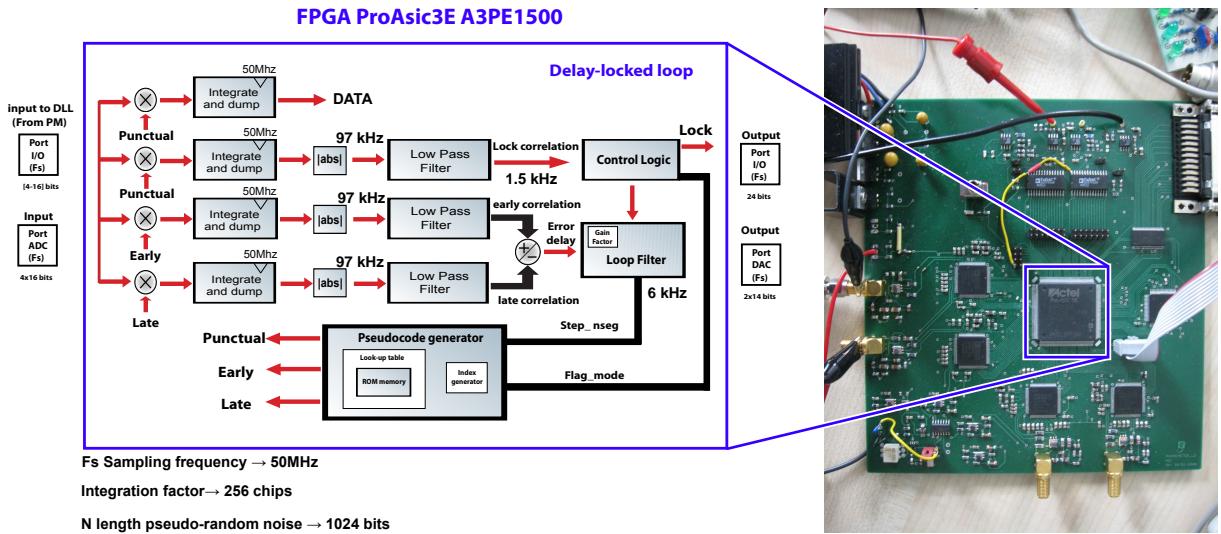


Figure 3. Implementation of the DLL in the same prototype board used for PMS development

The main characteristics of the used board can be summarised as follows:

- ProAsic3E Actel FPGA with 1.5 Million system gates with 147 high-performance inputs/outputs (I/Os)
- Four A/D-converters (AD9446-100) with 16-bit resolution
- Two D/A-converters (AD9744-210) with 14-bit resolution
- Enhanced parallel port (EPP) with output rate up to 1 MB/s
- High-speed PCI digital input/output (DIO) board with direct memory access features and maximal rate of 2 GB/s

4. Results

The results of the implementation of the proposed design in a software simulation are presented in Figure 4. These results have been verified in the FPGA target described in Section 3. The two top time series represent the input phase signal fed to the DLL with different levels of phase noise. In the left part of the graph, the input phase noise has been obtained assuming a normalized white noise of $A_N = 0.2 \text{ rad}_{\text{rms}}$ and a modulation index of 0.14 rad (for 1% power in side-band). This leads to a noise amplitude of $A_{\text{LISA}} = 0.2 \times 0.14 = 0.029 \text{ rad}_{\text{rms}}$ and consequently a equivalent phase noise of $\tilde{\phi}_{\text{LISA}} = A_{\text{LISA}}/\sqrt{f_s} = 4 \mu\text{rad}/\sqrt{\text{Hz}}$. In the left time series, the PRN sequence is clearly visible, in contrast with the right hand one which presents an increasing of $40 \mu\text{rad}/\sqrt{\text{Hz}}$ in the equivalent phase noise. The bottom part of Figure 4 represents the error signal in the tracking mode corresponding to each upper input signal, respectively. The correlation value is given by the substraction of early and late correlators at measurement rate of $\simeq 6 \text{ kHz}$ (integration time of 16 data bits, corresponding to 256 PRN chips). The system is able to match the correlation properties of the incoming signal and remains locked even in the presence of the described phase noise.

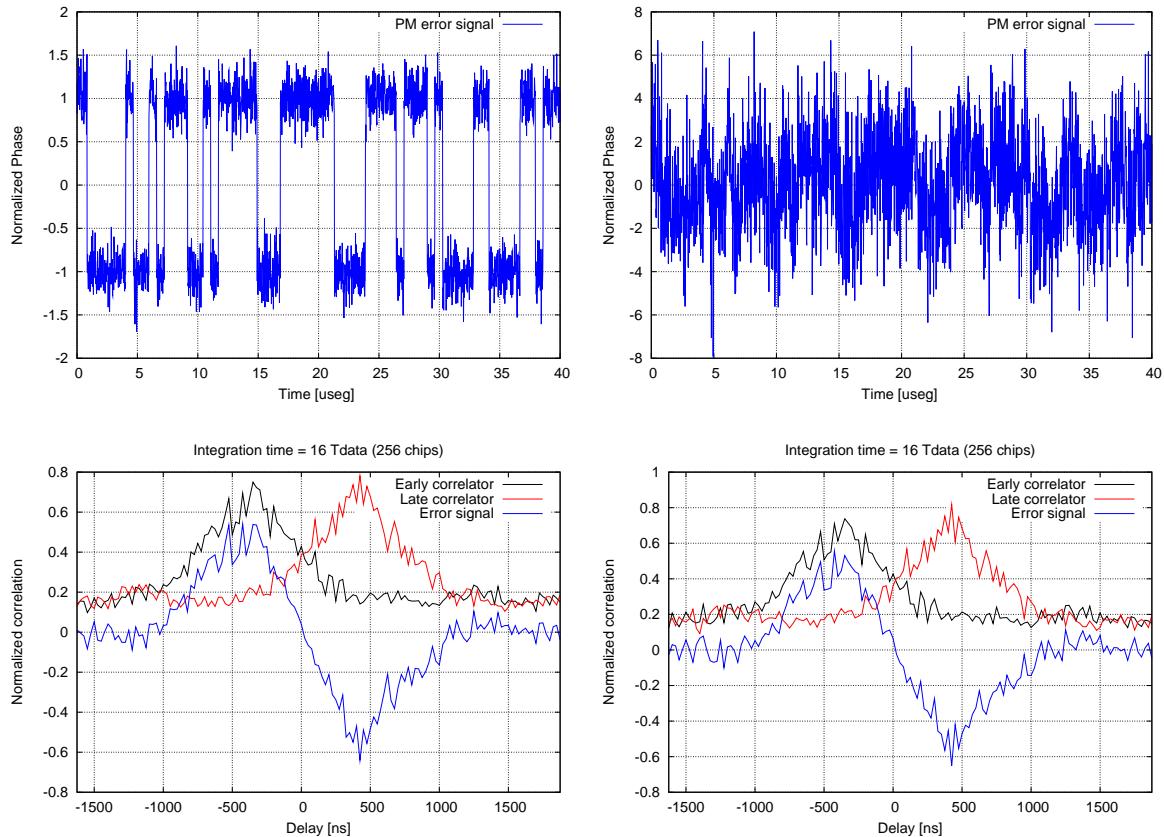


Figure 4. Noise impact on discriminator function for different amplitudes of additive gaussian noise, $\simeq 4 \mu\text{rad}/\sqrt{\text{Hz}}$ and $\simeq 40 \mu\text{rad}/\sqrt{\text{Hz}}$ respectively. Top: two time series of PRN with additive gaussian noise of amplitude. Bottom: resulting tracking error in presence of additive gaussian noise. Design parameters of the DLL: Integration time $T_i = 16$ data bits = 256 chips ($\frac{1}{T_i} \approx 6 \text{ kHz}$).

5. Conclusions

This paper presents an architecture based on a DLL for the implementation of optical ranging and inter-spacecraft data transmission for LISA. The proposed design can be implemented as back-end processing of the phasemeter. Its functionality has been tested in a software simulation and in a hardware implementation on the same board as our present phasemeter design.

The next steps include the evaluation of the performance with external phase signals and the integration, together with the phasemeter, in a full optical ranging experiment.

6. References

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