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PERSPECTIVE

# Scalable integration of quantum emitters into photonic integrated circuits

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## Abstract

Scaling up photonic quantum devices to reach complexities allowing to solve real-world problems requires a platform enabling scalable integration of solid-state quantum emitter with a high yield. Their nanometer-size together with their excellent quantum optical properties make them the ideal candidates for on-chip photonic quantum technologies. However, robust, scalable integration remains elusive. Here, we discuss the state-of-the-art methods to integrate quantum emitters into photonic integrated circuits, emphasizing the pros and cons of the integration methods applicable for specific quantum emitters. Based on our thorough comparison we give our perspective on the most promising approaches and how to overcome the remaining challenges.

## 1. Introduction

Quantum photonics has emerged as a promising technology to enable applications in quantum computation [1], communication [2], sensing [3], and simulation [4]. Unlike other carriers of quantum bits, information encoded on photons is only lost by photon absorption and not due to decoherence effects caused by their environment. This makes photons an ideal quantum information carrier only hampered by the source's intrinsic optical coherence. Up to now most photonic quantum technology demonstrations relied on bulky table-top implementations of photonic components, e.g., first quantum key distribution experiments [5] or the recent boson sampling showing quantum advantage [6]. Despite their major scientific impact, these experiments are not scalable to reach real-life applications. The marketability of photonic quantum technologies requires miniaturization and integration into hand-held devices, existing infrastructure, and space applications [7]. The roadblocks observed in many cases occur due to the large size and stability drifts of non-integrated systems. Implementing all device functionality, such as photonic quantum bit generation, manipulation, storage, and detection, on a scalable photonic integrated circuit (PIC) will significantly improve these shortcomings. A recent roadmap paper from Pelucchi *et al* [7] discussed in details the requirements on these quantum PICs, their building blocks, possible use cases, and the challenges hindering their realizations. One of the major bottlenecks is the on-chip photonic quantum bit generation. It requires the integration of quantum light sources as well as their efficient coupling to photonic circuits. A scalable approach would finally enable the generation of complex photonic cluster states, a resource for quantum computing and communication. Alongside the steady progress in miniaturization and integration of non-linear quantum light sources [8], a flourishing research field around the integration of solid-state quantum light sources in PICs has emerged to tackle this goal. In this perspective we give an overview of current approaches by categorizing different photonic circuit integration methods and discussing their advantages and disadvantages with respect to the solid-state quantum emitter type.

### 1.1. Integrable solid-state quantum emitters

Semiconductor quantum dots (QDs) [9, 10] are one of the most versatile quantum emitters developed in the past years, showing outstanding optical properties such as ultra-pure emission of single [11] and indistinguishable photons [12, 13] and the emission of entangled photons at cryogenic temperatures [14]. It is also possible to tune the emission wavelength, of epitaxially grown QDs, from the visible to the telecommunication band at 1550 nm via bandgap engineering [15, 16].

Color centers in diamonds (NV, SiV, etc) [17] are attractive structures for electron spin readout and manipulation [18, 19] due to their long electron spin coherence times in the order of up to seconds [20]. These long coherence times can only be achieved if cryogenic temperatures are employed along with dynamical decoupling techniques that modify the interaction between the system and the environment [21]. The long spin coherence time makes color centers excellent candidates as stationary quantum bits for optically addressable quantum memories [22] and suitable for quantum information processing [23–25] and multi-mode quantum networks [26]. In addition, indistinguishable photons [27, 28] and spin-photon entanglement were reported for NV [29] and SiV [30, 31] centers. Color centers in SiC crystals also offer high photon emission rates [32] as well as electron spin readout possibilities [33]. New developments suggest artificial atoms in silicon [34–36] to be another promising platform for PIC integration.

Single-photon emitters (SPEs) hosted in 2D materials [37–40] [hexagonal boron nitride (hBN), transition metal dichalcogenides like $WSe_2$ and MoSe, etc] are generated by applying strain to the material [41] or inducing defects [42]. The wavelength is determined by the choice of material [43] and can be also tuned by changing the strain acting on the flake [44]. The location of emitter formation is controllable by placing strain-seeds or by targeted irradiation [42, 45, 46]. Even though single-photon emission has been achieved in various experiments the confirmation of indistinguishability of those photons remains elusive due to spectral diffusion and wandering of the emitters [39, 47, 48]. A solution might be the integration in on-chip cavities using the Purcell enhancement to overcome the low optical coherence times induced by dephasing mechanisms stemming from phonon interactions [49, 50]. Further research in source engineering is needed to achieve Fourier-limited photons and performances comparable to state-of-the-art solid-state quantum emitters like QDs and defects in diamonds [51, 52].

Despite their low intrinsic emission rates due to long-lived states, rare-earth ions [53] in crystals show promising applications in quantum memories when interfaced with single photons. Placing them in cavities coupled to a waveguide would be an ideal system to enhance the spontaneous emission rate and achieve near-unity coupling efficiencies ($\beta$) into the waveguide.

Single-wall carbon nanotubes (SWCNTs) show large excitonic binding energies and light emission over a broad wavelength range [54] from the near-infrared up to the telecom O-band, even allowing for the observation of room-temperature single-photon emission [55]. Interfacing SWCNTs with plasmonic nano-antennas at cryogenic temperatures, exploiting cavity quantum electrodynamic effects, even made it possible to show the emission of indistinguishable photons in the telecom O-band [56].

Single molecules based on polycyclic aromatic hydrocarbons: terylene (Tr), perylene, dibenzanthantrene (DBATT), and dibenzoterrylene (DBT), are another group of promising SPEs [57]. Tr molecules have shown a near-unity quantum yield [58]. While on more recent years, single-photon purity as low as 0.003 on DBATT molecules [59] and 20% coupling efficiencies between SiN waveguides and DBT molecules [60] have been demonstrated.

Finally, colloidal QDs are another group of auspicious SPEs. Colloidal QDs are formed by pieces of semiconductor crystals in the nanoscale regime, which are protected by an outer layer of ligands. This outer layer or shell allows them to disperse stably inside a solvent. Single-photon purity values as low as 0.004 have been shown for CdSe/ZnS colloidal QDs [61]. A compressive review of their properties and fabrication methods can be found in reference [62].

## 2. Overview on state-of-the-art integration methods

After a quick introduction to possible integrable quantum emitters, we give a thorough elaboration on the three main integration methods and compatible emitter platforms, as well as their limitations.

### 2.1. Monolithic integration

A straightforward approach to integrate SPEs into PIC is to fabricate the circuits out of the material hosting the emitters [63], also called monolithic integration (see figure 1 (left)). The emitters are either randomly induced across the sample [64–67] or generated at predetermined locations (site-controlled generation) [68–70]. Subsequently, photonic structures are fabricated around those SPEs to, e.g., tune their spin properties [22], increase their brightness [68, 71], or analyze their single-photon properties, i.e., purity or indistinguishability [72] on chip.

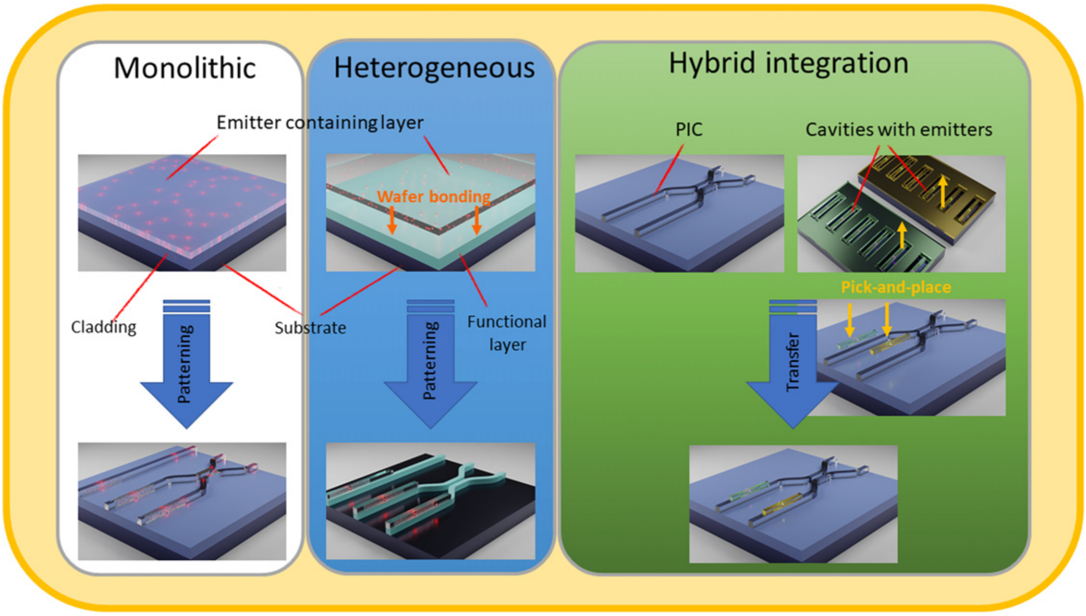


**Figure 1.** (Left) Monolithic integration approach. Quantum emitters are already implemented in the host material which later serves as the PIC. A direct lithography step is carried out and the PIC is transferred to the substrate via etching. (Middle) Heterogeneous integration approach. An emitter-containing layer is brought into contact with a functional layer that serves as the PIC after the fabrication (WB). Several fabrication steps are carried out to pattern the emitter-containing layer and the functional layer. (Right) Hybrid integration approach. The PIC and emitter-containing photonic structures are created on separate substrates and combined by transfer techniques.

#### *2.1.1. Compatible platforms*

Prominent examples of monolithic integrations are color centers in diamond and silicon carbide [22, 69, 71, 73, 74]. New developments of SPEs in silicon nitride [75] and G-centers in silicon [34–36], expand the material list where monolithic integration might be or is possible, respectively. Monolithic integration also has been demonstrated fabricating free-standing hBN circuits combined with subsequent emitter generation by an annealing process [64]. QDs fabricated on the InAs/GaAs platform have been extensively used as quantum emitters for PIC fabrication, enabling components like 50:50 beam splitters [76], cavities [77] and on-chip Hong–Ou–Mandel experiments [72].

#### *2.1.2. Limitations*

The most significant drawback in this approach is the limitation to one material platform and its optical properties. While some platforms exhibit large thermo-optical or electro-optical manipulation properties, others exhibit strong nonlinearities [63], which could be desirable to have on the same chip. During monolithic processing, random implementation of other emitters into the circuitry cannot be avoided in most emitter platforms resulting in photon scattering, re-absorption, and losses reducing the device performance. In addition, a few materials like diamond or SiC are rather difficult to process due to their chemical robustness, leading to rough sidewalls that can induce photon loss inside the PIC. That means working with only one material platform may prevent the development of high-performance devices.

### 2.2. Heterogeneous integration

In the heterogeneous integration approach, two or more material platforms that cannot be produced in one step before the circuit fabrication are brought into direct contact (see figure 1 (center)). The most prominent example of heterogeneous integration is wafer bonding (WB). One of the oldest integration methods designed and optimized to interface two materials, typically different semiconductors with silicon (Si) for electrical integrated circuits [78].

#### *2.2.1. Compatible platforms*

WB interfacing the Si platform with III–V semiconductors [79] has been successfully used to integrate single-photon sources (SPS) in PICs. An In(Ga)As QD-hosting layer was bonded onto a $Si_3N_4$ substrate. Afterwards, $Si_3N_4$ waveguides were produced and QD-containing nanobeams were fabricated aligned with the waveguide position, achieving optical coupling of single photons to the $Si_3N_4$ circuit up to 90% [80, 81]. To mitigate coupling losses between the two different material platforms another approach uses one material as the PIC cladding material and the wafer bonded SPS host material also as the waveguide core. This has been used to integrate 4H-SiC PICs on $SiO_2$ [74].

*2.2.2. Limitations*

WB relies on van-der-Waals forces as a prebonding step for the wafers. This step requires flat and cleaned surfaces before bringing them into contact. The formed bond is later strengthened either by an annealing step at high temperatures $> 700\,^\circ$C or if the structure cannot withstand high temperatures by more modern low or room temperature methods: plasma-activated bonding and ultraviolet-activated bonding. For a comprehensive review of these and other methods please check reference [82].

### 2.3. Hybrid integration

We define hybrid integration as a method where two or more devices are independently fabricated on different platforms and later integrated on the same chip (see figure 1 (right)). In general, this method allows for the realization of a large set of functionalities on hybrid integrated circuits, since each individual component can be independently optimised [83].

For hybrid quantum emitter integration one method is drop-casting SPEs in a solution on a PIC. Drop casting is a straightforward hybrid integration method. In this process, the SPEs are initially contained within a liquid solution and later deposited on top of the substrate or PIC by spreading a droplet of the solution. This method has the main drawback of random deposition of the SPEs on top of the PIC surface resulting in an inhomogeneous concentration of SPEs and probabilistic placement of the emitters. This last issue can be circumvented by engineering the PIC in such a way the solution containing the SPEs gets trapped before evaporating the solvent, therefore giving reproducibility to the placement of the SPEs on the PIC. In the case of carbon nanotubes, the drop-casting method has been used to deposit the SWCNT's on a specific position of the PIC. This is achieved by applying an electrical field on the PIC to guide the nanotubes to the desired position by exploiting the polarizability of the SWCNT's [84, 85]. Different SPEs have already been integrated by this method, for example, DBT molecules on $Si_3N_4$ waveguides [60], DBT molecules on ring resonators coupled to $TiO_2$ waveguides [86], nanodiamonds in ring resonator [87], hBN flake on $Si_3N_4$ waveguides [88], carbon nanotubes into waveguides [89] and ring resonators [90] and colloidal QDs into tantalum pentoxide waveguides [91]. Nonetheless, for higher yield and better positioning accuracy the pick-and-place method for hybrid SPE integration has been successfully developed (see figure 1 on the right).

*2.3.1. Pick-and-place*

Pick-and-place is one prominent example of a hybrid integration method where the SPE and the PIC are fabricated on different platforms and brought together with the help of nano- or micromanipulators. Typically, tungsten [92] and glass needles [93], atomic force and scanning tunneling microscope (AFM/STM) tips [94, 95], or electrostatic [96] tips are used for the transfer process. Another approach is based on viscoelastic stamps typically made from polydimethylsiloxane (PDMS) or other low glas temperature polymers [97]. Performing the pick-and-place method with a PDMS stamp is also referred to as transfer printing in the literature.

***2.3.1.1. Compatible platforms*** Tungsten needles have been utilized to transfer individual SPEs embedded in nanowire structures for waveguide integration [98] or to transfer multiple microbeam-cavities containing heterogeneous SPEs onto PICs [99]. A near-unity theoretical emitter-to-PIC coupling efficiency, considering the dipole orientation with respect to the PIC and resulting losses, is predicted for PDMS stamp transfer of QDs embedded in photonic crystal cavities [100]. Glass needles have been used to pick up semiconductor photonic trumpets [93]. While AFM and STM tips have been employed with [95] and without electric potential [94] to arrange nanodiamonds on PICs. The transfer printing method is extensively exploited for 2D materials [46, 101], where multiple SPEs are generated with one transfer. Even large-scale deterministic creation of emitters in 2D materials has been shown by, for example, transfer printing tungsten diselenide $WSe_2$ onto an array of micropillars [45, 46]. Furthermore, a transfer method based on a thermal release tape approach has been developed providing large-scale transfer of thin membranes [102]. The wide range of successful applications of pick-and-place techniques demonstrated a high degree of positioning control [98, 103, 104] and large-scale integration [99], making the pick-and-place methods indispensable tools in the state-of-the-art fabrication of hybrid quantum photonic circuitry.

***2.3.1.2. Limitation*** The transfer process is labor-intensive. Microscopic structures must be found and aligned with the transfer device. The surface quality of the sample is here as crucial as in the case of WB since contamination will interfere with the van-der-Waals or electrostatic forces between the different platforms.

### 2.4. Overview of quantum emitter integration approaches

In this section, we compare a large variety of integration methods and suitable quantum emitters. We categorize them into random and deterministic integration approaches. Typically, random integration allows for

**Table 1.** Categorization of integration methods for emitters with respect to scalability.

| Integration method | Emitter type | Yield | Large-scale | Scalability | Challenges |
|---|---|---|---|---|---|
| Drop casting (random) | SWCNT [89, 108] | Low | Yes | No | All: intrinsically not scalable due to the poor reproducibility of the emitters placement. |
| | Molecules [60] | Low | Yes | No | |
| Pick-and-place (random) | 2D materials [101, 109] | High | Yes | Yes | All: due to the randomness of the process the emitter properties are not guaranteed. |
| | hBN [110] | High | Yes | Yes | |
| | Rare-earth ions [113] | Low | Yes | No | |
| | QDs [97, 100, 104] | Low | Yes | No | |
| | NV-centers in diamond [99] | Low | Yes | No | |
| Monolithic (random) | NV-center in diamond [73] | High | Yes | Yes | All: since the integration is monolithic the usability of the devices is limited. Randomly placed emitters in the wave guides introduce high photon losses. |
| | QDs [72] | High | Yes | Yes | |
| | SiC-color centers [114] | High | Yes | Yes | |
| | hBN [115] | High | Yes | Yes | |
| | G-centers in silicon [34–36] | High | Yes | Yes | |
| Monolithic (deterministic) | SiV centers in SiC [69, 70] | Low | Yes | No | SiC: yield of emitter creation via ion implantation has to be improved. |
| | QDs [76] | High | No | No | QDs: well-performing site-controlled QDs have to be produced. Pre-characterization is time-consuming. |
| WB (random) | QDs [80] | High | Yes | Yes | QDs: poor SP properties. It was proposed in [80] to lower the density of QDs and employ a site-controlled QD technique. This would also result in a higher yield. |
| | SiC-color centers [74] | Low | Yes | No | SiC-color centers have poor yield. To achieve a higher yield it was proposed in [114] the use of a focused ion beam to irradiate the sample. |
| Dropcasting (deterministic) | hBN [88] | Low | No | No | All: needs further control over the number of deposited emitters. |
| | Colloidal QDs in nanobeam cavities [116] and waveguides [91] | High | Yes | Yes | Colloidal QDs: 80% placement yield and 48% of that show single-photon emission [91]. |
| | SWCNTs [84, 85, 117, 118] | High | Yes | Yes | |
| | Nanodiamonds [112] | Medium | Yes | No | Nanodiamonds: Only 42% of the devices fabricated had the nanodiamonds placed correctly [118]. |
| WB (deterministic) | QDs [81] | High | No | No | Pre-characterization-based deterministic integration techniques are relatively slow. It is fast for prototyping but slow for large scale manufacturing. |
| Pick-and-place (deterministic) | QD nanowires [92, 103] | High | No | No | All: high-speed and high-precision microscopic placement has to be developed. |
| | NV-centers in nanodiamonds [95] | High | No | No | |
| | Carbon nanotubes [119] | High | No | No | |

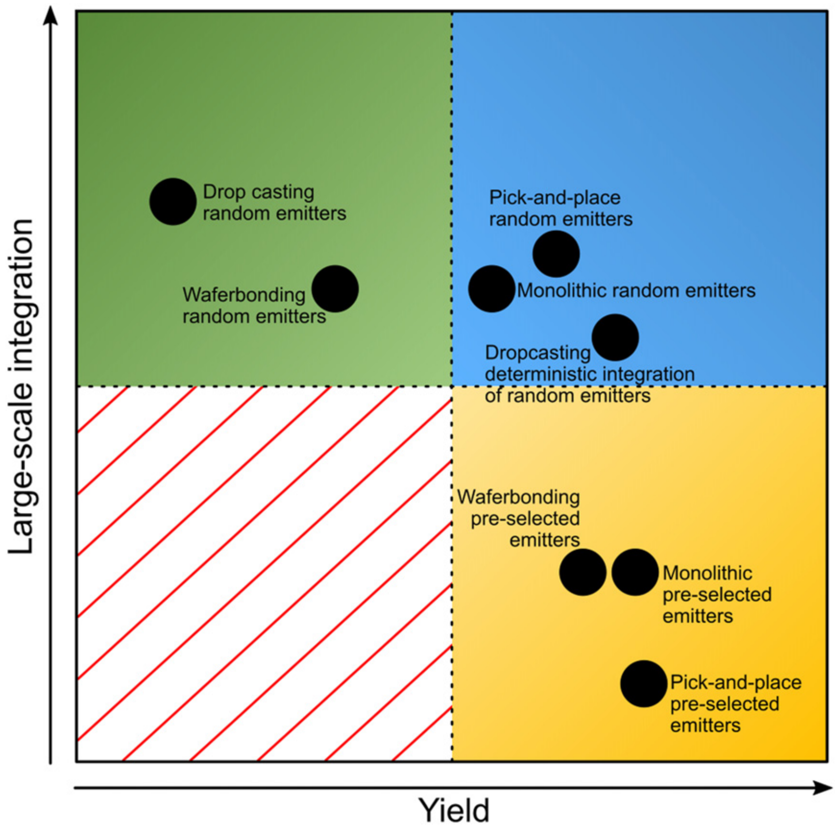


**Figure 2.** Map for ranking all different integration methods considering yield and large-scale integration potential. The red hatched area represents the region which is to avoid representing low yield and low potential for large-scale integration. Blue stands for the region with the highest scalability potential due to the possibility to achieve large-scale integration with high yield. The green region allows for research-oriented complex and fast prototyping, while the orange one supports the manufacturing of application-reliable prototypes.

scalability by sacrificing high yield, whereas deterministic approaches drastically increase the yield but are more time-consuming. In the past, many approaches have been developed to deterministically incorporate quantum emitters into various platforms compatible with PICs, such as precise ion implantation for emitter generation or deterministic lithography approaches based on emitter localization [105–107]. Currently, there is no ideal integration method for all emitter platforms, but some are more suitable than others when it comes to scalability. In table 1 we would like to address two requirements that are essential for scalable integration, namely high yield and large scale processing, which are challenging to achieve simultaneously. Scalability can only be achieved if large-scale processing is combined with a high production yield of properly working final devices.

So far, no integration platform has made it into a market-ready SPE-coupled PIC device. Currently, different solid-state quantum emitters require distinct approaches for integration. In the case of heterogeneous and hybrid integration, these often stem from (i) the poor optical properties of the quantum emitter host material as a circuit platform, preventing monolithic integration. (ii) Immature nanofabrication of the quantum emitter host material, making the monolithic large-scale circuit fabrication unfeasible. For the latter, new fabrication technologies might cause a paradigm shift enabling scalable integration of quantum emitters with high yield. Until then the community needs to continue to explore different routes for integration and further push the boundaries of nanofabrication.

In table 1 we stated challenges that different integration methods currently face to achieve large-scale integration of SPE in functional PIC devices. To overcome most of these challenges we need to (i) gain precise knowledge and control over the emitter position and spectral properties like photon indistinguishability, entanglement fidelity, spectral jitter, decay times, and many more depending on the application; (ii) ideally fabricate an ordered array of emitters with known properties enabling scalable interfaces with PICs or other optical devices since their geometry and properties can be tailored precisely with respect to the emitter characteristics.

Taking the information of table 1 into account, we present our current assessments of methods to realize scalable integration of quantum emitters into PICs in figure 2. We divide the methods roughly in four categories. The red hatched region represents emitter integration with low yield and no potential for large scale integration. This region should be avoided since it does not have any potential for scalability. However methods providing low yield, but large-scale emitter integration can be used for fast research-oriented complex prototyping in proof-of-principle experiments (green area). The orange region represents high integration yield, but lacks the potential for large-scale integration, but being useful for application reliable prototyping. Methods with high production yield and showing large-scale integration at the same time are represented by the blue region fulfilling the criteria for scalable emitter integration.

The ranking is a snapshot of the current state-of-the-art of integration methods with respect to potentials in scalability.

### 2.5. Conclusion

Based on our comparison we conclude that pick-and-place techniques are more suitable in the short run to deliver scalable quantum emitter integration. It enables devices that are not realizable via monolithic or wafer-bonding schemes. Currently, the way to go is to mix and match, rather than try to optimize a single platform, making sacrifices on performance. Thus, combining optimized photonic structures, such as nanobeam resonators containing embedded quantum emitters, with specifically tailored photonic circuits will be the integration method of choice for the coming years. This method is limited by a large time consumption but offers the highest performance with maximum reconfigurability. This is important when realizing different functionalities on a single chip, i.e. adding active circuit elements such as modulators or nonlinear optics, or single-photon detectors. Pick-and-place methods combine the best of quantum emitter research with the best photonic circuitry platform. Furthermore, it is not only limited to two different material systems. It gives the possibility to interface quantum emitters and memories from entirely different platforms, such as color centers in diamond or SiC, 2D materials, and QDs. This becomes especially interesting considering the telecom wavelength range where state-of-the-art telecom QDs could be interfaced with SiV centers in diamond or rare-earth ions as memories.

In summary, collective efforts from the quantum emitter communities and classical PIC platforms are still required to gain full control over the scalable and deterministic integration. Right now proof-of-concept demonstrators of complex integrated circuits are realized by coping with the huge overheads of transfer printing. To bring costs down and yield up in the currently prioritized hybrid integration methods, it is imperative to achieve higher transfer speeds and fabrication accuracies. In this regard, it will prove advantageous to pursue developments in site-controlled emitter fabrication and high-speed transfer methods. If these prerequisites prove to be elusive, we envision a shift away from hybrid integration methods favoring monolithic or heterogeneous integration to reach industrial fabrication standards.

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## Data availability statement

Data sharing is not applicable to this article as no new data were created or analyzed in this study.

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