SSCL-N-857

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April 1994
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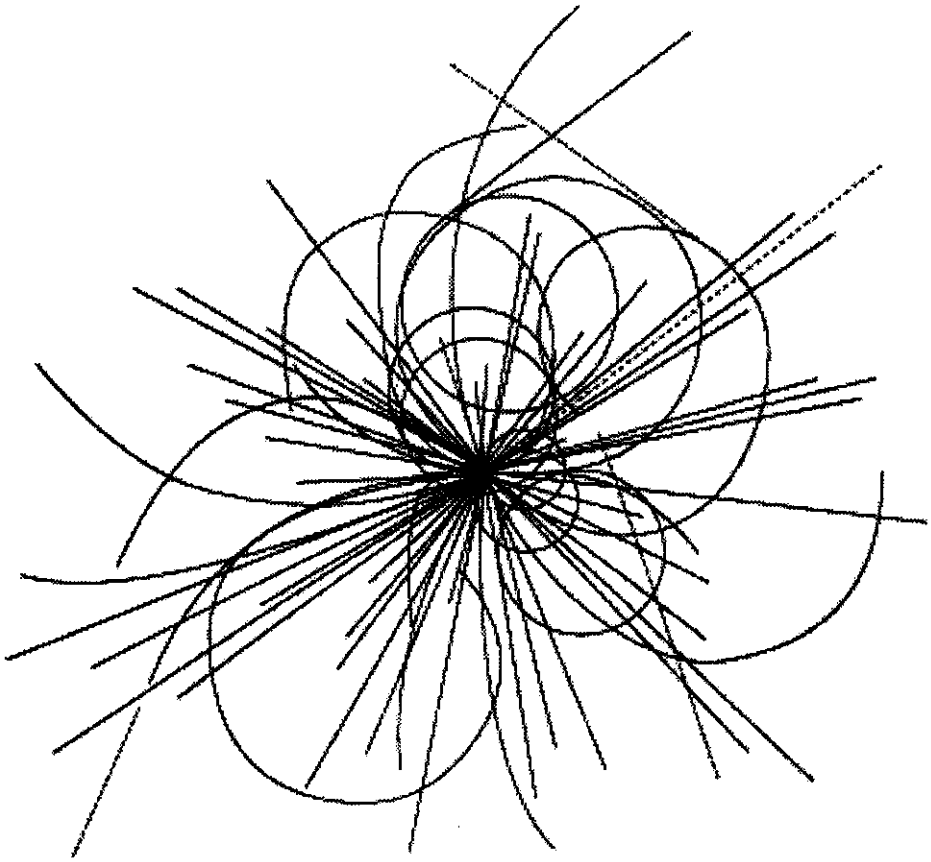
H. Nguyen

VME T1 Interface



Superconducting Super Collider
Laboratory

SSCL-N-857

VME T1 Interface*

H. Nguyen

Superconducting Super Collider Laboratory
2550 Beckleymeade Ave.
Dallas, TX 75237 USA

April 1994

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Superconducting Super Collider Laboratory
Accelerator Division
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Dallas, TX 75237-3946

Document/Records Submission Form

Title: VME T1 Interface

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Author(s) Title

Steve Hunt

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3) T1 Interface
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Content Description

This is the design of a T1 Interface using Industry Pack interface standard to handle the SSC site-wide distribution of all control system messages. The messages are assembled in the control room area and encapsulated for transmission via a T1 interface to devices distributed throughout the 70 miles of tunnel.

Remarks

Schematic design was captured on Racal-Redac ECAD software. All files are stored at bear.ssc.gov. Included photoplot.

Statement of Work for the

design and prototype production of a

T1 Industry Pack Interface

for the ASD Controls Department

Document Number ABA-1010005 Release 0

March 4, 1993

Approved By:

Steven Hunt
Group Leader
ASD Controls Communications

3/4/93
Date

Dave Gurd
Department Head
ASD Controls Department

3/4/93
Date

John Wentz
Section Leader
ASD Quality Assurance

3/4/93
Date

1 Introduction

1.1 Background

The Superconducting Super Collider (SSC) is a complex of proton accelerators presently under development by Department of Energy and the Superconducting Super Collider Laboratory (SSCL) in Ellis County, Texas. When complete the SSC will be the largest scientific instrument ever constructed.

The Controls department is responsible for the hardware, software and communication systems to control each of the six accelerators in the SSC complex, as well as for the integration of these accelerators into a functioning whole capable of meeting the needs of the experimental physics facilities.

Due to the complexity of the research and development effort for the SSC, University Research Associates, the prime contractor for the SSC, has determined that it is necessary to subcontract certain research and development tasks.

1.2 Objective

This statement of work (SOW) addresses the requirements of the ASD Controls Department for the design and prototype production of a T1 Industry Pack Interface.

2 Scope

The principle tasks under this subcontract (itemized below) are studies towards a design for a T1 network interface. The contractor shall provide all personnel, equipment, facilities and services necessary to perform the tasks listed in this SOW.

3 Requirements

3.1 Requirements Definition

The sub-contractor shall design a T1 Industry Pack with the following features.

- Single height Industry Pack conforming to the Greenspring IndustryPack (IP) Logic Interface Specification.
- Shall conform to the attached functional description and block level diagram.
- Use 16 Bit data path option including ID, memory, I/O and interrupt acknowledge cycles.
- Hardware and software compatible with MVME-162 IP carrier PCB.
- Employ Brooktree T1 chipset (R8069B, R8070A and R8071A) with all registers being accessible from the CPU.
- Have 1 M byte on board usable dual port static random access memory, plus a channelized interrupt status FIFO.
- Shall use a single interrupt line with a programmable interrupt vector register.
- Memory shall be accessible as up to 64 K bytes per channel.
- Capable of operating as channelized (24 DS0), hyperchannel or T1 mode.
- Provision of a PROM to hold 32 bytes of identification information accessible from the CPU.
- Register addressing memory map compatible with the attached specification.

3.2 Deliverables

- Documentation as specified bellow
- Two working prototype modules.
- Four unpopulated Printed Circuit Boards.

3.3 Documentation of Contract Results

Documentation delivered under this contract shall include

- Full schematics on hardcopy and magnetic media.
- PCB layout on film and Magnetic media

- Drill tape or Disk.
- Source level listings of any programable devices with description of operation.
- Description of circuit operation.

3.4 Project Management

The sub-contractor shall appoint a single task manager to have overall responsibility for the planning and execution of each task. This individual shall be responsible for all program management, budgeting and reporting requirements defined below. The individual assigned as the task manager shall be named and SSCL notified of the selection within 15 days of task initiation.

4 Special Considerations

SSCL may choose not to support increases in cost beyond the amount stated in the purchase order or to terminate the work prior to completion. In the event that the SSCL determines not to continue the work by the sub-contractor, the sub-contractor shall immediately deliver all sketches, designs, drawings, software media and documentation, tooling, fabricated parts and assemblies, and other incidental materials to the SSCL, who may elect to have the work completed by others or to complete the work at SSCL.

All designs carried out under this contract shall be the property of the SSCL.

5 Period of Performance

The period of performance is from 1 March 1993 until 30 May 1993.

SSCL Controls Communications Group

T1

T1 is a Time Division Multiplexing Standard used throughout the data communications and telephony industry. It is a byte serial interface operating with a 125 micro second time–slot. Within this 125 micro second period, 24 bytes of data + 1 bit for synchronization are transmitted. The bit rate is therefore ((24 * 8)+1) / 0.000125 = 1.544 M bits per second.

T1 is used by the telephone industry to transmit digital telephone calls. Each voice circuit occupies one byte in each 125 micro second time slot. Thus a T1 can carry 24 phone calls.

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SSCL Controls Communications Group

The T1 Industry Pack Interface

The T1 Industry Pack Interface was designed as a high performance low cost way to interface VME computers to a T1 network.

The specification was written and an RFQ issued to industry for the design and prototype production. The RFQ was won by Comar Systek of Dallas, who have completed the contract and delivered a working prototype.

The card is a single height Industry Pack which uses the Brooktree chipset to provide up to 24 channelized links of 64 K bits. Each channel can use the HDLC protocol. The electrical interface is DSX-1, eliminating the need for an external DSU/CSU.

The card supports H11 Hyperchannels and 'flexible' hyper-channels, allowing a channel to consist of an arbitrary number of 64 bit channels. Click here to see a picture of the T1 Industry Pack.

Click here to get a zip file of the schematics.

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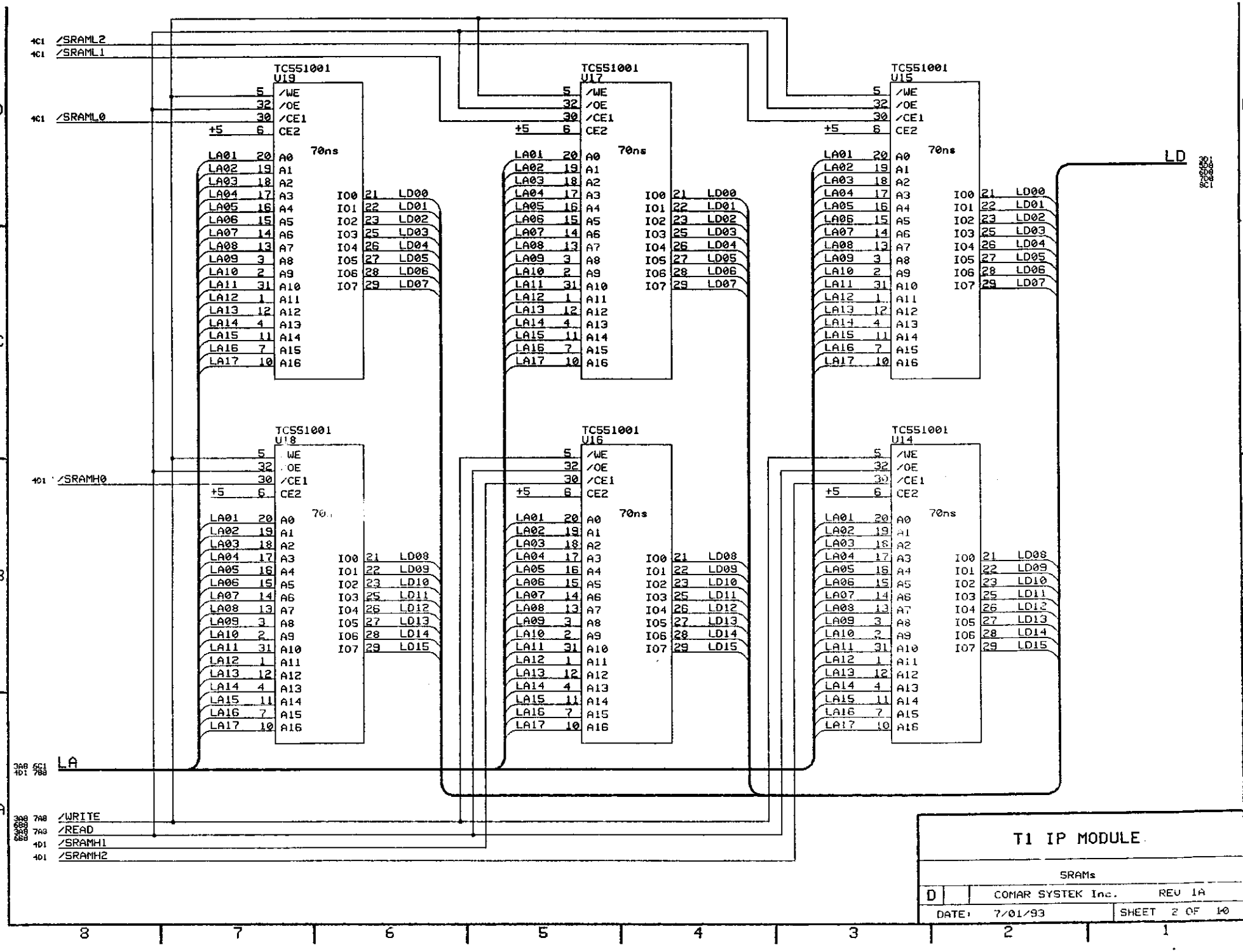
ADI - 88 or 13

D C B A

8 7 6 5 4 3 2 1

T1 IP MODULE

D		CONAR SYSTEK Inc.	REV 1A
DATE: 7/01/93			SHEET 1 OF 10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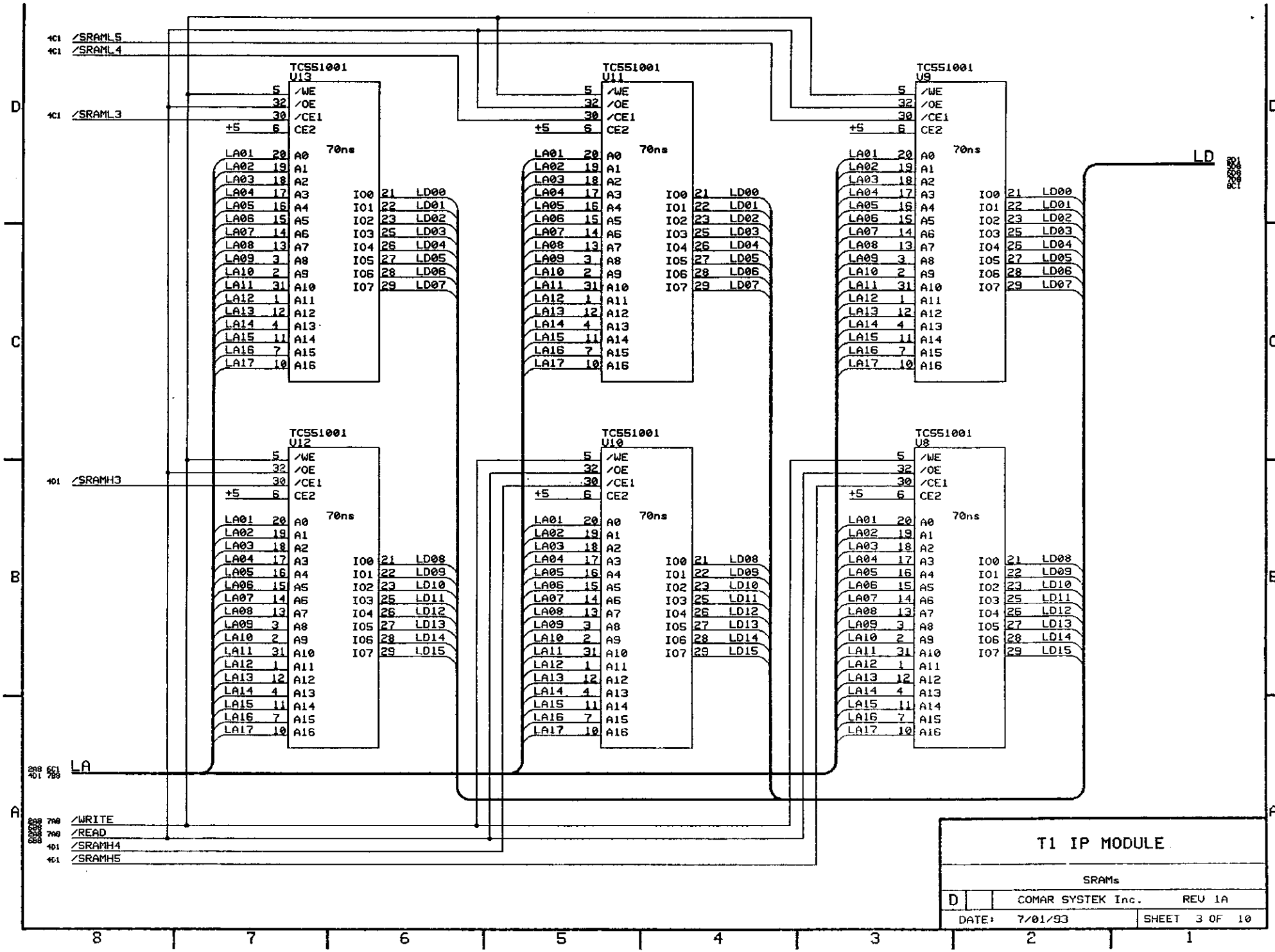
/SRAML1
/SRAML0
/SRAMH0
/SRAMH1
/SRAMH2
/WRITE
/READ
LA
LD
TC551001
U19
U18
U17
U16
U15
U14
/WE
/OE
/CE1
CE2
70ns
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
LD00
LD01
LD02
LD03
LD04
LD05
LD06
LD07
LD08
LD09
LD10
LD11
LD12
LD13
LD14
LD15
T1 IP MODULE
SRAMs
COMAR SYSTEK Inc.
REV 1A
DATE: 7/01/93
SHEET 2 OF 10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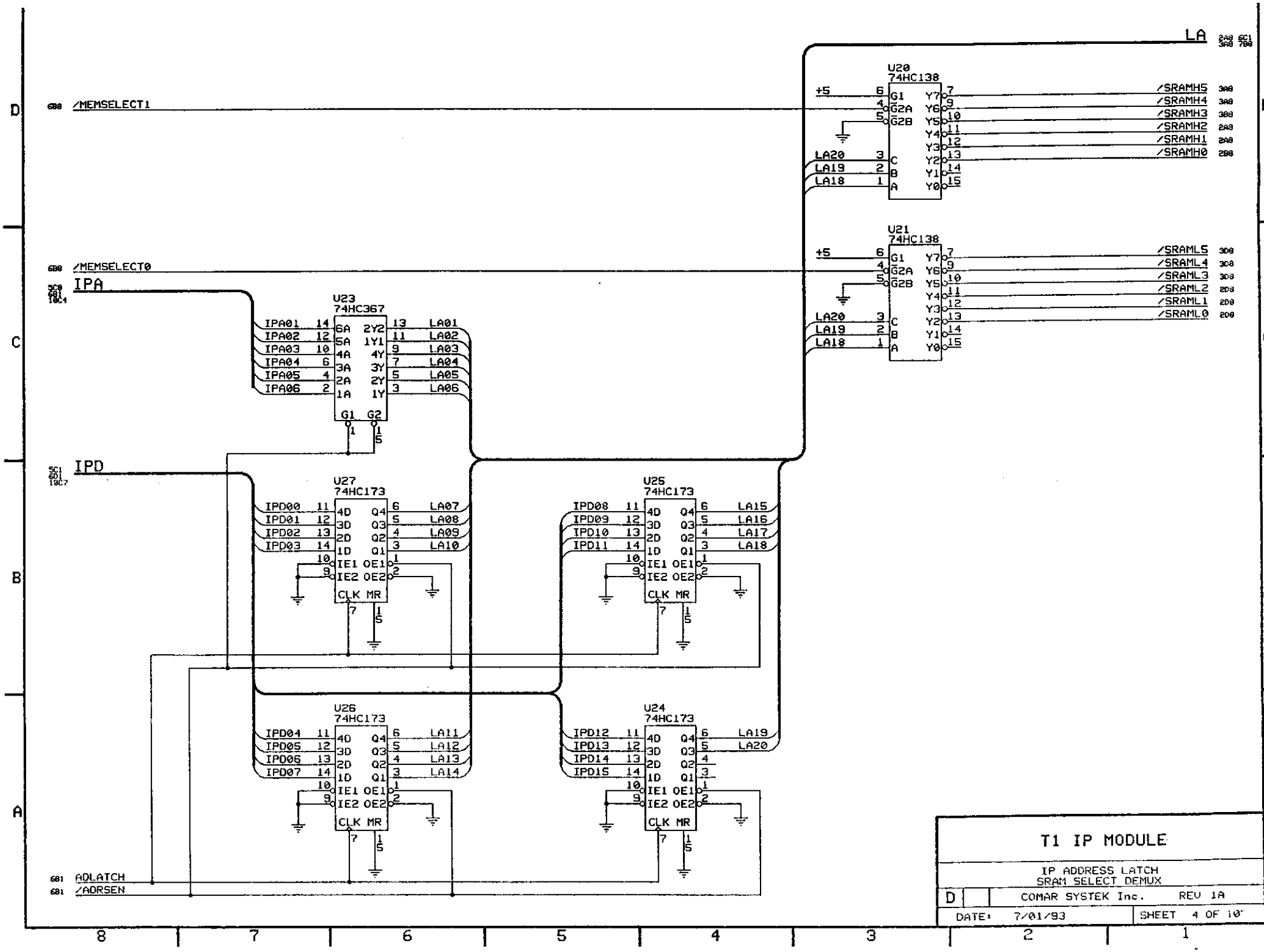
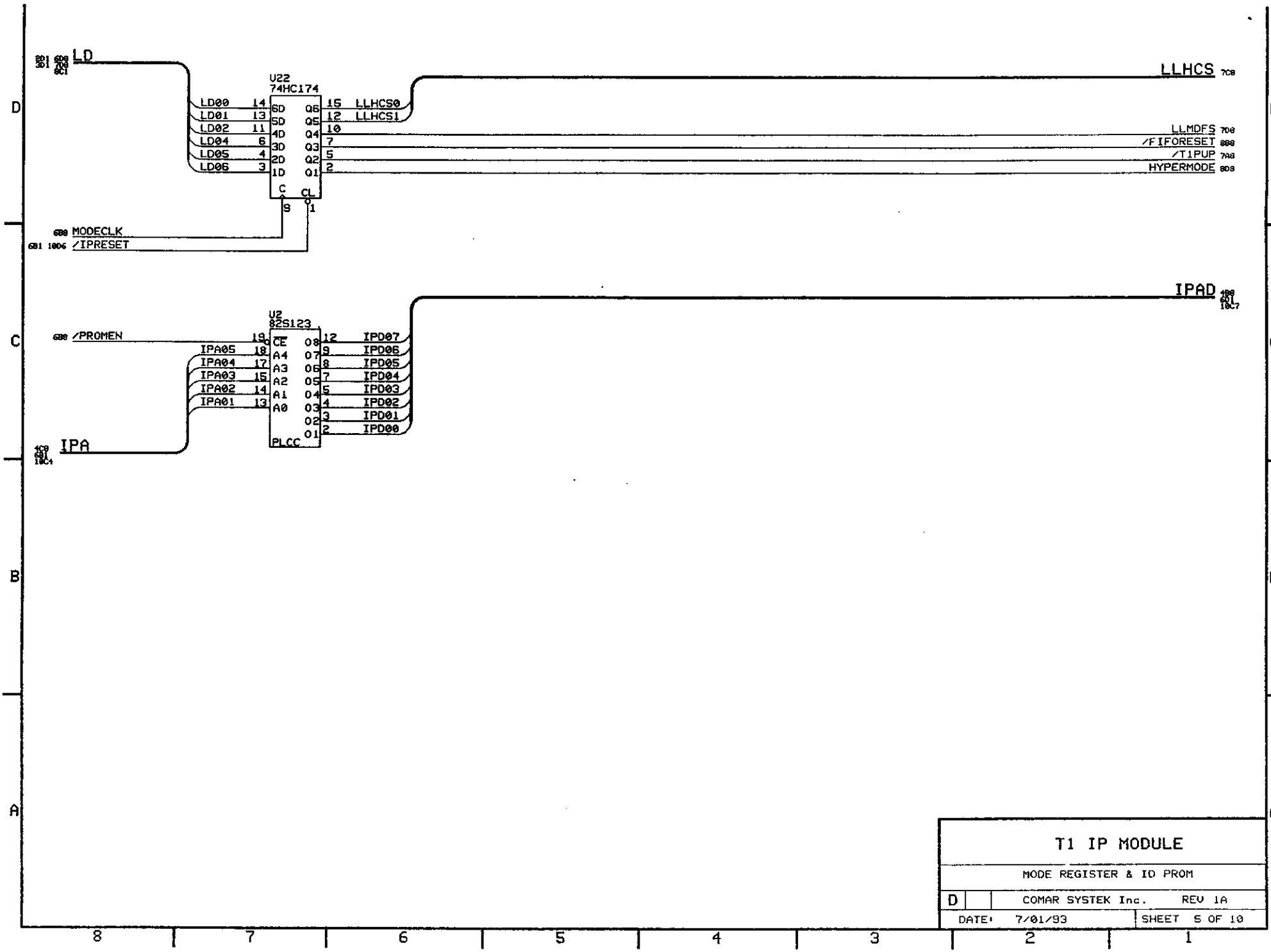
/SRAML4
/SRAML3
/SRAMH3
/SRAMH4
/SRAMH5
/WRITE
/READ
LA
LD
TC551001
U13
U12
U11
U10
U9
U8
/WE
/OE
/CE1
CE2
70ns
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
IO0
IO1
IO2
IO3
IO4
IO5
IO6
IO7
LD00
LD01
LD02
LD03
LD04
LD05
LD06
LD07
LD08
LD09
LD10
LD11
LD12
LD13
LD14
LD15
T1 IP MODULE
SRAMs
COMAR SYSTEK Inc.
REV 1A
DATE: 7/01/93
SHEET 3 OF 10


LA
/MEMSELECT1
/MEMSELECT0
IPA
IPD
U20
74HC138
U21
74HC138
/SRAMH5
/SRAMH4
/SRAMH3
/SRAMH2
/SRAMH1
/SRAMH0
/SRAML5
/SRAML4
/SRAML3
/SRAML2
/SRAML1
/SRAML0
LA20
LA19
LA18
U23
74HC367
IPA01
IPA02
IPA03
IPA04
IPA05
IPA06
LA01
LA02
LA03
LA04
LA05
LA06
U27
74HC173
U25
74HC173
U26
74HC173
U24
74HC173
IPD00
IPD01
IPD02
IPD03
IPD08
IPD09
IPD10
IPD11
IPD04
IPD05
IPD06
IPD07
IPD12
IPD13
IPD14
IPD15
LA07
LA08
LA09
LA10
LA15
LA16
LA17
LA18
LA11
LA12
LA13
LA14
LA19
LA20
ADLATCH
/ADRSEN
T1 IP MODULE
IP ADDRESS LATCH
SRAM SELECT DEMUX
COMAR SYSTEK Inc.
REV 1A
DATE: 7/01/93
SHEET 4 OF 10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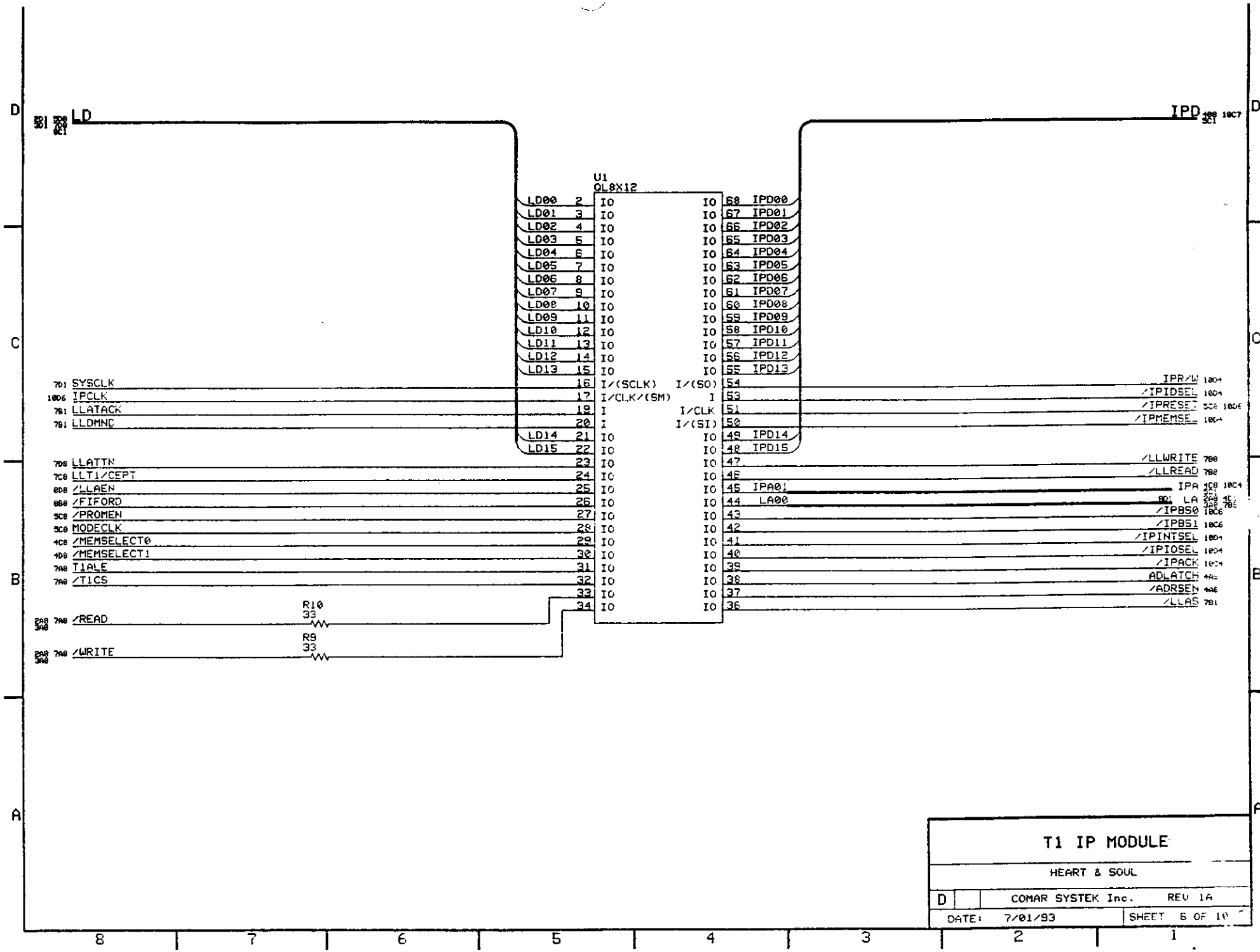
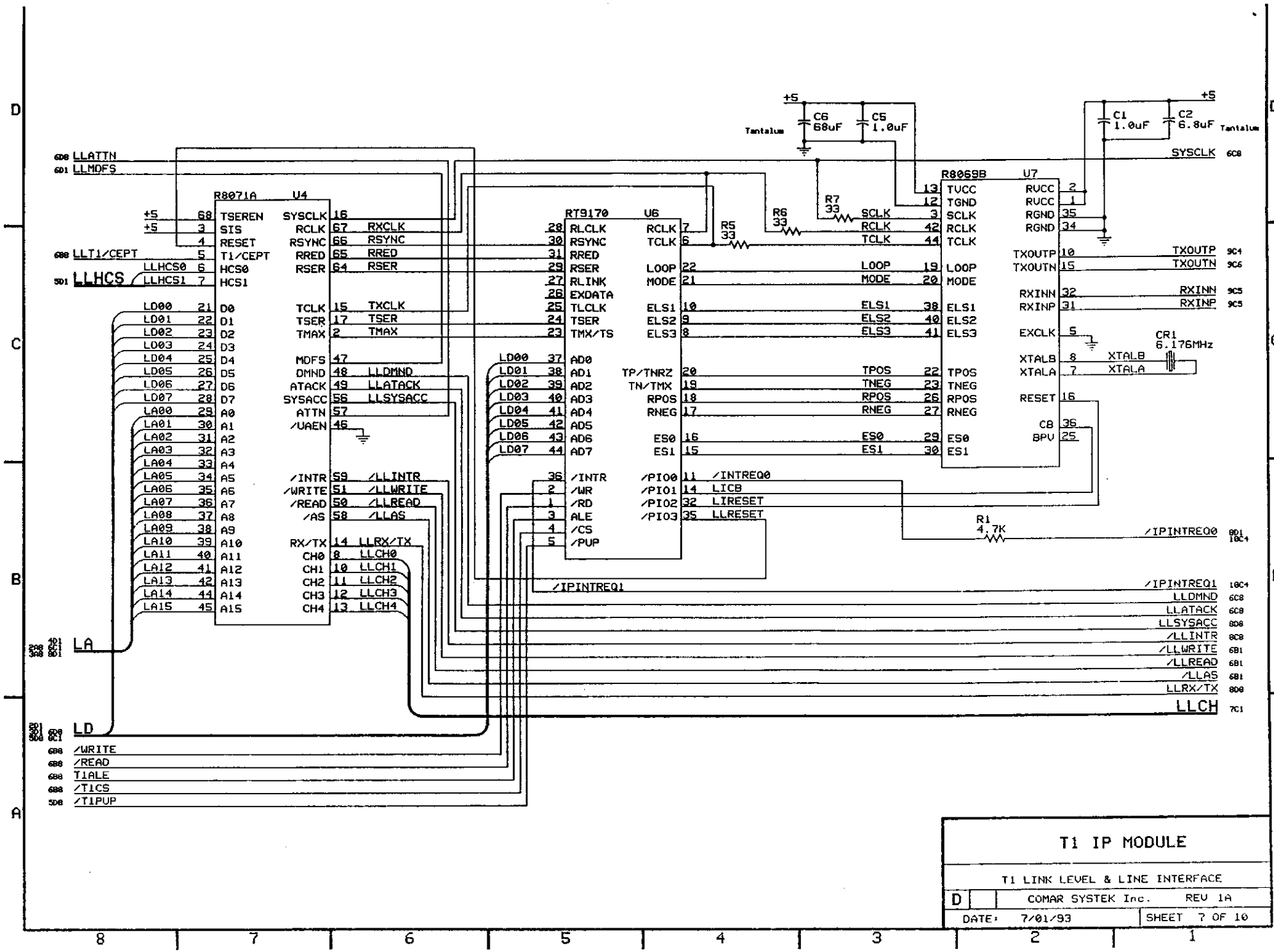
V22
74HC174
LD00 14
LD01 13
LD02 11
LD04 6
LD05 4
LD06 3
6D
5D
4D
3D
2D
1D
C
CL
9
1
Q6 15 LLHCS0
Q5 12 LLHCS1
Q4 10
Q3 7
Q2 5
Q1 2
LLHCS
LLMDFS
/FIFORESET
/T1PUP
HYPERMODE
MODECLK
/IPRESET
IPAD
V2
82S123
/PROMEN 19
IPA05 18
IPA04 17
IPA03 15
IPA02 14
IPA01 13
CE
A4
A3
A2
A1
A0
PLCC
O8 12 IPD07
O7 9 IPD06
O6 8 IPD05
O5 7 IPD04
O4 5 IPD03
O3 4 IPD02
O2 3 IPD01
O1 2 IPD00
IPA
T1 IP MODULE
MODE REGISTER & ID PROM
D
COMAR SYSTEK Inc.
REV 1A
DATE: 7/01/93
SHEET 5 OF 10


LD
IPD
U1
QL8X12
LD00 2 IO
LD01 3 IO
LD02 4 IO
LD03 5 IO
LD04 6 IO
LD05 7 IO
LD06 8 IO
LD07 9 IO
LD08 10 IO
LD09 11 IO
LD10 12 IO
LD11 13 IO
LD12 14 IO
LD13 15 IO
16 I/(SCLK) I/(SO)
17 I/CLK/(SM) I
19 I I/CLK
20 I I/(SI)
LD14 21 IO
LD15 22 IO
23 IO
24 IO
25 IO
26 IO
27 IO
28 IO
29 IO
30 IO
31 IO
32 IO
33 IO
34 IO
IO 68 IPD00
IO 67 IPD01
IO 66 IPD02
IO 65 IPD03
IO 64 IPD04
IO 63 IPD05
IO 62 IPD06
IO 61 IPD07
IO 60 IPD08
IO 59 IPD09
IO 58 IPD10
IO 57 IPD11
IO 56 IPD12
IO 55 IPD13
54
53
51
50
49 IPD14
48 IPD15
47
46
45 IPA01
44 LA00
43
42
41
40
39
38
37
36
SYSCLK
IPCLK
LLATACK
LLDMND
LLATTN
LLT1/CEPT
/LLAEN
/FIFORD
/PROMEN
MODECLK
/MEMSELECT0
/MEMSELECT1
T1ALE
/T1CS
/READ
/WRITE
R10
33
R9
33
IPR/W
/IPIDSEL
/IPRESET
/IPMEMSEL
/LLWRITE
/LLREAD
IPA
LA
/IPBS0
/IPBS1
/IPINTSEL
/IPIOSEL
/IPACK
ADLATCH
/ADRSEN
/LLAS
T1 IP MODULE
HEART & SOUL
D
COMAR SYSTEK Inc.
REV 1A
DATE: 7/01/93
SHEET 6 OF 10
8
7
6
5
4
3
2
1
A
B
C
D

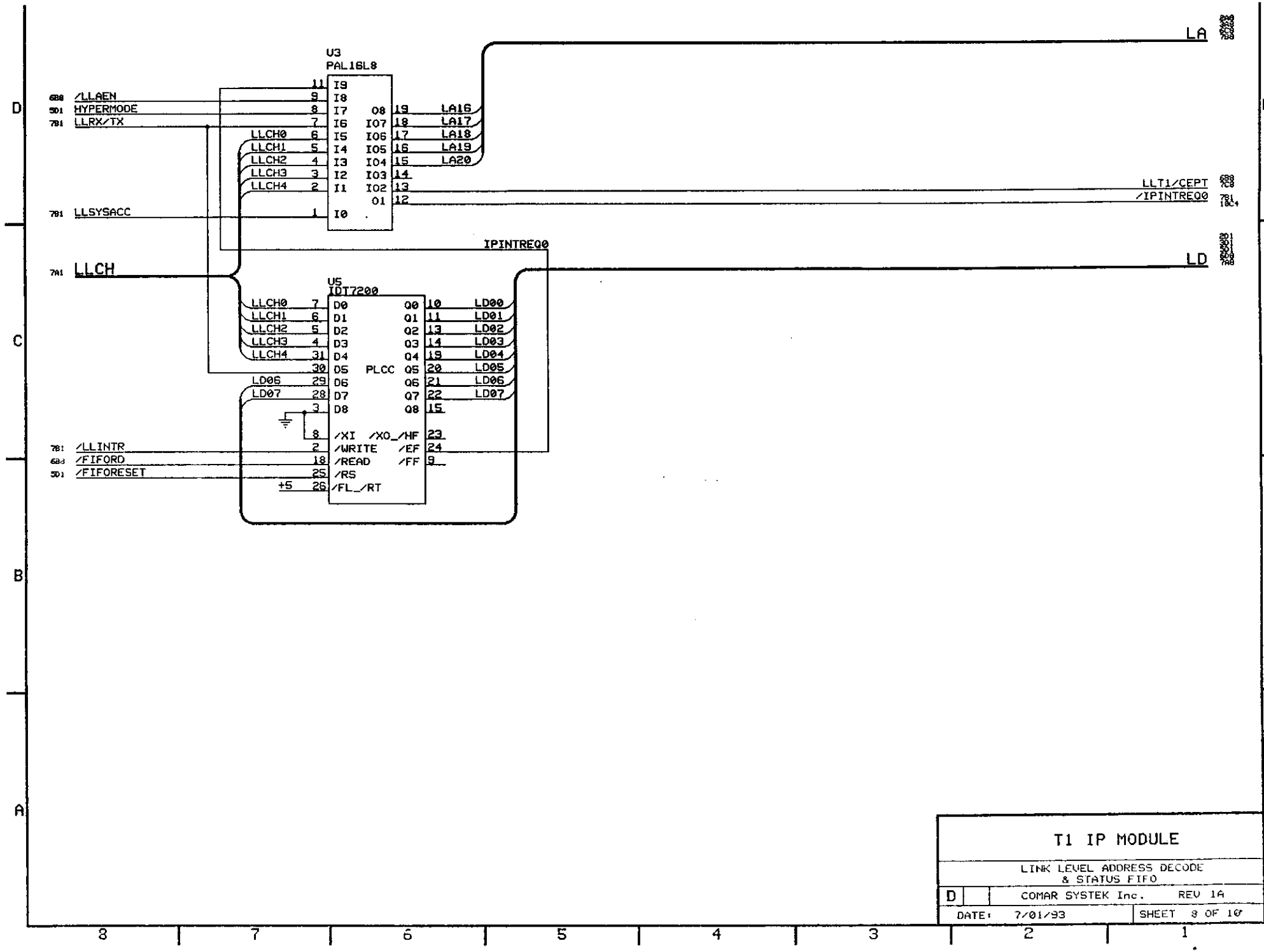


T1 IP MODULE

T1 LINK LEVEL & LINE INTERFACE

D | COMAR SYSTEK Inc. | REV 1A

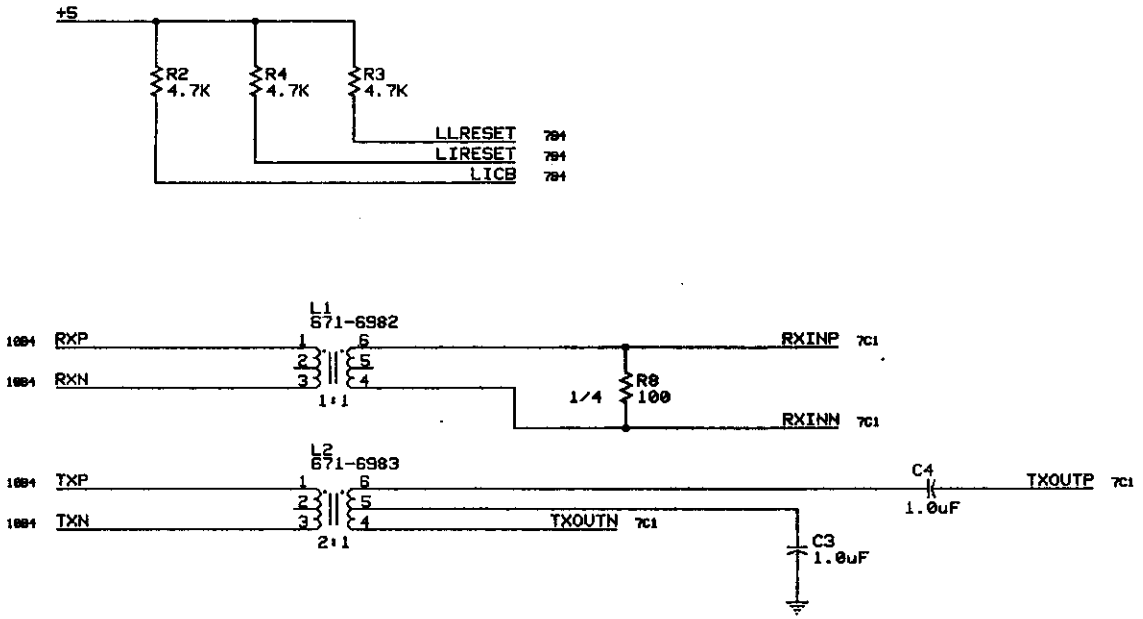
DATE: 7/01/93 | SHEET 7 OF 10



T1 IP MODULE

LINK LEVEL ADDRESS DECODE & STATUS FIFO

D	COMAR SYSTEK Inc.	REV 1A
DATE: 7/01/93		SHEET 8 OF 10

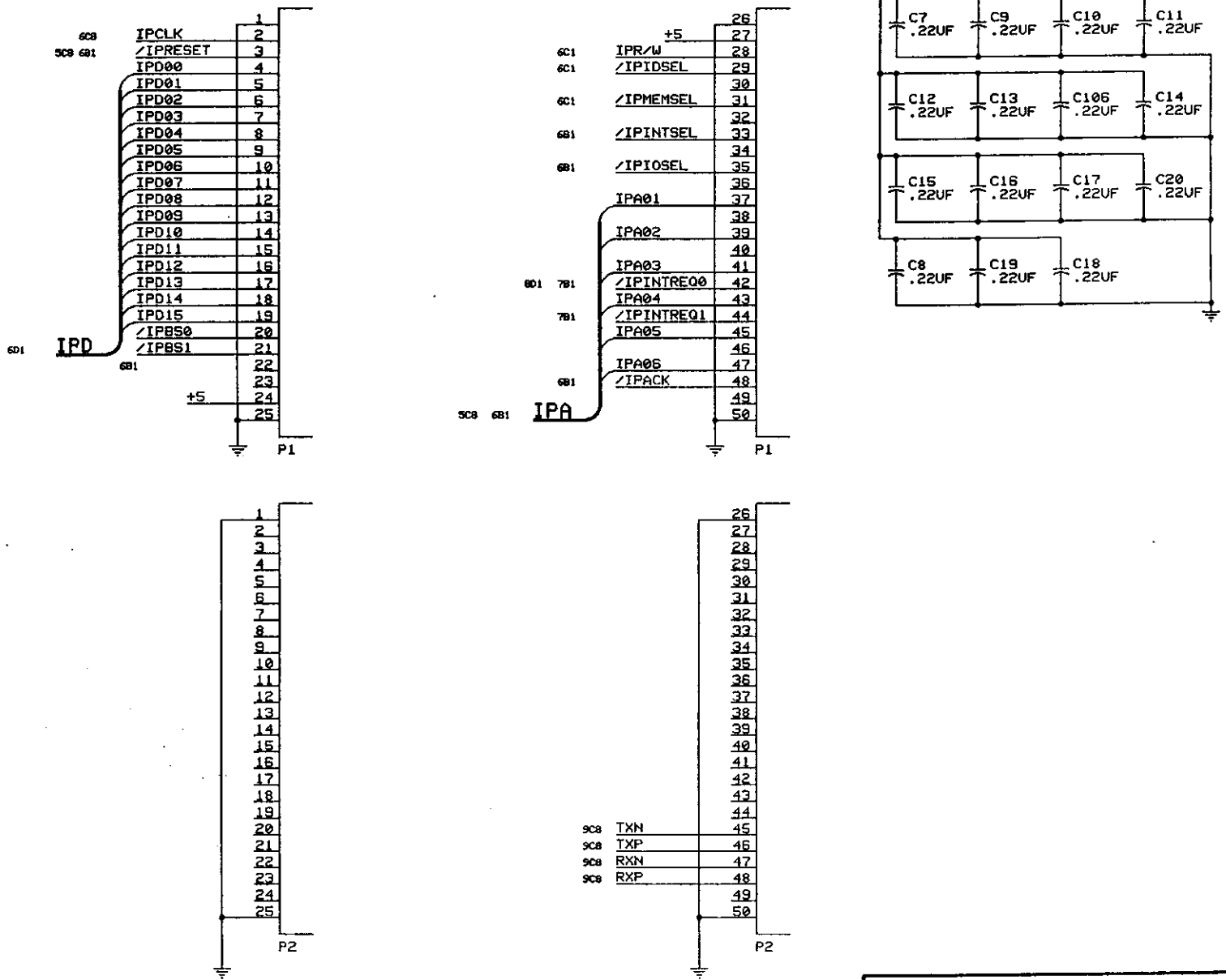


D							
C							
B							
A							
8	7	6	5	4	3	2	1

T1 IP MODULE

PULL-UPS & PULSE TRANSFORMERS

D	COMAR SYSTEK Inc.	REV 1A
DATE: 7/01/93		SHEET 9 OF 10



T1 IP MODULE

IP Bus Connector

D		COMAR SYSTEK Inc.	REV 1A
DATE: 7/01/93			SHEET 10 OF 10

LINE WIDTH .006

CAD

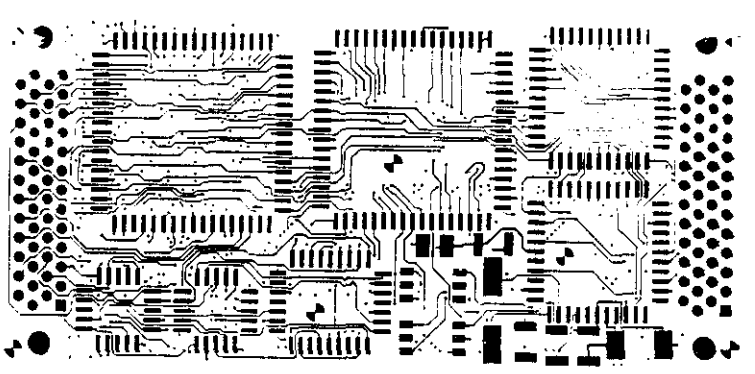
COMAR SYS. T1IP REV - 07/20/93

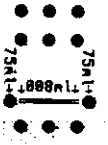
SOLDER SIDE

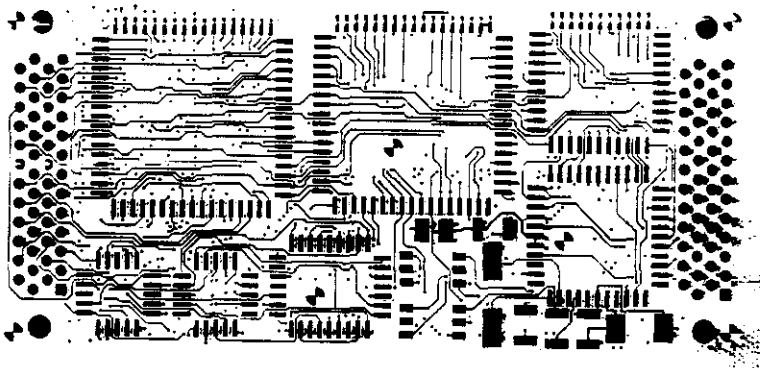
OMAR SYS. TIIP REV.- 07/20/93 Lay 1

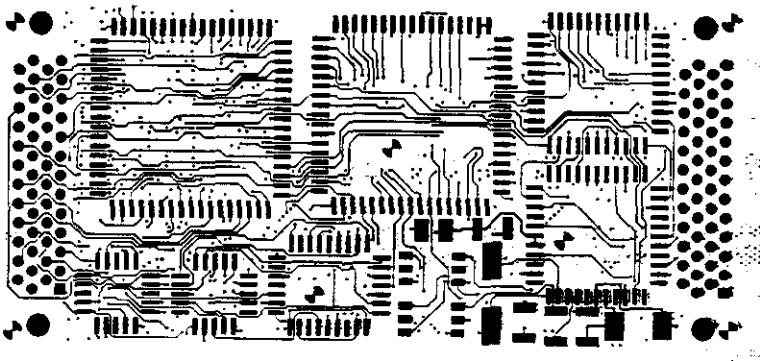
PONENT SIDE

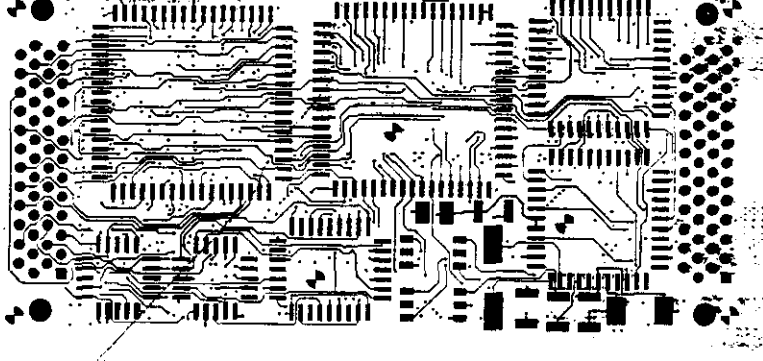
SCALE FOR FR-4











Superconducting Super Collider
Accelerator Systems Division
Controls Department
Communications Group
2550 Beckleymeade Ave., MS-4002
Dallas, TX. 75237-3946

December 6, 1993

MEMORANDUM

93 1200 E A 0405

To: Lee Graw

From: Steve Hunt

Subject: Licensing of T1 Industry Pack

I have received the record of inventions guidelines sent to me, I have filled it in as best I am able, and will return it. However I have a number of points that I would like to bring to your attention.

- This card is a communication interface, using a Time Division Multiplexing standard known as T1. This standard is in very wide use throughout the Telecommunications and Computer industry for the transmission of voice and data.
- Computer interfaces for this standard are available from a number of vendors. We ourselves have purchased T1 interfaces for VME bus computers from Rockwell CMC and PRI. The SSC required a large number of T1 interfaces (2000), the cost of purchasing this number of commercial VME boards would have been prohibitive. We therefore decided to develop our own lower cost interface.
- Industry Pack (IP) interfaces are computer Mezzanine cards conforming to the Industry Pack Specification published by Greenspring Computer. The concept behind this interface standard is to allow customization of computer systems at a lower cost than developing complete VME interfaces. IP interfaces are smaller and cheaper to produce than VME interfaces, VME CPUs and carriers are available from a number of vendors that support IPs. A variety of IPs have been developed by industry and other national labs.
- A specification was developed, and it was decided to have industry carry out the detailed design and build the first prototype. AN RFQ was issued (SSC-93-A-120393) with a statement of work (ABA-1010005), and the bid was won by Comar-Systek of Dallas. They have carried out this contract and delivered the first working prototypes.
- I believe they wish to develop further this design, (to make it cheaper to manufacture), and commercialize it themselves or through another company.
- The concept and design make use of standard and widely available techniques. The reason for this development and its status has been widely discussed within the Lab, and with some external organizations such as other national labs. The development has also been described at an international conference (ICALEPCS 93).

In view of the above, I do not know if this is classifiable as an invention, or if it is patentable. Perhaps you could also advise on the rights held by Comar Systek, and ourselves.

cc: Dave Gurd, Koni Nayak