Testing and Performance Analysis of 10 Gigabit Ethernet on Altera Stratix V FPGA

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Introduction

In the high-energy physics experiment a large amount of data are produced at a very high rate. With upgrade that will be taking place in ALICE experiment at LHC in 2018 after Long Shutdown 2, the data flow will be of about 1 TB/s [1]. There are a large number of front-end electronic channels associated with each high energy detector setup, resulting in a bulk amount of raw data generation. So, multiplexing of data turns out to be an important perspective of the project. After multiplexing, the concentrated data must be transmitted over high speed link. This high speed link can be custom defined or popular commercial link. But, if custom defined high speed link is used, it becomes a problem for interfacing with commercially available PCs, which support only popular interfaces. 10 Gigabit Ethernet is in a position to replace all these proprietary technologies as a next-generation interconnect [2]. Using multiple 10 Gigabit Ethernet link, the required 1 TB/s data flow can be achieved.

Testing Procedure for 10 Gigabit Ethernet

10-Gigabit Ethernet or 10GbE uses the IEEE 802.3 MAC (Media Access Control) sub layer. MAC is connected through a 10 Gigabit Media Independent Interface (XGMII) to Physical Layer (PHY) [2]. The details of these interconnections is shown in fig. 1.

For high speed 10GbE communication, error testing and performance analysis is of utmost importance. The testing of 10GbE communication is done in parts. MAC testing was done using internal Ethernet Loopback module, and transceiver testing was done using optical loopback. For performance analysis Eye Diagram[3] is used.

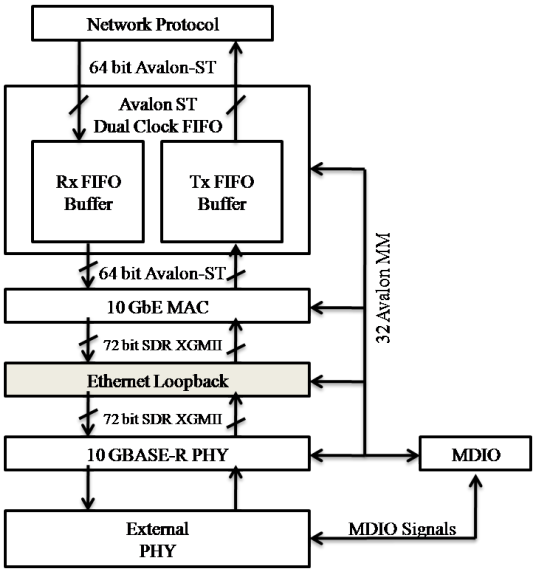

FIG. 1: 10GbE Design Block Diagram

Modular Design Approach for 10 Gigabit System Integration

The 10GbE design is a composition of three main blocks: (a) MAC receiver (MAC Rx) and MAC transmitter (MAC Tx); (b) 10GBASE-R PHY and (c) MDIO (Management Data Input/Output); as shown in fig. 1. The MAC Rx and MAC Tx handle data flow between the client and Ethernet network. The 10GBASE-R PHY handles the physical coding and medium attachment sub layer [2]. While MDIO is a serial interface to connect a Station

Management entity and a managed PHY for providing access to management parameters and services. Apart from these three blocks there is a debugging block, i.e. Ethernet Loopback block. It helps to check the functionality of MAC and PHY independently.

Loopback Testing

Ethernet Loopback block does two types of loopback, one is Local loopback and another is Line loopback. Apart from this there can be PHY level loopback, known as Serial loopback [5].

FIG. 2: Transceiver level loopback

When the local loopback is enabled, the Ethernet loopback module takes the transmit frame from the MAC XGMII Tx and loops it back to the MAC XGMII Rx datapath. During this cycle, the loopback module also forwards the Tx frame to the PHY, and ignores any frame received from the PHY.

When the line loopback is enabled, the Ethernet loopback module takes the XGMII Rx signal received from the PHY and loops it back to the PHYs XGMII Tx signal. During this cycle, the loopback module forwards the XGMII Rx signal to the MAC, and ignores any frame transmitted from the MAC.

When Phy-Level or serial loopback is enabled, the data from the FPGA fabric passes through the Tx channel and is looped back to the Rx channel, bypassing the Rx buffer. Single-Mode optical fibre is used for this loopback. Fig. 2 shows the test result of successful PHY level loopback, indicating the transceiver is working properly.

Eye Diagram Analysis

For successful multi-gigabit transceiver operation, noise level analysis is an important parameter. An eye diagram is a common indicator of the quality of signals in high-speed digital transmissions [3]. It is generated by overlaying sweeps of different segments of a long data stream driven by a master clock. The signal to noise ratio of this high speed data signal is directly indicated by the amount of eye closure, or Eye Height [4]. Fig. 3 shows eye diagram for this 10GbE transmission in low noise channel environment. EyeQ tool of Altera Transceiver Toolkit is used for capturing signal eye.

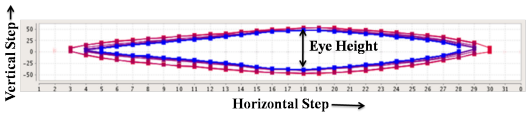

FIG. 3: Eye Diagram captured using EyeQ tool of Altera Transceiver Toolkit

Conclusion and future work

This entire analysis was done using Altera's 28-nm Stratix V FPGA chip. It is programmed using Quartus II 13.1 design software. The architectural layout was implemented using QSYS, the system integrator tool from Altera. A further detailed qualitative analysis is required for 10GbE communication, like throughput measurement.

References

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