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A family of transient recorder ASICs for detector readout

H. Flemming,* H. Deppe and P. Wieczorek

GSI Helmholtzzentrum für Schwerionenforschung GmbH, Planckstr. 1, 64291 Darmstadt, Germany

E-mail: h.flemming@gsi.de

Abstract: A set of highly integrated read out ASICs with a common digitising and data acquisition back end but different front ends is currently under development at the GSI electronics department. The concept consists in using an analogue transient recorder stage for an efficient application of the area and power consuming analogue to digital converter. A focus of these ASICs is the read out of detectors with a large dynamic range. Possible applications could be the electromagnetic calorimeter of the PANDA detector or the GEM TPC of the Super-FRS at FAIR.

Keywords: Front-end electronics for detector readout; VLSI circuits; Analogue electronic circuits

*Corresponding author.

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1 Introduction

The future experiments at the FAIR accelerator center have high demands on the read out electronics. Hadron spectroscopy as well as heavy ion tracking with a wide range of isotopes require a large dynamic range of $\geqslant 10^3$. At the same time the high luminosity requires a reasonable good time resolution in the order of a nano second to disentangle single events.

To address these requirements a set of read out ASICs with a common back end architecture currently is under development at GSI. This architecture is based on an analogue transient recorder with succeeding analogue to digital conversion and digital signal processing.

This back end will be combined with different front ends. A differential input buffer [1] can be used to connect the ASIC with an external pre-amplifier while an integrated charge sensitive amplifier (CSA) with adaptive feedback [2] offers the possibility to read out detectors with this ASIC directly.

The main analogue and mixed signal components and their interaction have been tested on a first 4-channel-prototype [3]. The first full-scale prototypes were produced and delivered in December 2021 and will be characterised soon. In this paper the global architecture and the main components of these ASICs are presented.

2 Architecture

2.1 Global achitecture

Figure 1 shows a block diagram of the transient recorder ASIC architecture. The transient recorder consists of four blocks with four channels each. Each recorder block is connected with a four channel front end. Main component of the recorder unit is an analogue memory organised in 16 columns and 4 rows for each channel in order to provide four independent transient buffers per

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channel for derandomisation. The incoming analogue signal is sampled with up to 100 MS/s and written into the analogue memory in a cyclic manner. When a pulse is detected the write logic switches to the next row after a configurable delay and the state of a clock synchronous time stamp counter is stored for operation in a triggerless environment. This way the complete pulse transient is stored in the memory and can be read out asynchronously by a read out circuit consisting of 16 integrators and an analogue multiplexer. Afterwards the transient is digitised with a 33 MS/s, 12 bit pipeline ADC which is shared by the four channels. It is based on 1.5 bit pipeline stages with a self-calibrated digital correction logic for gain and offset errors similar to that in [4]. Dynamical measurements of the ADC yielded an effective number of bits (ENOBs) of 10.5 [3].

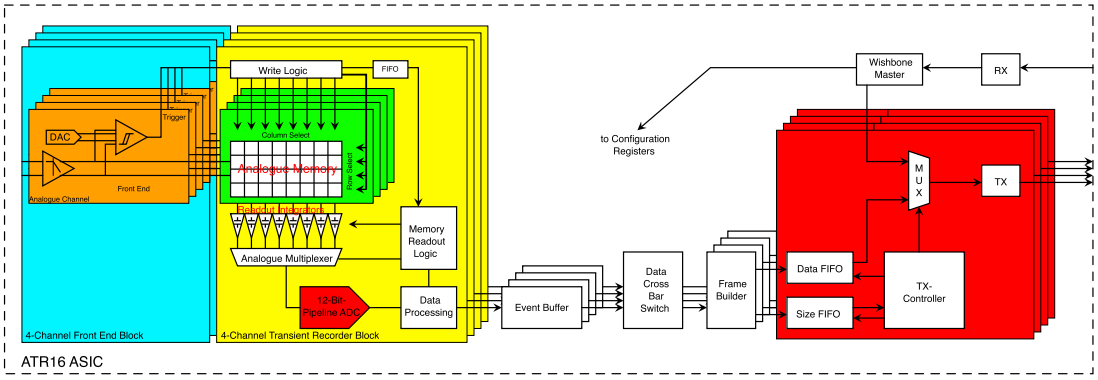

Figure 1. Block diagram of the transient recorder ASIC.

The four read out blocks are independent data sources. Given by the ADC speed for each block the raw data rate can reach up to 50 MByte/s for full occupancy which can be reduced to ≈7.9 MByte/s by on-chip data processing as it is described in section 3. The data are stored in event buffers of 512 Byte. In the triggered mode these buffers act as latency buffers, storing the events until a trigger selector checks whether the events are in the trigger window or not. After the buffer read out and trigger selector unit a cross bar switch allocates the data to up to four 500 Mbit/s serialisers.

For configuration register write and readout a single serial link with reduced bit rate ($f_{RX} = 1/8 f_{TX}$) is available. Acknowledge and register readout responses are feed in into the data stream. The hardware realisation of up- as well as downlinks are copper links on LVDS levels. The used communication protocol is a subset of the HDLC protocol. The overall power consumption depends on the integrated front end and the operating conditions and is expected to be in the order of 50 mW to 75 mW per channel.

2.2 Trigger

The first level trigger which controls the transient recording is part of the front end. While the integrated charge sensitive amplifier is equipped with a simple leading edge discriminator, the input buffer is combined with a more sophisticated trigger unit which additionally provides a trigger on the differentiated signal [1].

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In both variants at power up of the ASIC, a dedicated logic performs threshold scans of each channel to determine baseline position b and noise width w (FWHM) and sets the trigger threshold to $b \pm \alpha w$ with the programmable coefficient α. The CSA trigger unit in addition contains for baseline tracking in case of a baseline shift due to detector leakage currents a comparator comparing the CSA output with the nominal voltage. Depending on the comparator output the control signals of a reference DAC are set to correct the baseline.

The read out logic can be operated in a self triggered mode as well as in a triggered mode. In the self triggered mode all transients detected by the first level trigger are read out and sent to the data acquisition. In the triggered mode a trigger selector rejects all transients which are not in a defined time window around an external trigger signal.

3 Data processing

On-chip data processing is mainly motivated by the triggered mode. The deferred trigger selection requires event buffering of all events during the trigger latency. As the extracted amplitude and time information requires 6 bytes in comparison to 38 bytes of raw data the number of events that can be buffered can be increased by more than a factor of 6 by feature extraction. Therefore in a first step variances of the analogue memory cells have to be corrected.

3.1 Analogue memory correction

The analogue memory stores the input voltage V_i in a range of ±1 V on a capacitor $C = 1$ pF as a charge $q = CV_i$. During read out this charge is transferred to the read out integrators. So cell to cell variations of the capacitor cause slope variations of the analogue memory characteristics. In addition offsets might occur due to asymmetries in the differential memory cells and the integrators. Measurements of these variations by colleagues of the Helmholtz Institute Mainz [3] with the 4-channel prototype found slope variations of $\Delta S/\bar{s} = 2.2\%$ and offset variations of $\Delta b/\bar{b} = 6\%$ (see figure 2).

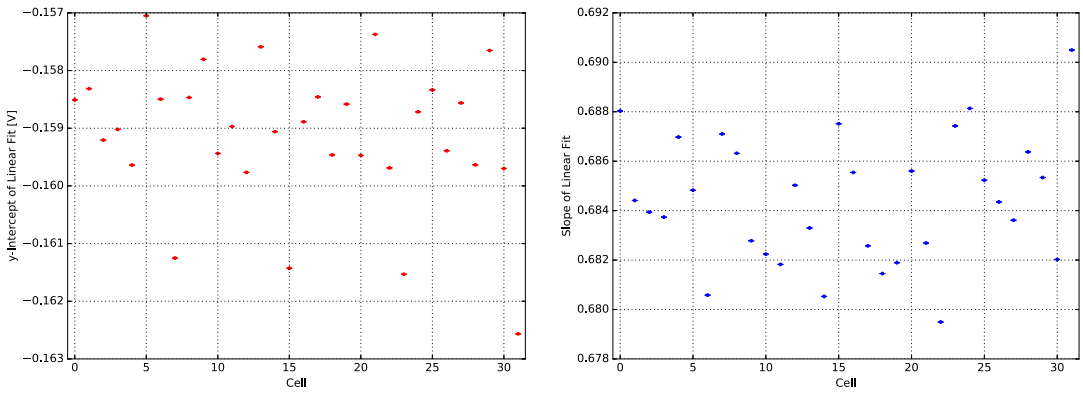

Figure 2. Variances of analogue memory cell characteristics measured on the memory array of the 4-channel-prototype. Offset on the left side and slope on the right side. Courtesy of Phillip Grasemann.

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As these variances are not acceptable for the aimed dynamic range the individual slope and offset of each memory cell has to be characterised for correction. Therefore DC traces can be recorded by connecting the memory input to a dedicated DAC and triggering the memory by software. From a set of traces with various DC levels the characteristics and therefore correction constants for slope and offset correction can be extracted. For On chip correction a correction logic determines the cell address for each sample by channel, row and column registers to fetch the correction constant from a dedicated memory. Then the slope correction factor is multiplied with the ADC value and an offset is added.

3.2 Feature extraction

In literature descriptions of feature extraction hardware implementations can be found [5, 6] using elaborated filtering algorithms requiring a continuous data stream. In difference to these implementations a dedicated feature extraction logic needed to be developed which can cope with short transients of 16 samples a_i. As shown in figure 3 from these samples differences $d_i = a_i - a_{i-1}$ are calculated. Comparators are used to detect the pulse start ($d_i > d_{\mathrm{thr}}$), the inflexion point ($d_i < d_{i-1}$) and the pulse maximum ($d_i < 0 < d_{i-1}$). By linear interpolation of the zero crossing of the differences or of the baseline crossing of a tangent at the inflexion point a sub-sampling interval fine time can be calculated.

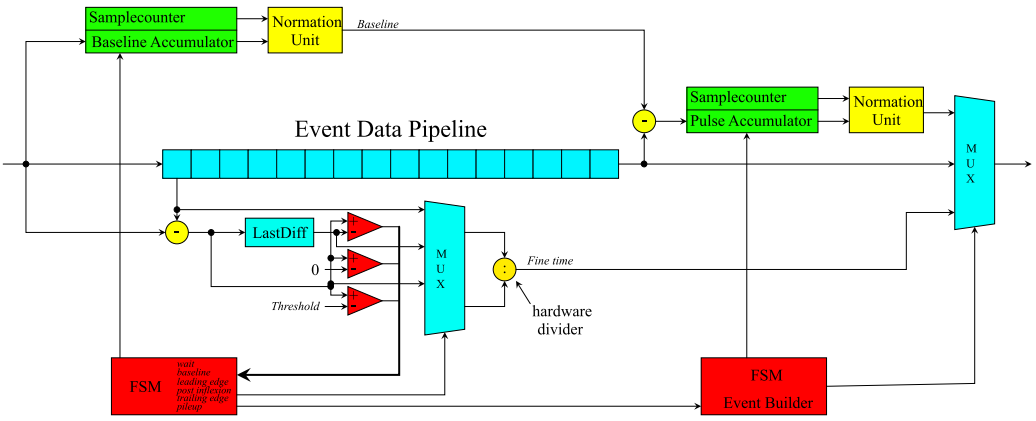

Figure 3. Block diagram of the feature extraction logic.

A finite state machine triggered by the comparators controls a baseline accumulator used for a pedestal subtraction and a pulse accumulator which is used to extract the pulse amplitude by calculating a window integral.

The hardware implementation supports a fine time precision of 6 bit and an amplitude precision of 16 bit and was tested in extensive simulations. Nevertheless as the ASIC is a generic device foreseen for different applications the obtained precision will strongly depend on the environment and configuration.

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4 Summary and outlook

The design of an analogue transient recorder ASIC with signal digitisation and data processing was described in this paper. Based on this generic architecture the design of two fully equipped transient recorder ASICs have been completed. Figure 4 shows the layout of the variant with fully differential input buffers. The chip was designed in the UMC 180 nm CMOS technology and contains more than 3 million transistors on 5 mm by 10 mm. Tape out of both ASIC variants was in October and delivery in December 2021. The next steps will be testing and characterisation of both chips.

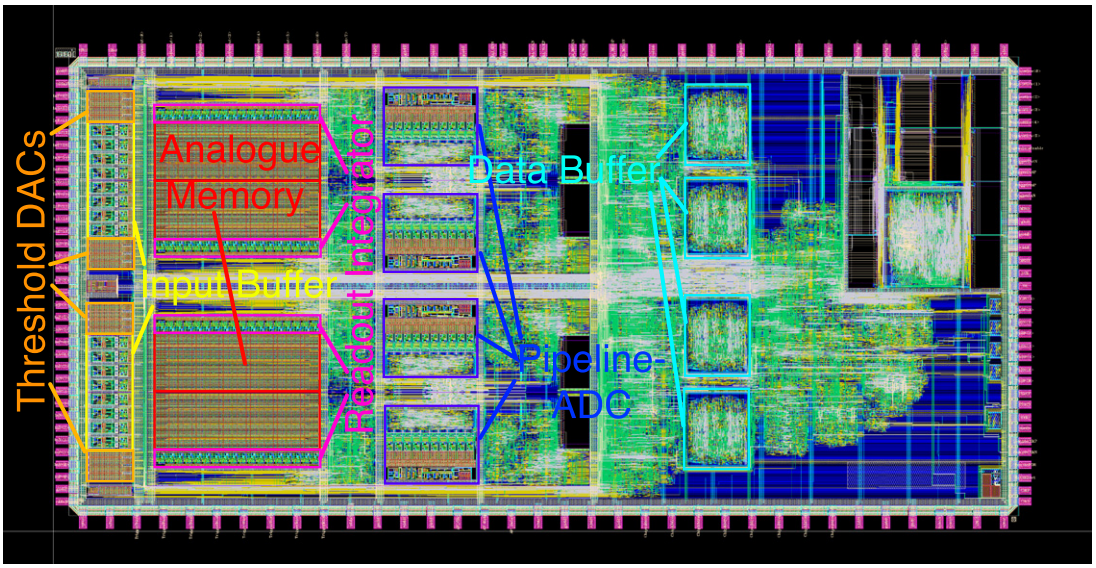

Figure 4. Layout of the transient recorder ASIC.

Potential applications are the PANDA EMC, the PANDA GEM tracker or the GEM-TPC at the Super-FRS at FAIR. Therefore detector tests with a calorimeter prototype and a GEM-TPC are planned for the next future also.

Acknowledgments

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