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Power-pulsing schemes for vertex detectors at CLIC

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ABSTRACT: The precision requirements of the vertex detector at CLIC impose strong limitations on the mass of such a detector (<0.2% of a radiation length, X_o, per layer). To achieve such a low material budget, ultra-thin hybrid pixel detectors are foreseen, while the mass for cooling and services will be reduced by implementing a power-pulsing scheme that takes advantage of the low duty cycle of the accelerator. The principal aim is to achieve significant power reduction without compromising the power integrity supplied to the front-end electronics. A current based power-pulsing scheme is proposed and its electrical features are discussed on the basis of measurements.

KEYWORDS: Voltage distributions; Pulsed power

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[2]On behalf of the CLIC detector and physics study.

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1 Introduction

The Compact Linear Collider (CLIC) is an electron-positron linear collider under development with a maximum centre-of-mass energy of 3 TeV [1]. It will complement the results of the LHC experiments and measure the properties of new particles with high precision [2]. Figure 1 shows the CLIC beam structure, consisting of bunch trains at a repetition rate of 50 Hz. Each train is formed by 312 bunches separated by 0.5 ns each.

Two general-purpose detector concepts are currently under study for CLIC: CLIC_ILD with an axial magnetic field of 4 T and CLIC_SiD with a field of 5 T. Both concepts include a pixel vertex detector placed as close as possible to the interaction point to obtain optimal secondary vertex reconstruction and to increase the precision and efficiency of the track reconstruction in particular for low-momentum tracks. The vertex detector is composed of a barrel and a forward vertex region, as depicted in figure 2. The barrel region is placed at the center and is made of several layers, 3 double layers for the CLIC_ILD detector and 5 single layers for the CLIC_SiD detector. Each layer is composed of several ladders, for instance the innermost layer of CLIC_ILD is composed of 18 ladders, while its outermost layer is composed of 34 ladders. Figure 2 shows the inner tracking region of the CLIC_ILD detector, highlighting a 24 cm long vertex ladder which is composed of 24 sensors, each bonded to a 1 cm^2 CLICpix hybrid readout chip currently under development [3]. The radiation exposure of the vertex detector is expected to be small, compared to the corresponding regions in high-energy hadron colliders. For the non-ionizing energy loss (NIEL), a maximum total fluence of less than $10^{11} n_{eq}/cm^2$ per year is expected for the inner-barrel and forward-vertex layers. The simulation results for the total ionizing dose (TID) predict approximately 200 Gy/year for the vertex detector region.

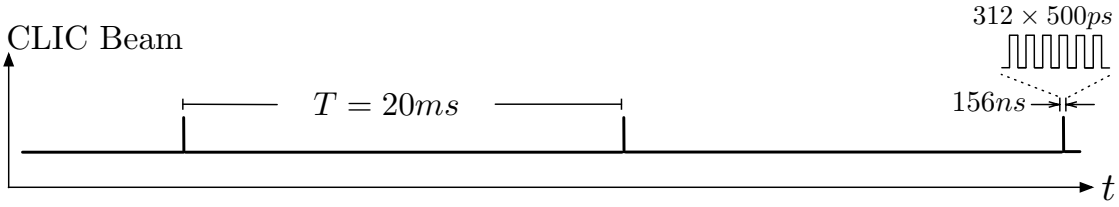

Figure 1. CLIC beam structure.

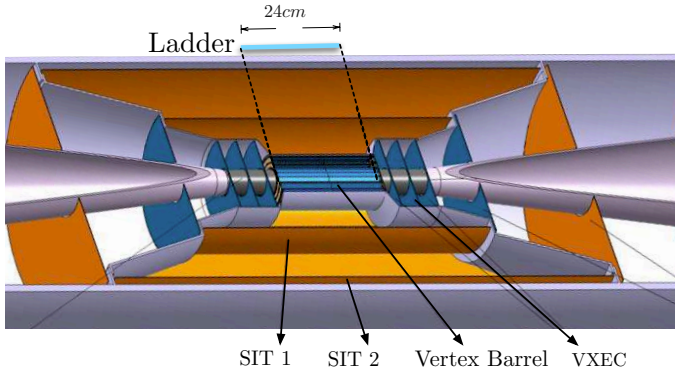

Figure 2. CLIC_ILD inner tracking region. The barrel region is placed at the center and is made of 3 double layers.

This paper proposes a low-mass power-pulsing scheme for powering the analog and digital electronics of the pixel barrel layers of the CLIC_ILD vertex barrel region. It is expected that CLIC_SiD will use the same readout topology and therefore a similar scheme will be also applicable in that case.

2 Requirements for the power delivery of the vertex detector readout electronics

In order to achieve the precision physics goals, the material budget of the vertex barrel detector is required to be less than 0.2% of a radiation length, X_o, per layer. To achieve such a low mass, ultra-thin high-resolution pixel detectors are foreseen, leaving approximately 0.1% X_o for cooling, mechanical structure and powering. Therefore, the contribution of the power delivery infrastructure should be well below 0.1% X_o per detection layer.

In order to reduce the mass contributed by cooling liquids and pipes, air cooling is foreseen instead [2]. This limits the average power removal to $50\,\mathrm{mW/cm^2}$, while the instantaneous power consumption of the front-end (FE) ASICs (Application-specific integrated circuits) is foreseen to reach few $\mathrm{W/cm^2}$. Air cooling would not be able to dissipate the heat if the FE ASICs were dissipating that power constantly. Therefore, the FE electronics needs to change from a high to a low power consumption state when possible, thereby reducing the average power consumption. The voltage regulation has to be stable even during high to low and low to high power consumption transitions. This restriction is particularly important for analog electronics, which are much more sensitive than digital. As a design goal, the voltage regulation for the analog electronics of the CLICpix chips should be within 50 mV in order to ensure a stable Time-over-Threshold (ToT) measurement.

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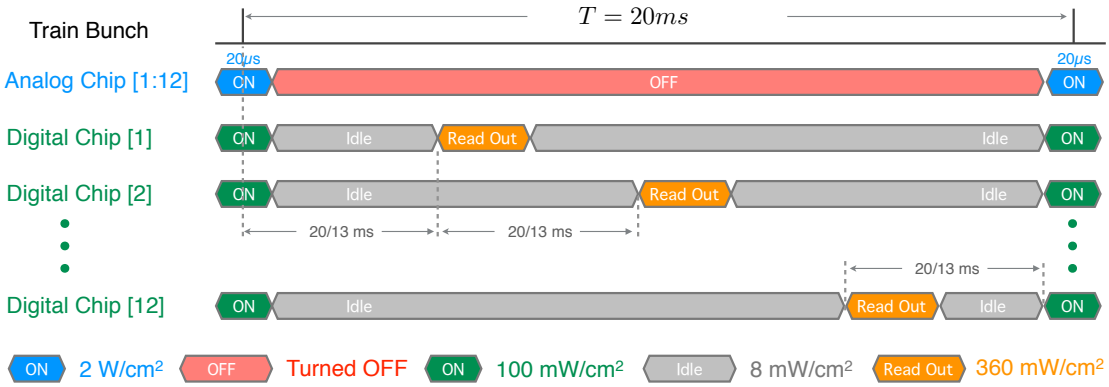

Figure 3. Analog and digital power consumption per half-ladder (N=12 ASICs).

3 Power consumption per half-ladder and power-pulsing

The barrel is foreseen to be powered symmetrically from both sides. Similarly, the 24 CLICpix ASICs belonging to a ladder would be read out from both sides in groups of twelve. Figure 3 summarizes the expected power consumption per half-ladder of the analog and digital electronics of the CLICpix ASICs, where N = 12 corresponds to the total number of CLICpix chips in the half-ladder and $T = 20\,\text{ms}$ to the time between bunch train crossings.

The analog electronics have a power consumption peak of $2\ \text{W}/\text{cm}^2$ during a time t_{on} around the bunch train. The time t_{on} has to be long enough to turn on the analog electronics and to process the data, and it is expected to be close to $20\,\mu\text{s}$. Contrary to the digital electronics, the analog electronics can be turned off completely after t_{on}. By doing that, the average power consumption can be reduced by a factor corresponding to T/t_{on}. In this particular case, the duty cycle is equal to $t_{\text{on}}/T = 20\,\mu\text{s}/20\,\text{ms} = 1/1000$, so the average power consumption is reduced to $2\,\text{mW}/\text{cm}^2$. This way of providing high power during small intervals and low power during the longest part of every period is referred to as "power-pulsing", and it represents an efficient way to reduce the average power consumption down to the allowed level.

Nevertheless, the transitions from high to low and from low to high power consumption imply load variations which make it more difficult to provide the required regulated voltage. For instance, as there are 12 chips in a half-ladder and the voltage required by the analog electronics is 1.2 V, the analog current in a half-ladder changes from 0 to 20 A. In order to facilitate the design of the power distribution system, each chip will be turned on and turned off gradually resulting in an increased rise t_r and fall t_f time (reducing the current bandwidth), as depicted in figure 4. Nevertheless, there is a compromise in how slow the rise and fall time can be in order not to increase substantially the average power consumption. In this paper we assume $1\,\mu\text{s}$ of rise and fall time.

Similarly, the digital electronics has a peak of power consumption around the bunch train where all the chips consume $100\,\text{mW}/\text{cm}^2$ (figure 3). After that, the 12 chips change to an idle state of $8\,\text{mW}/\text{cm}^2$ until the first chip starts to be read-out $\frac{20}{13}$ ms after the bunch train. Only one CLICpix chip is read-out at a time with a power consumption of $360\,\text{mW}/\text{cm}^2$, while the 11 remaining chips stay in an idle state. The time needed to read out every chip is proportional to the occupancy

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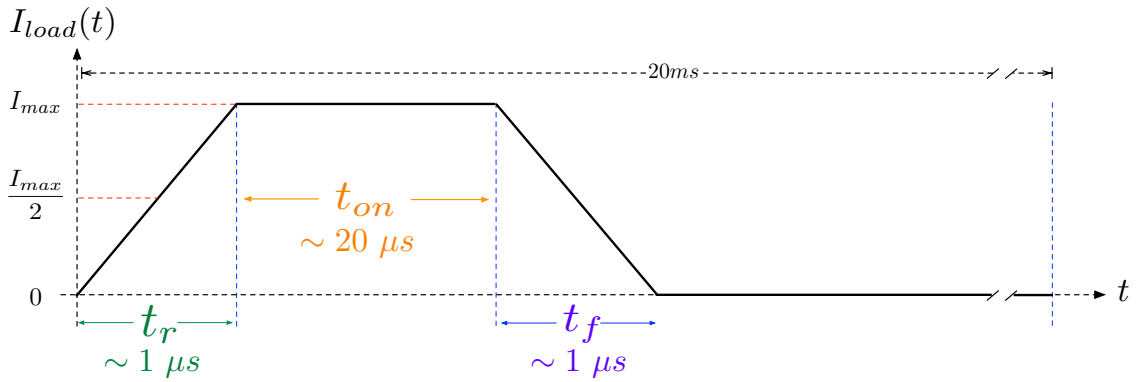

Figure 4. Analog load current per half-ladder. It changes from 0 to 20 A with a rise time t_r and fall time t_f of 1 μs each.

(number of pixels hit in the sensor divided by total number of pixels per sensor). For instance, it takes around 300 μs to read a chip with an occupancy of 3%, which is the maximum expected occupancy for the barrel region. The following chip is read out $\frac{20}{13}$ ms after the first one started to be read out in order to keep them equally spaced in time. This is repeated until the 12 chips are read out. The average power consumption for the digital electronics, assuming $t_{\text{on}} = 20\,\mu$s, $T = 20$ ms and the longest read-out time possible (300 μs), corresponds to 13.4 mW/cm^2. As the voltage required by the digital electronics is 1 V, the current transient during the bunch train will be from 96 mA to 1.2 A. Beside that load transition, there will be one extra transition every time a chip is read. When a chip is read, the current transition for the half-ladder will be from 96 mA to 444 mA. The current transient in the digital electronics case, even if more frequent, is much smaller than for the analog one. This makes it easier to provide good regulation to the digital electronics. In addition, regulation is less critical for digital electronics as it is less sensitive to voltage fluctuations. Analog and digital electronics will be powered separately. In that way, their powering schemes can be optimized independently to achieve their particular requirements.

4 Proposed powering scheme

In our application, we have a small interval of time of full consumption in which the capacitors discharge (20 μs) and then a much longer time of low power consumption (20 ms) that can be used to charge back the capacitors to their previous level (V_m).

The use of a controlled current source allows the value of the necessary current to be minimised, by using the whole duration of low power consumption to charge the capacitors. This charging current (I_{charge}) can be easily estimated as follows:

$$I_{\text{charge}} = \frac{I_{\text{discharge}} \cdot \Delta t_{\text{discharge}}}{\Delta t_{\text{charge}}} = \frac{20\,\text{A} \cdot 20\,\mu\text{s}}{20\,\text{ms}} = 20\,\text{mA} \tag{4.1}$$

where $I_{\text{discharge}}$ is the current consumed by the ASICs during the bunch train (20 A) and Δt_{charge} and $\Delta t_{\text{discharge}}$ are the charging (20 ms) and discharging (almost 20 μs) time, respectively.

The small duty cycle ($\Delta t_{\text{discharge}}/\Delta t_{\text{charge}}$) allows for a significantly reduced charging current. For instance, we could deliver the 20 A required by the half-ladder using a 20 mA continuous current from the back-end to the ladder.

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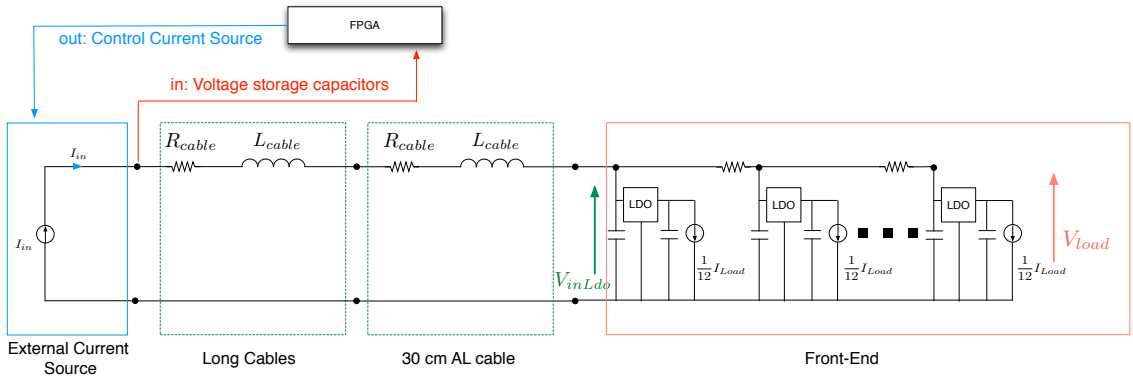

Figure 5. Diagram of a controlled current source powering a half-ladder. The voltage of the capacitors is sensed at the back-end.

In [4] we proposed a scheme for powering the analog electronics, based on local energy storage and voltage regulation. The energy was stored in capacitors close to the ASICs and the regulation was provided by low-dropout regulators (LDOs). The storage capacitors have to be charged back to their initial voltage before the next bunch train arrives. This was previously meant to be achieved using a DCDC buck converter [5] outside the vertex barrel region, connected through a 30 cm flex cable to the front-end electronics. In the following we present an improved powering scheme where the DCDC buck converters are replaced by programmable current sources.

This paper proposes a scheme that uses a back-end current source to charge up the capacitors, instead of a DCDC buck converter, which allows us to considerably decrease the material of the cables and to get rid of the mass of the DCDC converter.

4.1 Implementation

The current needed to charge the storage capacitors depends on the operating conditions of the readout electronics (temperature, occupancy, power consumption) which can vary from one bunch train to the next. A feedback mechanism is therefore implemented adjusting the back-end current based on the voltage at the capacitors at the end of the on-time.

This is illustrated in figure 5. A field-programmable gate array (FPGA) reads the sensed voltage of the storage capacitors and calculates the next value of the current (I_{in}) needed to reach V_m, which is programmed to the current source.

As the current flowing through the cable is of the order of a few tens of mA, it is possible to measure the voltage of the capacitors at the back-end, reducing the number of cables and therefore the mass. The voltage drop can be compensated knowing the resistance of the cable, as the injected current is known.

To describe the most important signals, let us suppose that the analog back-end input current (I_{in}) during the previous period was 20 mA. During the time t_{on} the front-end ASICs consume the 20 A. The storage capacitors discharge ΔV from their initial voltage (V_m) and the LDOs provide a regulated voltage close to 1.2 V. After this time, the analog electronics turns off and the voltage is not needed anymore. For that reason and in order to save power, the LDOs are disabled dropping their voltage to zero. The voltage at the capacitors is then measured and the new required current

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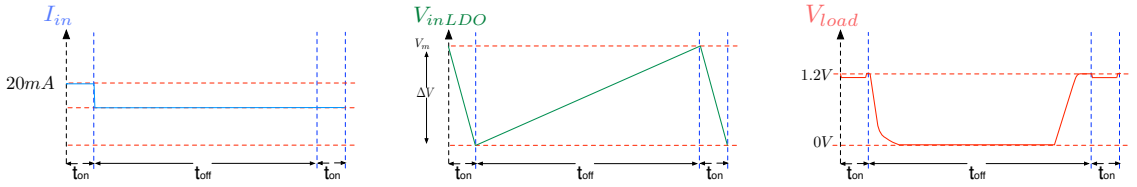

Figure 6. Typical waveforms. (Left) Back-end current. (Middle) Capacitors voltage. (Right) Output voltage.

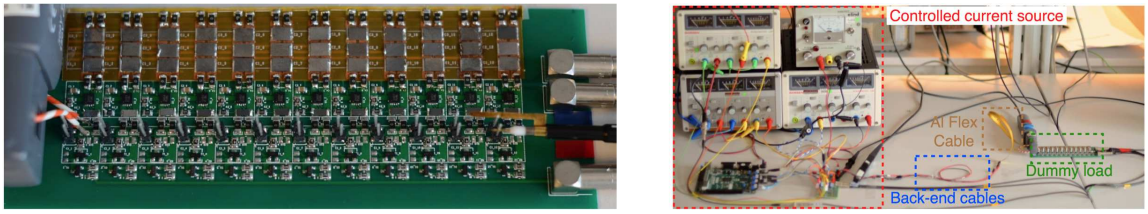

Figure 7. (Left) Analog dummy load PCB. (Right) Analog test setup.

is calculated in order to reach the voltage V_m in the available remaining time. If the power consumption during this bunch train was different from the previous one, then the current would be slightly different as depicted in figure 6. The LDOs are enabled 200 μs before the next bunch train to reach the required voltage before the electronics pass to the next high power consumption state, after which the cycle repeats again. For this first prototype the LDOs are enabled/disabled using a signal from the FPGA (not shown in figure 5). In the final application that signal could be either provided by the FE chip or not needed at all in case we use LDOs with smaller quiescent current (in which case the LDOs would be enabled all the time).

The digital electronics solution is very similar to the one for analog, but there are a few differences to take into account in the program of the FPGA. First, the discharge of the capacitors happens every $\frac{20}{13}$ ms instead of every 20 ms. The most challenging difference is that the digital electronics have a constant current consumption which might change with temperature, so it has to be predicted. Due to that constant current and as the time to recharge the capacitors is shorter, the total current from the back-end is around 10 times larger than for the analog. The signals are similar to the ones of figure 6, but the period is $\frac{20}{13}$ ms and the LDOs are always enabled, so their voltage is always 1 V.

4.2 Setup

The CLICpix FE readout ASICs are currently under development. In order to test the proposed scheme, their behavior was emulated using an array of MOSFETs commuting at the expected values of current and duration using signals from the FPGA. For convenience the low-mass flex cable, LDOs and capacitors were integrated in a single PCB, as shown in figure 7 (left). Two such dummy load PCBs were built, one for analog and one for digital, where the analog PCB is shown in figure 7 (left). The 1 mm wide flex cable has two layers of 20 μm thick aluminium instead of copper to reduce the mass contribution. For the same reason, the input and output capacitors are IPDIA silicon capacitors [6]. The LDOs were commercial off-the-shelf components.

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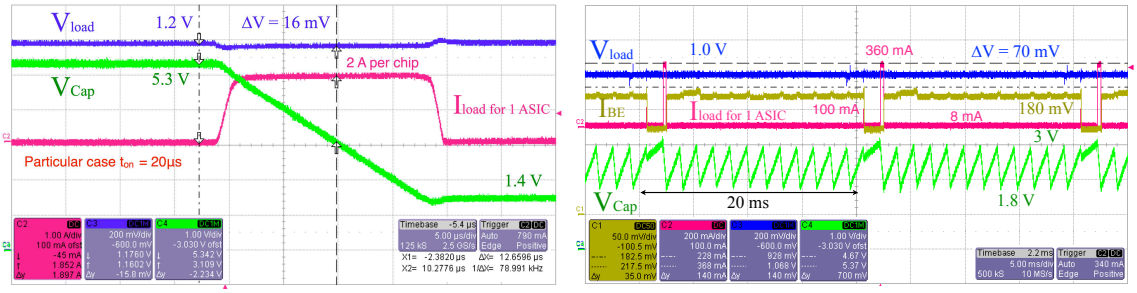

Figure 8. Measured output current and voltage at the last ASIC for (left) analog and (right) digital electronics.

Figure 7 (right) shows the implemented setup. At the left, four voltage supplies power the FPGA and a custom-made PCB serves as the controlled current source. The latter is connected to the back-end cables (represented each by 16 μH inductors with a series resistance of 1 Ω), which are then followed by the aluminium flex cable that is connected to the PCB emulating the FE electronics. The current at the load is measured using a current probe and the voltage regulation is measured using a scope voltage probe at the last chip, which represents the most challenging case. Finally, signals from the FPGA were used to trigger the MOSFET array and to disable/enable the LDOs.

5 Results

5.1 Regulation and power dissipation

The regulated voltage at the last ASIC was measured for t_{on} , t_r, and t_f equal to 20 μs, 1 μs and 1 μs, respectively. The analog voltage was constant during the on-time, having less than 20 mV voltage drop during the full on-period (figure 8 (left)). This was achieved using capacitors at the input and output of the LDOs of 10 μF and 1 μF, respectively. Similarly, the digital voltage had a good regulation with a spike of 70 mV during the transitions as shown in figure 8 (right). This was achieved using capacitors at the input and output of the LDOs of 6.6 μF and 1 μF, respectively. The presumed occupancy for all the chips was 3%, so the read out lasted for 300 μs per each chip. The scheme was also tested for varying read-out times to emulate variations from chip to chip and from one bunch train to the next. This resulted in an equivalent regulation of the output voltage.

The power consumption resulting from this scheme was measured. The total power losses are below the required 50 mW/cm^2, being less than 10 mW/cm^2 for analog and 35 mW/cm^2 for digital. Most of the losses are due to the LDOs, which could be reduced at the price of adding more material.

5.2 Material budget calculation

The material budget contribution of the powering infrastructure is calculated taking into account the components placed on the half-ladder: the low-mass flex cable composed of two conductive layers and a dielectric in the middle, the input and output capacitors and the LDOs. The average material thickness of each component was calculated assuming that the material is distributed evenly over

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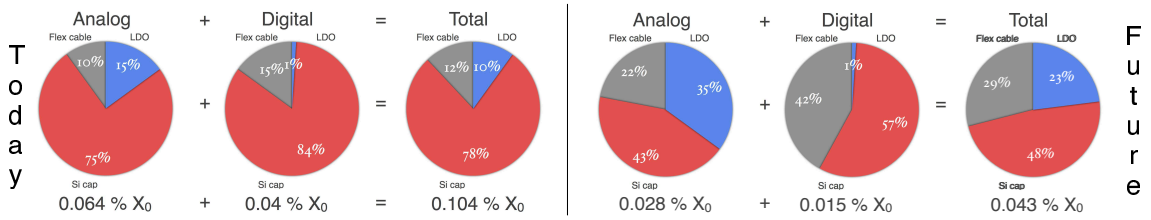

Figure 9. Material budget calculation for the powering of the ladder area: (left) with today's technology and (right) with improved silicon capacitors technology expected to be available in few years time.

the surface of the ladder. Figure 9 (left) shows the results of the calculation using the technologies available today. The total material budget contribution is 0.104% X_o (for digital plus analog) which, although small, still exceeds the material target of 0.1% X_o to share with the mechanical structures. From the pie chart (figure 9 (left)) it can be noted that the silicon capacitors are the dominating contribution (80%).

It is expected that within the next few years silicon capacitors with 4 times larger capacitance density will become available [6]. Taking this into account for the calculation, the total contribution decreases to 0.043% X_o (figure 9 (right)). The material can be decreased further using flex cables with thinner/narrower aluminum conductors and integrating the LDOs in the CLICpix ASICs. The width of the conductor can be decreased further ensuring that its resistance does not produce excessive voltage drop and/or power dissipation in the cable. As a simple estimation, the analog cable width (and therefore the mass) could be reduced by a factor 10 while the digital cable width could be reduced by up to a factor 3 in the ladder region.

6 Conclusions

A low-mass pulsed-powering scheme is proposed for the future CLICpix ASIC (Application-specific integrated circuit) of the CLIC vertex detectors. It comprises regulation and silicon capacitors in the front-end, which are charged up using a back-end current supply of around 20 mA for the analog part and less than 200 mA for the digital part. The scheme fulfills the regulation requirements, having a voltage drop during the acquisition time of less than 20 mV for the analog electronics and 70 mV for the digital electronics. The average power consumption of 45 mW/cm^2 (10 mW/cm^2 for analog and 35 mW/cm^2 for digital) is below the target of 50 mW/cm^2 in the sensor area.

The material contribution in the ladder area of 0.104% X_o per layer is already close to the target value. Future improvements of the silicon capacitor technology are expected to decrease the material budget even further, to levels close to 0.04% X_o. This can be reduced even further by redesigning the aluminum flex cable and by integrating the low-dropout regulators (LDOs) in the CLICpix ASICs.

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