Radiation damage measurements on the SVX readout chip

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Abstract

The effects of ionizing radiation on the SVX Rev D data acquisition integrated circuit are presented. This chip was fabricated in 3 micron CMOS technology and will be used to readout the Silicon Vertex subsystem of the CDF detector at the FNAL collider. Results include the change in the signal to noise ratio and the change in gain for the amplifier-discriminator circuit, and threshold and transconductance shifts for single test transistors included in the device.

1 Introduction

The SVX silicon strip readout circuit is a full custom VLSI chip [1] developed at Lawrence Berkeley Laboratory for use in the CDF [2] microstrip silicon vertex detector [3] (SVX) at the Fermilab Tevatron collider. The SVX chip has been fabricated in 3 micron CMOS technology at the foundry of the Hewlett Packard Corporation. It contains 128 channels of low noise charge amplification, sample and hold, and comparator latch circuitry followed by a digital section which allows readout of only those channels in which the integrated charge exceeds a pre-injected analog threshold level (sparse readout).

The radiation level inside CDF has been measured during the last collider run [4] (fig. 1). These measurements show that for the 50 pb^{-1} expected for the 1992 run, the radiation level for the innermost layer of the SVX detector could reach 20krad [5]. Previous measurements on an earlier version of the SVX chip (SVX Rev C") showed a large increase in the input noise level after 20krad [6] confirming the "softness" of the CMOS process used in the fabrication of this chip.

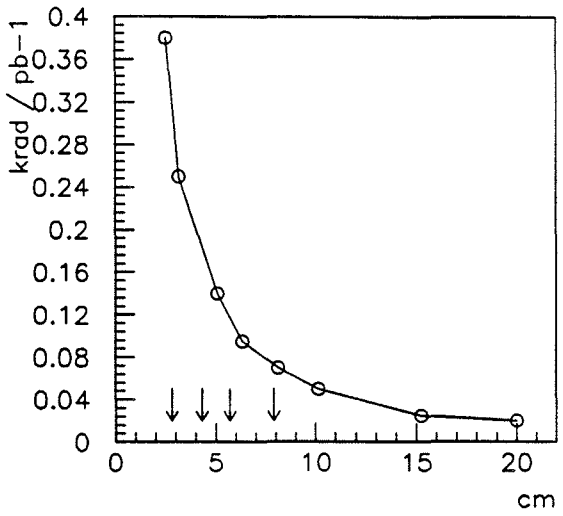

Figure 1: *Expected radiation level inside CDF as function of the distance from the beam line (the position of the 4 SVX layers is indicated by the arrows)*

The zero dose noise levels of the SVX Rev C" chip exceeded the specifications for use in CDF. Consequently a new version of the SVX chip that met the zero dose specifications was designed and fabricated at the same foundry (SVX Rev D). Here we report on a new set of radiation damage measurements made on SVX Rev D. These measurements were undertaken to give a limit on the

survival of the two innermost layers of the SVX detector inside CDF, to aid in the development of dosimetry and radiation monitoring for use during the CDF run, and to set the time schedule for the replacement of the inner SVX layers with a new radiation hard version chip (SVX Rev H) which is being currently manufactured at United Technologies Microelectronics Center.

In the layout of the SVX Rev D chip four external transistors were included (2 PMOS and 2 NMOS) for test purposes. These are unconnected to the other circuitry of the chip. They all have a W/L ratio of 138/3. We studied the characteristics of these single transistors as a function of the radiation dose in order to have a better understanding of the different processes through which the ionizing radiation is degrading the performance of the chip.

2 Experimental Setup

The irradiations were done using a $^{60}Co\,\gamma$ source at Lawrence Berkeley Laboratory. This source delivered about 3krad per hour at 1 meter. The samples were irradiated with a dose rate which never exceeded 10krad per hour.

The samples were mounted perpendicularly to the incident γ radiation with a screen of aluminum and lead (1.5mm and 0.5mm thick respectively) in front of the chips in order to reach the appropriate "charged particle equilibrium" [7].

Some of the chips were exposed with the power on and some other with the power off. This was done to test the generally accepted view that radiation damage to MOS devices is worse under power and to justify a proposed power down procedure during lossy operations of the accelerator.

In order to simulate the presence of the silicon strips three of the 128 preamp inputs were connected to capacitors (10, 20 and 30pF) near the beginning, center and end of the chip's channels. The other inputs were left floating.

The results presented are averages of measurements taken on 4 chips. A fifth unirradiated chip was measured as a reference.

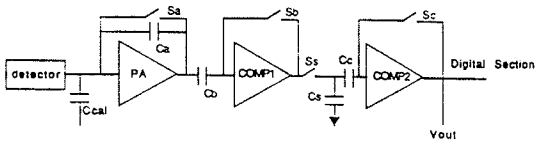

Figure 2: *SVX Rev D: input channel*

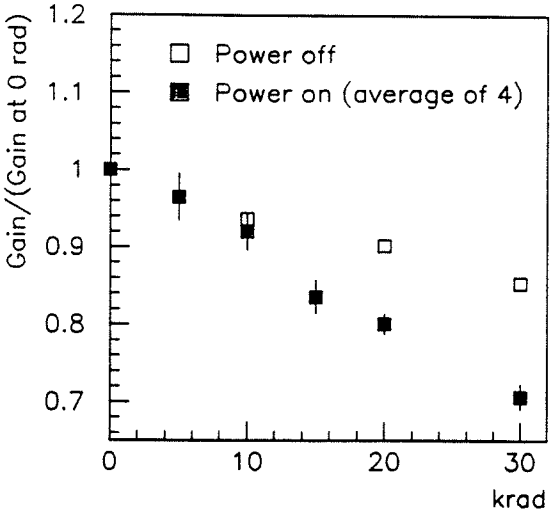

Figure 3: *SVX Rev D: Gain vs Dose*

3 SVX Rev D: Gain and Noise

The logic diagram of the analog part of the chip is shown in fig. 2. The first stage is a charge sensitive preamplifier whose open loop gain is about 2000 and whose charge gain is set by the feedback capacitor. This is followed by three stages of CMOS inverters which serve as voltage gain stages, elements of sample and hold comparators and an output buffer. The gain stages operate in an open loop configuration as single transistors with diode connected loads.

Fig. 3 shows the change in the overall gain of the chip as a function of the radiation dose. The expected loss of gain with the dose (due to a lower value of g_m) is higher for the power on measurements than for the power off measurements. The loss is about 30% after 30krad. This fact is consistent with the decrease of the value of the transconductance measured for single transistors (see section 4).

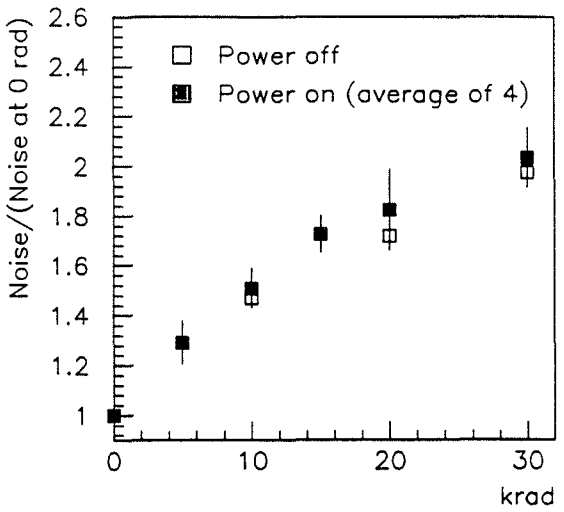

Figure 4: *The SVX Rev D, Noise vs Dose for the 30pF input channel*

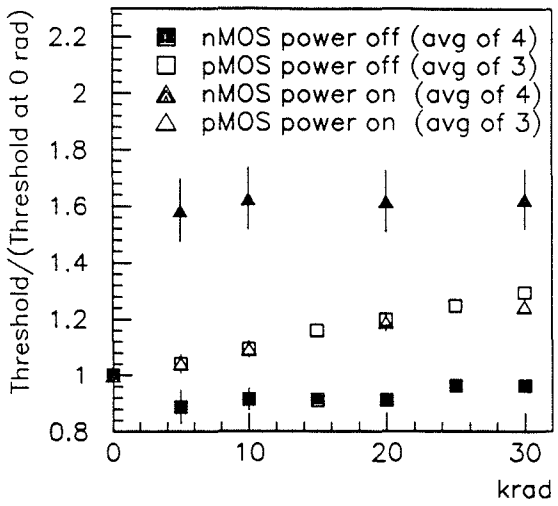

Figure 5: *Threshold shift vs Dose for both PMOS and NMOS*

Gain	0 rad	30 krad
preamp	0.19	0.19
comp1	4.90	4.20
comp2	0.89	0.78

Table 1: *Gain of different amplification stages*

The gain of the preamp and the individual open loop stages were measured on a probe station both before and after irradiation (Table 1). We observed that the gain losses were distributed among the open loop stages. As expected the charge gain of the preamp stayed constant.

The output noise spectrum of a CMOS amplifier is generally dominated at low frequencies by the $1/f$ noise and at higher frequencies by white noise. Both these components are influenced by radiation due to trapped interface states under the gate oxide of the input transistor.

In our measurements the noise level referred to the input of the integrator increased with the dose but we observed no significant difference between power on and power off measurements (fig. 4). On the 30pF input channel the noise doubled after 30krad. Some saturation at higher doses was indicated as well. After 30krad, the signal to noise ratio was reduced from 12 to 6, which is insufficient to our purposes.

4 Single transistors: threshold and transconductance

For power on measurements the single transistors were irradiated using a simple common emitter polarizing scheme with a 1kΩ collector resistor, 5V at the collector and 2.5V at the gate terminals. For the PMOS devices the expected hole trapping in the Si/SiO_2 interface results in a shift of the threshold toward more negative values, up to about 30% of its original value at 0 rad (fig. 5). There is no noticeble difference between power on and power off measurements.

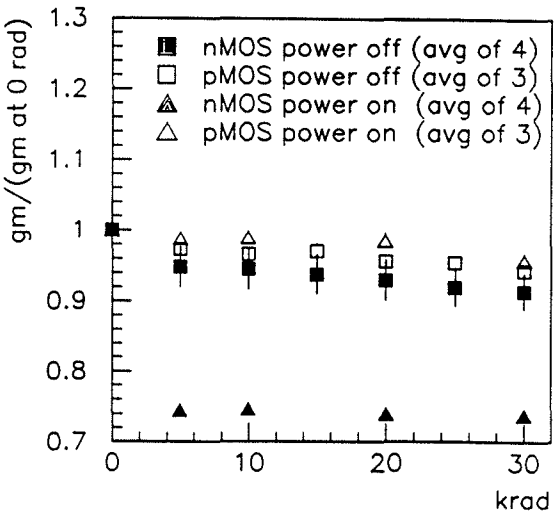

Figure 6: *Transconductance g_m vs Dose for both PMOS and NMOS*

The decrease of the transconductance values is mainly the result of the build up of interface states which degrades the mobility of carriers in the channel and consequently g_m. For the PMOS deveices we measured almost no change in the g_m which suggests that charge trapping is the main effect of the ionizing radiation here. The NMOS devices showed a different behavior. Here the hole trapping and the generation of interface states are competing mechanisms

and for the power off measurements there was almost no change in the threshold value with dose. For the power on measurement however, we observed a dramatic change in the threshold (which rises by 60% of its original value after just 3krad) which maybe due to a heavy build up of interface states. This conjecture is consonant with the measured loss in the transconductance (fig. 6) value which also goes down by 25% after only 3krad.

5 Conclusions

We measured the gain and the noise performance of the SVX Rev D chip as a function of ionizing radiation dose up to values of 30krad with a ^{60}Co source at LBL. We conclude it will be necessary to replace the first two layers of the silicon vertex detector at CDF due to the radiation damage after an accumulated dose of 30krad.

References

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