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SEMICONDUCTOR DRIFT CHAMBER - AN APPLICATION OF A NOVEL CHARGE TRANSPORT SCHEME†

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ABSTRACT

The purpose of this paper is to describe a novel charge transport scheme in semiconductors in which the field responsible for the charge transport is independent of the depletion field. The application of the novel charge transport scheme leads to the following new semiconductor detectors:

i) Semiconductor Drift Chamber
ii) Ultra low capacitance - large area semiconductor x-ray spectrometers and photodiodes.
iii) Fully Depleted Thick CCD

Special attention is paid to the concept of the Semiconductor Drift Chamber as a position sensing detector for high energy charged particles. Position resolution limiting factors are considered, and the values of the resolutions are given.

I. INTRODUCTION

For many applications the use of a semiconductor as a detection medium is a great advantage. In low energy radiation spectroscopy it is well known that semiconductor detectors achieve the best energy resolution.

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In high energy physics, however, the position sensing is performed today mostly with gas proportional or drift chambers. For several years there has been an interest in the application of semiconductors as high resolution position sensing detectors for particle physics[1].

Figure 1 shows an example of a typical position sensitive silicon microstrip detector[2]. It consists of a thin (≈ 300 μm) n-type silicon wafer having a continuous n^+n junction on one side of the wafer and a strip pattern of p^+n junctions on the opposite side. A suitable reverse bias voltage is applied across the wafer to deplete the detector and to provide the collection field. A fast charged particle passing through the detector produces electron-hole pairs which drift toward the electrodes under the influence of the electric field. The motion of the charge carriers induces the signal in an external amplifier connected between the n^+ and the p^+ contacts.

Position sensing in this kind of configuration is done by the granularity of p^+ contacts. The method, in principle, requires as many amplifiers as the number of individual strips. Using charge division readout (capacitive or resistive) the number of amplifiers can be reduced by up to a factor of 10; a certain price is paid in the complexity of the readout channels and the doubletrack resolution is sacrificed. Nevertheless the number of readout channels per unit length remains very large (≈ 20 - 500 channels/cm). The practical problems related to the number of readout channels (the volume requirement, the heat dissipation and the connection problems) limit the application of microstrip silicon detectors to a few special experiments.

In this paper we are going to describe a novel scheme of operation for semiconductor detectors which is applicable to the position sensing in silicon detectors. The new method should be capable of achieving the same position resolution as a very fine microstrip silicon detector with hundreds times fewer readout channels.

In Part II the principles of the method, that is the full depletion of the semiconductor from a virtual electrode (anode) and the application of the charge transport field, are described.

Part III presents results of experimental tests which confirm the principles of the method. In Part IV the new detector devices are introduced. In Part V the analysis of the Semiconductor Drift Chamber is presented.

II. PRINCIPLES OF THE METHOD.

We are going to show that it is possible to fully deplete a thin, large area semiconductor wafer through a small contact somewhere at the edge of the wafer (virtual electrode). After a complete depletion of the semiconductor wafer we are free (within certain limits) to superpose the second electric field to transport carriers in a way suitable for position sensing of ionizing particles.

Figures 2a, b, c and d show the depletion of the semiconductor wafers from a "virtual" electrode.

Let us start with a classical semiconductor junction (diode) detector. Figure 2a shows two n-type silicon detectors with a p^+ and an n^+ junction at opposite sides of the wafer. Two detectors are placed parallel to each other in such a way that the n^+ electrodes are in contact. We start to apply the same reverse bias to both detectors.

Figure 2b shows the depleted region and the potential across the two detectors under the one-sided abrupt junction one-dimensional approximation[3,4]. If we neglect the built-in and the thermal potential we can write down a well-known expression for the thickness of the depletion region d:

$$d = \sqrt{\frac{2\varepsilon U}{q \cdot N_D}} \cdot \qquad d \leq \ell/2 \qquad (1)$$

where U is the applied potential, ε is the absolute dielectric constant, q is the charge of an electron and N_D the concentration of electrically active donors in a semiconductor bulk.

From Figure 2b and equation (1) we see that the formation of the depletion region with the potential drop U across it is a consequence of the reverse biased rectifying p^+n junction. Uncovered fixed positive charges in the depletion region are compensated with an equal total negative charge "sitting" in the p^+n junction. The n^+n junction does

not play any role in the mechanism of the depletion. Its only function is to conduct the removed electron from the depletion region to the external contact.

Figure 2c shows the same electrostatic situation as in Figure 2b, but with a single semiconductor wafer twice the thickness of the previous ones and with two p^+n junctions at two sides of the wafer. The connection to the undepleted central part of the wafer is at the edge of the wafer as shown in Figure 2a.

The undepleted semiconductor in the middle of the wafer acts as a conductor and thus replaces the function of the n^+ junction in Figure 2b. The mechanism of the depletion is identical to the "classical" p^+ n junction, that is the same as in Figure 2b, and governed by equation (1). With the increasing bias voltage U the depletion region increases at the expense of the thickness of the undepleted conductive channel. Figure 2d shows the limiting case of a fully depleted silicon wafer; the central conductive channel has disappeared. The instability of the fully depleted wafer against the thermal generation of electron-hole pairs is not a conceptual problem. We can incline the potential shown in Figure 2d in the direction perpendicular to the paper plane in such a way that thermally generated electrons are continuously swept towards the n^+ anode.

Figure 3 shows the resulting potential function in two dimensions. A section of this surface with the plane $y = o$ gives the parabola of Figure 2d. The uniform electric field applied along the y-axis transports electrons in the middle of the valley toward an anode located farther downstream (not shown).

This "gutter" picture illustrates the operation of the Semiconductor Drift Chamber. Electrons generated during the passage of a fast particle are transported in this "gutter" from the position of the generation to the anode. The time delay between the passage of the fast particle and the signal at the anode is due to the drift of electrons. The measure of this time delay gives the measure of the distance between the position of the fast particle and the position of the anode in a similar manner to a gas drift chamber.

Before introducing the semiconductor drift chamber and related devices we will present experimental evidence of the depletion of the semiconductor (silicon) wafer through a "virtual" anode.

III. EXPERIMENTAL TEST OF THE DEPLETION

To verify the depletion mechanism of the semiconductor via the "virtual" electrode concept a special silicon device was prepared in the semiconductor lab at BNL[5].

Figure 4a shows the disc shaped silicon device (not to scale). The bulk material was n-type 10 k Ω cm ($N_D = 5 \times 10^{11}/cm^3$) silicon supplied by KOMATSU Corp. The rectifying p^+n barriers (junctions) on both sides of the wafer were realized by gold evaporation (surface barrier). Along the circular edge of the wafer six independent Aℓ (n^+) contacts were evaporated. The bias voltage was applied between the p^+n, gold barriers (connected to the same potential) and one of the aluminum n^+ contacts.

Two different capacitance-voltage (CV) characteristics were measured. The first characteristic is the dependence of the capacitance between two p^+ contacts on the bias voltage; the second characteristic is the capacitance between two p^+ contacts connected together and the n^+ contact as a function of the same bias voltage.

Figure 4b shows details of the first measurement. The n^+ contact was connected to the external bias circuit through a large (2M Ω) resistor. Thus the undepleted silicon in the middle of the wafer behaves (at the frequency of measurement) as a floating conductor between two electrodes. The measured capacitance can be represented as the result of two capacitances connected in series. The first capacitance is formed between the first p^+ electrode and the central channel and the second between the central channel and the other p^+ electrode. The value of each capacitance depends on the depletion layer and thus on the bias voltage U as given in equation (1).

Figure 5 shows the result of the measurement of the first CV characteristic. In the low voltage region the measured points follow closely the predicted $1/\sqrt{U}$ dependence (full line). Above the value of the bias voltage corresponding to full depletion the capacitance is

purely geometrical and does not depend on the voltage. The value of the depletion voltage agrees with an independent measurement of the depletion voltage of a standard n-p detector constructed from the same material. Also the measured value of the final geometrical capacitance agrees with the calculated value.

Details of the second measurement are shown in Figure 4c. This p^+, n^+ capacitance is expected to have an interesting dependence on the applied bias voltage. For voltages below the depletion voltage, the capacitance is essentially that of two standard detectors in parallel. As the bias voltage reaches the total depletion voltage, the conductive channel retracts and the capacitance drops abruptly.

The remaining value is a much smaller capacitance of a coaxial geometry between the p^+ electrode and the undepleted silicon around[6].

Figure 6 displays the experimental results. We can see a sharp drop in the capacitance at the bias voltage equal to the total depletion voltage as follows from the theory of the device.

We would like to stress that to confirm the full depletion, both measurements are required. It is possible to obtain an abrupt drop in the second measurement by a pinch-off of the n channel only somewhere close to the contact point. The first measurement by itself is not sensitive enough to prove the complete depletion of the wafer.

IV. APPLICATION OF THE NOVEL CHARGE TRANSPORT SCHEME TO NEW DEVICES

We will start this part by summarizing the principles of the novel method in a more mathematical language. The electric field inside a semiconductor device is described by the potential ϕ which defines the motion of carrier and thus governs the behavior of the device.

To calculate the potential ϕ inside a device we will neglect all built-in and thermal potentials as well as the effect of currents inside the semiconductor. Both approximations are justifiable in our application where the bias voltage dominates all other potentials and the signal currents are very small.

Under our assumptions the potential energy function ϕ inside a fully depleted semiconductor is defined by boundary conditions and has to satisfy Poisson's equation:

$$\Delta\phi = -\frac{N_D \cdot q}{\varepsilon} \quad , \tag{2}$$

where N_D, q and ε retain their meaning from eq. (1). (We have assumed n-type, uniformally doped semiconductor. It is easy to rewrite equations for the opposite configuration.)

We will "construct" the potential ϕ as the sum of two potentials ϕ_1 and ϕ_2. We will constrain the first potential ϕ_1 to satisfy eq. (2). Therefore, from the linearity of eq. (2) the potential ϕ_2 has to satisfy Laplace's equation:

$$\Delta\phi_2 = 0 \tag{3}$$

To fulfill the assumptions of small currents and the total depletion of the semiconductor the resulting electric field has to provide reverse bias for all junctions and the potential ϕ must not have any local minima or maxima.

The physical interpretation of ϕ_1 and ϕ_2 is obvious. The potential ϕ_1 is a depletion potential and its form is a consequence of the fixed charged uncovered in a depleted semiconductor. The second potential ϕ_2 has the form of the potential in a charge free region and is there to transport the carriers in a desirable way. Because it transports also thermally generated carriers, potential ϕ_2 stabilizes the full depletion of the semiconductor.

Now, let us see how it all works in a few examples of new devices.

i) Semiconductor Drift Chambers

In a one-dimensional case Poisson's equation (2) reduces to the following ordinary differential equation:

$$\frac{d^2\phi_1}{d_x 2} = -\frac{N_D q}{\varepsilon} \tag{4}$$

which has the parabolic solution:

$$\phi_1 = -\frac{N_D q}{2\varepsilon}(x-x_o)^2 + \phi_o \qquad (5)$$

where x_o and ϕ_o are the integration constants. The parabola of Figure 2d is exactly this solution with $x_o = \phi_o = 0$. (In all figures we show the negative potential or the electron potential energy as is always done in the semiconductor literature. In this convention, electrons are moving toward the lower values of -U.)

The potential given by equation (5) can be produced within an n-type semiconductor wafer with p^+n rectifying junctions on both sides of the wafer as was described in Part III.

The "gutter" shown in Figure 3 is the sum of potential ϕ_1 given by equation (5) and of the potential

$$\phi_2 = -E \cdot y \qquad (6)$$

The linear potential (6) clearly satisfies the Laplace's equation (3). The total potential ϕ describes the field of the Semiconductor Drift Chamber as was mentioned in Part II. The field due to the potential ϕ_2 transports the electrons for a long distance parallel to semiconductor faces. The field related to ϕ_1 brings the ionization to the center plane of the semiconductor and provides a focusing force during the drift.

ii Ultra Low Capacitance Detector

Potential ϕ_2 as given by equation (6) moves electrons parallel to the y-axis independently of the third coordinate z. Thus the length of the charge collecting anode in the z-direction cannot be shorter than the z-dimension of the detector. To obtain the smallest possible capacitance of the anode (to minimize the effect of the amplifier series noise for the total charge measurement) we can transport electrons toward practically a point anode. To realize the transport the potential ϕ_2 has to have the form:

$$\phi_2(x,y,z) = f(r), \quad \text{where} \quad r^2 = y^2 + z^2; \qquad (7)$$
$$f(r_1) < f(r_2) \text{ for } r_1 > r_2,$$

where f(r) satisfies the two dimensional Laplace's equation. If only

total charge information is required the exact form of f(r) is unimportant. If the measurement of the distance from the anode is performed at the same time we may require a function f(r) with "good" calibration properties.

An interesting feature of this kind of detector is the independence of the effective detector capacitance on the detector area. Very large area radiation detectors or photodiodes using this principle may have much improved noise performance when compared to traditional diode detectors.

iii) Fully depleted CCD

If the potential ϕ is different at two sides of the wafer the potential maximum (minimum of the electron potential energy) moves from the center of the wafer. The position of the maximum is the value of the integration contact x_o in eq. (5). We have full control of x_o through the boundary conditions. An interesting choice corresponds to the position of the potential maximum close to one side of the wafer (Fig. 7). Potential close to this side is similar to the potential of a buried channel charge-coupled device (BCCD)[7]. Therefore electrons can be transported in the same way as in a standard BCCD, that is, under the action of a peristaltic charge pump. We can view the field of the peristaltic pump as a dynamic generalization of our potential ϕ_2.

The main difference between the device described here and a standard BCCD is the full depletion of the new device. When used as a particle detector, electrons produced anywhere inside the semiconductor are moving rapidly into the potential energy minimum. Then they are transported due to the action of the pump towards the reading anode as done in a standard BCCD.

One side of the wafer has a continuous p^+n junction. If this junction is made sufficiently shallow, fully depleted CCDs may be superior to the special BCCDs used now in astronomy. (The dead layer due to the inactive silicon should decrease.)

V. ANALYSIS OF SEMICONDUCTOR DRIFT CHAMBERS

A possible practical realization of the Semiconductor Drift Chamber is schematically shown in Fig. 8[8]. It is a thin (≈ 300 μ thick few cm^2 in front area) wafer of high purity n-type silicon. The drift field potential (called ϕ_2 in the previous part) is formed by applying a linear potential to a strip array of rectifying p^+n junctions on both sides of the wafer. The only readout electrode (small capacitance anode) is also on the front face of the wafer to facilitate the photoengraving process during the fabrication.

The bottom of the "gutter" of Fig. 3 was moved from the center of the wafer toward the front face. The electrostatic configuration responsible for the turn of the "gutter" is shown in Fig. 9. In the anode region a different potential is applied to the junctions in the front and on the back sides of the wafer (with the same y coordinate). The bottom of the "gutter" thus moves toward one side of the wafer. The difference is largest at the anode plane. In this plane the new detector looks like a standard n-p junction detector.

The position information is derived from the measurement of the electron drift time and in the first order independent of the number (granularity) of drift field defining p^+ electrodes.

The form of the current induced at the anode due to the unit of charge drifting in the device of the geometry and applied electric field of Figs. 8 and 9 is shown in Fig. 10. (The corresponding electron drift velocity is 1.3 μm/ns.) The curve of the induced current starts when the charge is 500 μm away from the center of the anode as measured along the y-axis. There the effect of the moving charge is screened by surrounding p^+ electrodes (p^+ junction). The main portion of the total charge is induced when the distance of the moving charge from the anode is about the same as the width of the anode.

To calculate the position resolution[9] of the Semiconductor (Silicon) Drift Chamber with the geometry given in Fig. 8 the following position resolution limiting factors were considered:

i) series amplifier noise
ii) electron diffusion (and mutual repulsion of electrons[10])
iii) detector leakage current

(Due to the much higher density and the smaller energy requirement to produce an electron hole pair of the silicon compared to the gas, the two fundamental limitations of the gas drift chamber resolution, that is, δ-ray production and small number of the primary ionization clusters are largely reduced and are not expected to limit to the position resolution of the device.)

The calculated resolution is in the region of (2-5) μm, depending mostly on the detector thickness (signal charge) and on the value of the drift velocity. The contribution of amplifier noise increases with an increase of the drift velocity while the other two contributions decrease, leading to some optimal drift velocity for a given detector thickness ((1-2 μm/ns for a 300 μm thick wafer). This rather low value may not be the most desirable drift velocity for some applications. For a higher drift velocity the resolution is limited mainly by the amplifier noise. To circumvent this problem we can use the local transistor action at the p^+n junction next to the anode to provide a charge gain[11].

VI. CONCLUSIONS

A new charge transport scheme independent of the depletion voltage was proposed. The basic idea was verified experimentally. The application of the scheme leads to several new detector devices. The most straight-forward device, called Semiconductor Drift Chamber was described and some results of the analysis presented. The position resolution of the Semiconductor Drift Chamber is expected to be of (2-5) μm, i.e., in the region previously obtainable only by emulsion detectors.

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REFERENCES

[1] For example, Silicon Detectors for High Energy Physics. Proceedings of a FNAL, October 15-16, 1981, Univ. of Rochester.
[2] J. Kemmer et al. IEEE Trans. of Nuc. Sci., NS-29, No. 1,733, (1982)
[3] S. M. Sze, Physics of Semiconductor Devices, 2nd ed., p. 74, Wiley, New York, (1981).
[4] G. F. Knoll, Radiation Detection and Measurement, p. 383, Wiley, New York, (1979).
[5] We are indebted to R. H. Beuttenmuller for the fabrication of the device.
[6] A similar abrupt drop in capacitance was observed at depletion of a more complicated structure:
F. Capasso, IEEE Trans. on Electron Devices, ED-29, 1388, (1982).
[7] R. H.Walden et al., Bell Syst. Tech. J., 51, 1635, (1972).
[8] E. Gatti and P. Rehak. The concept of a Solid State Drift Chamber, Proceedings of the 1983 DPF Workshop on Collider Detectors, Feb. 28-March 4, 1983, LBL-15973, UC-37, CONF-830224, p. 97.
[9] E. Gatti and P. Rehak. to be published in NIM.
[10] We are indebted to G. Lutz from Max Planck Institute in München to bring our attention to this point.
[11] T. C. Madden and G. L. Miller. A Particle Detector Proving Charge Gain by Means of a Local Transistor Action, in Proceedings of a Gatlinburg Conf. on Semiconductor Nuclear Particle Detectors and Circuits., Nucl. Sci. Series, Report No. 44, Publication 1693, p. 314, Nat. Acad. Sci., Washington, D.C., (1969).

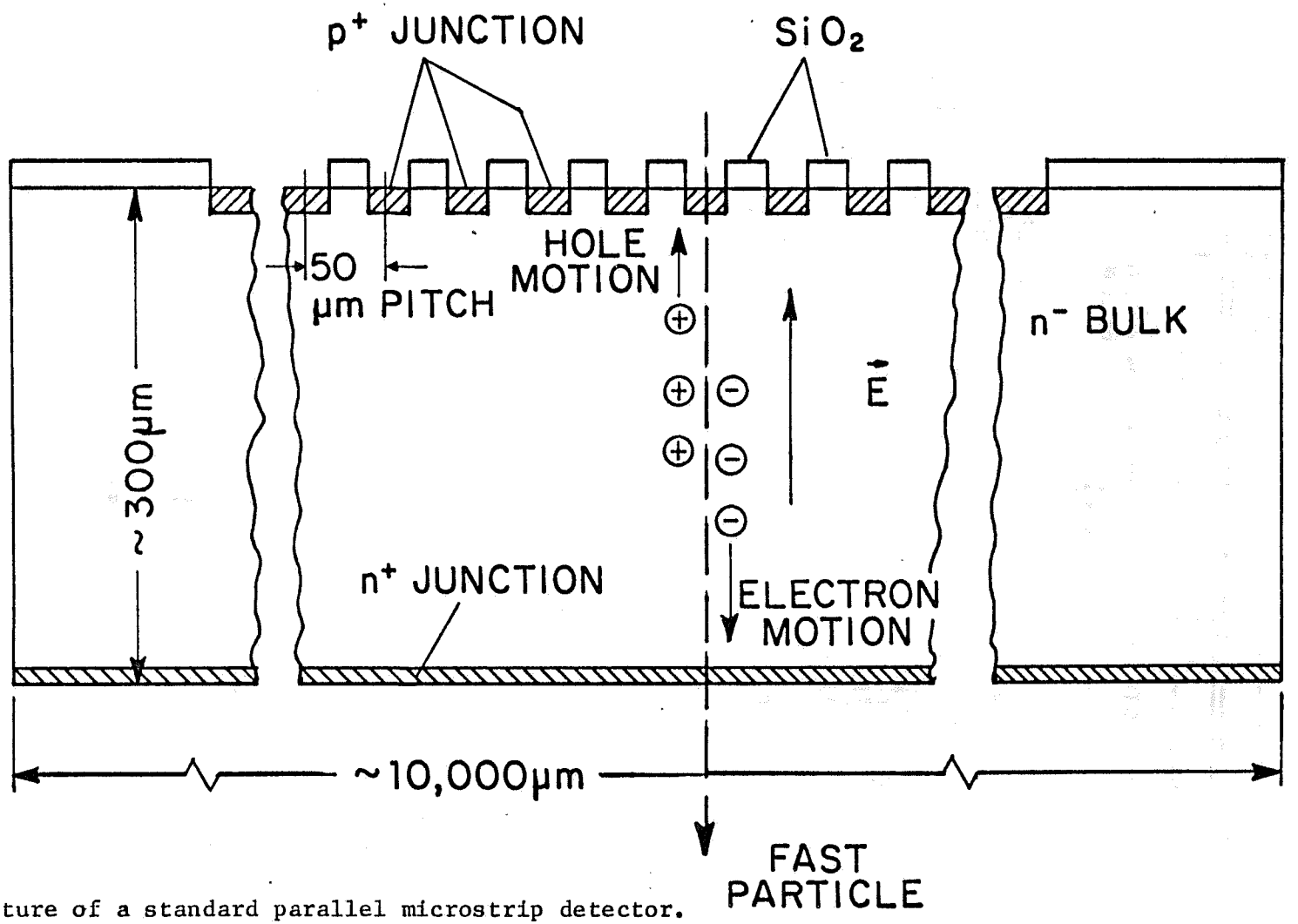


Fig. 1. Structure of a standard parallel microstrip detector. The same voltage provides the depletion of the semiconductor crystal and the drift field for charge carriers produced by ionizing particles.

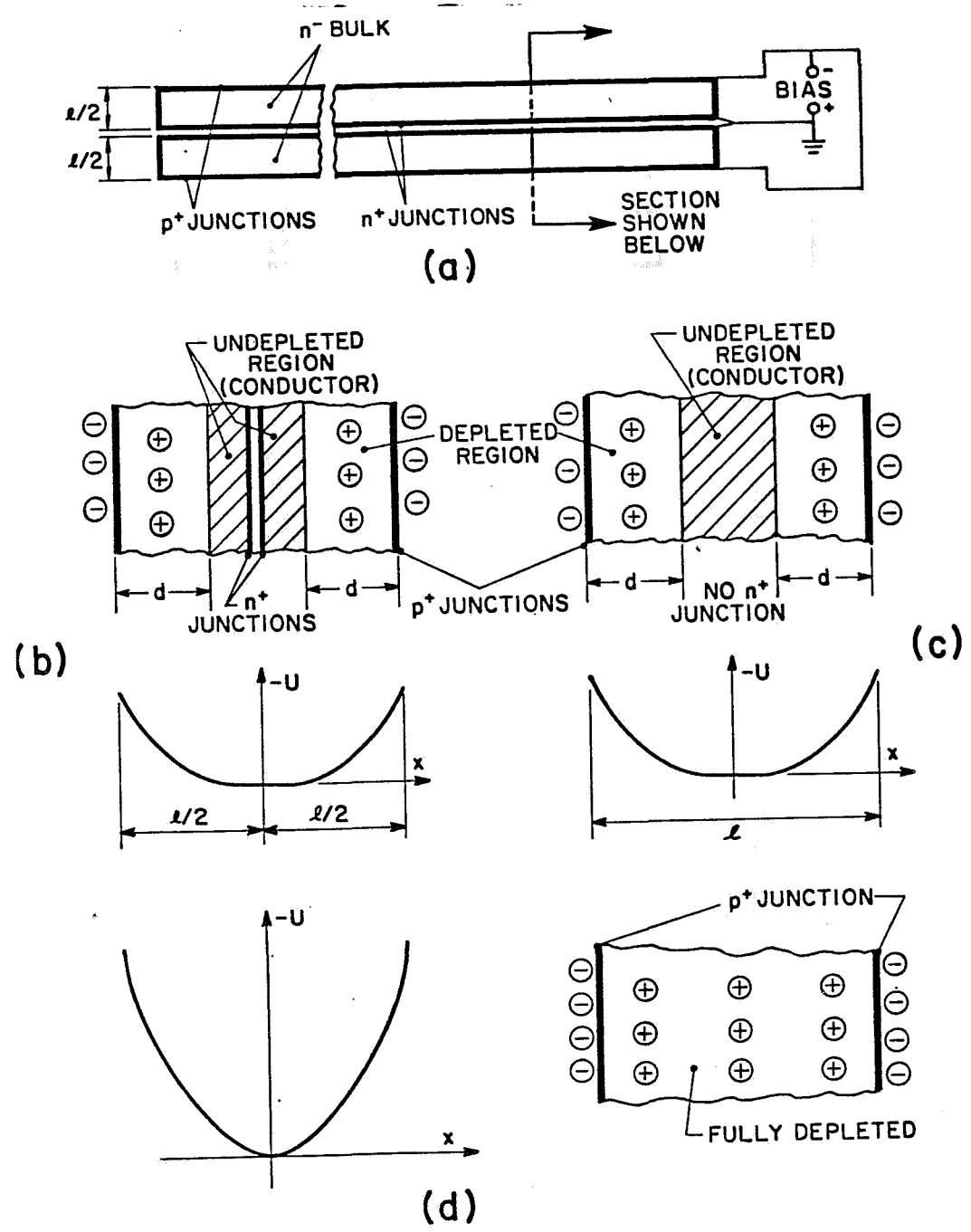


Fig. 2. a) Two standard n,p junction detectors with n^+ junctions in contact.

b) Depletion region of two detctors when a reverse bias voltage was applied (top). The potential profile across the detectors (bottom).

c) Depletion regions of a single n-type semiconductor wafer with p+ junction on both sides (top). The potential profile of the wafer (bottom).

d) Fully depleted silicon wafer. We see the potential across the wafer (left) and notice the disappearance of the central conductive channel (right).

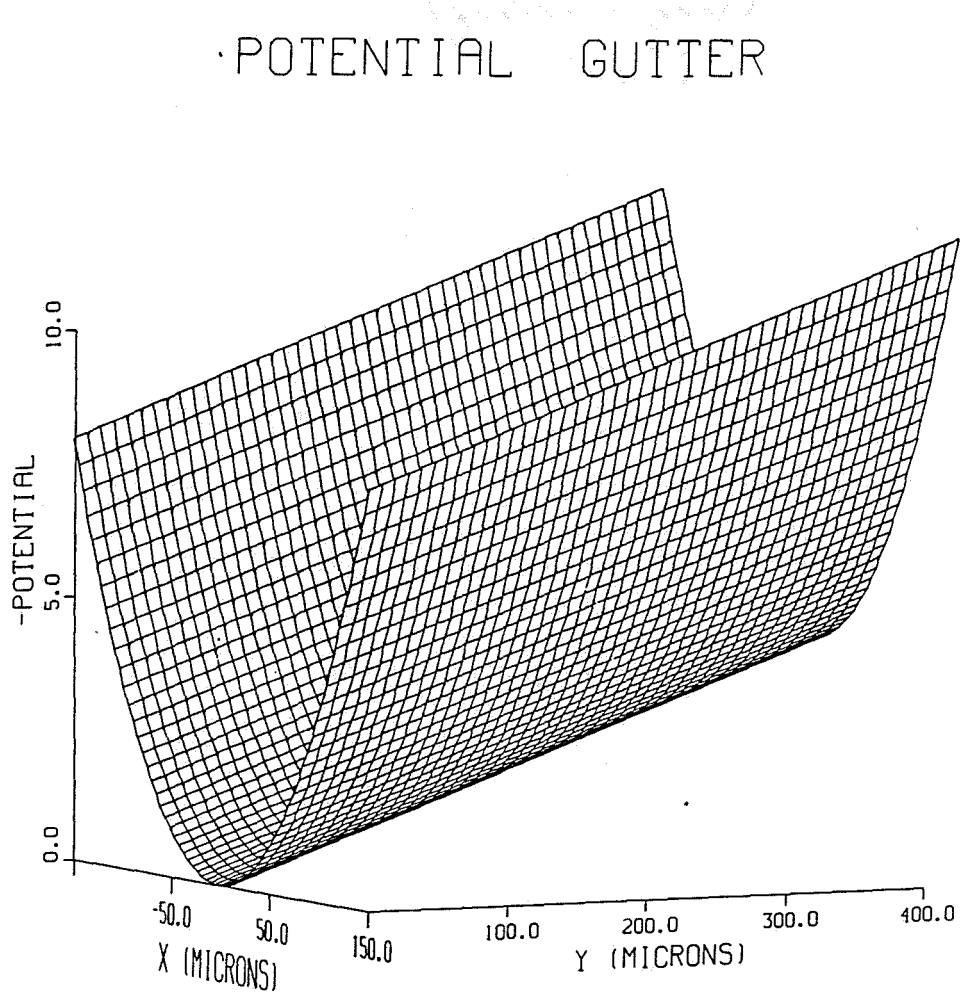


Fig. 3. The potential of a fully depleted silicon wafer when an additional linear field along the y-axis was superposed. The field stabilizes the full depletion by sweeping continuously all charges away.

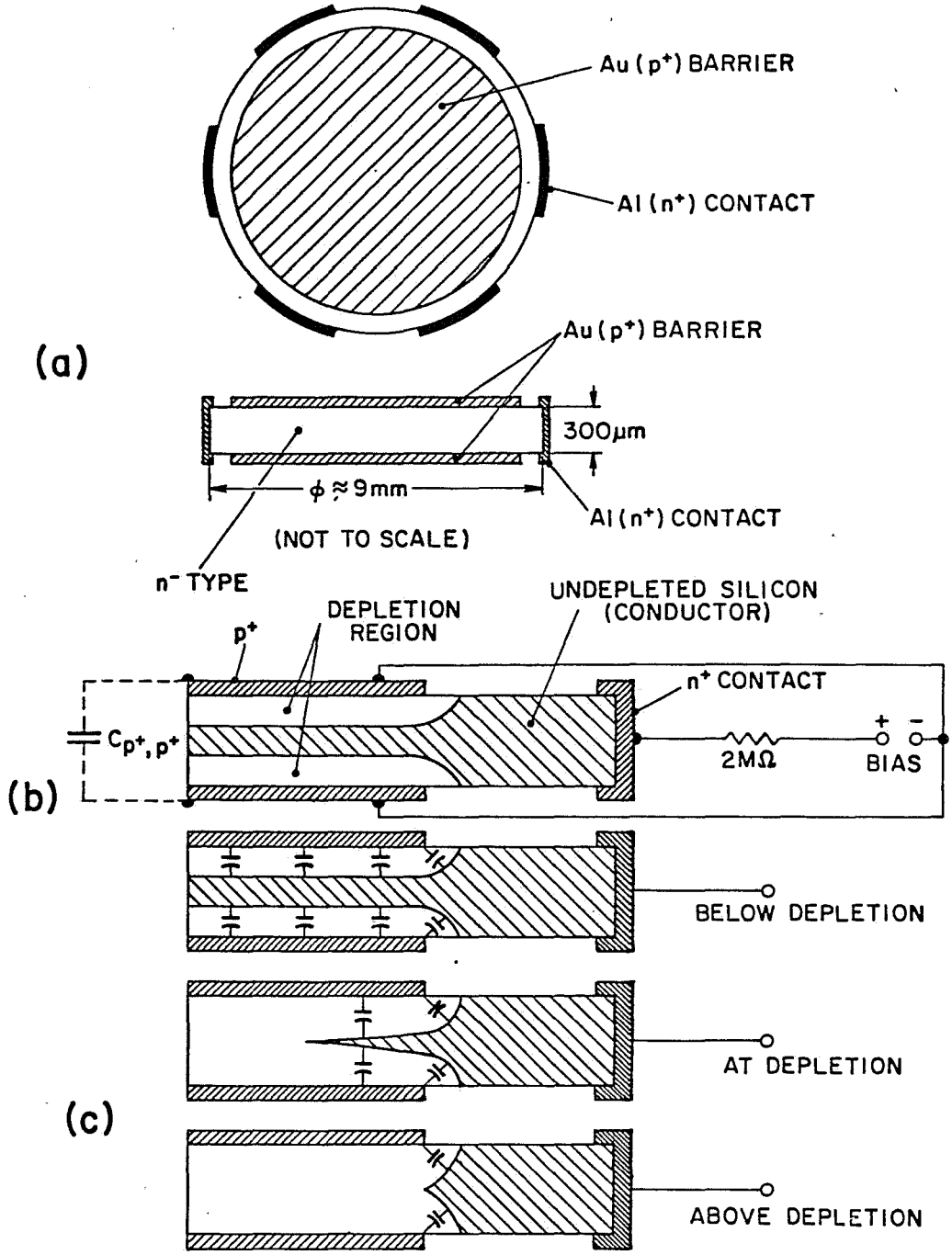


Fig. 4. a) Disc silicon device to test the mechanism of the depletion.

b) Connections to measure the capacitance between two p^+ junctions.

c) Behavior of the capacitance between p^+ junctions connected together and n^+ contact. At the bias voltage below the depletion voltage the capacitance is essentially that of the standard detectors in parallel (top). At full depletion the conductive channel retracts and the capacitance drops abruptly (center). At higher bias voltages the remaining capacitance is the much lower capacitance between the p^+ junction and the depleted silicon around (bottom).

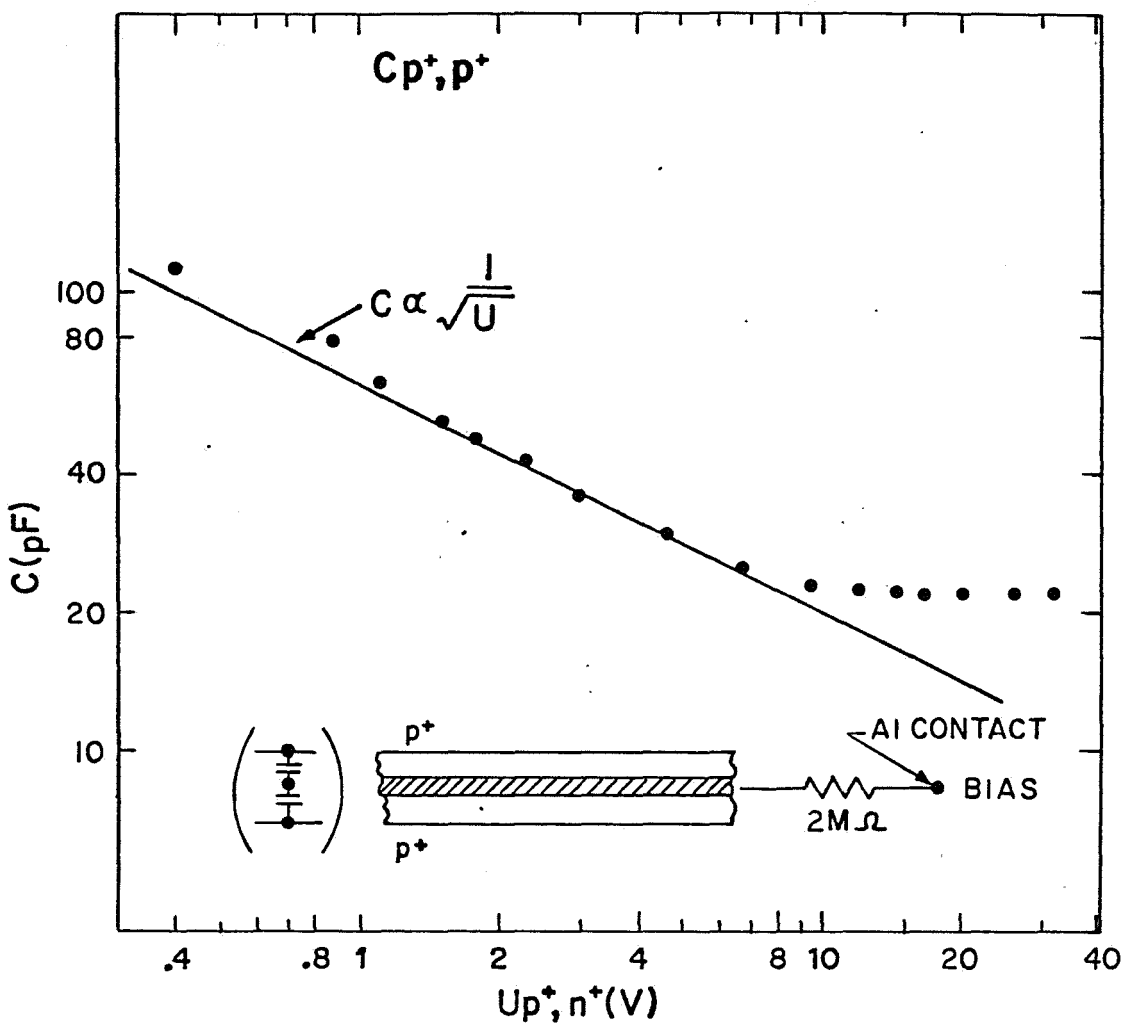


Fig. 5. Capacitance between two p^+ electrodes as a function of the bias voltage U. Solid line shows the expected $1/\sqrt{U}$ dependence for values of U below the depletion voltage.

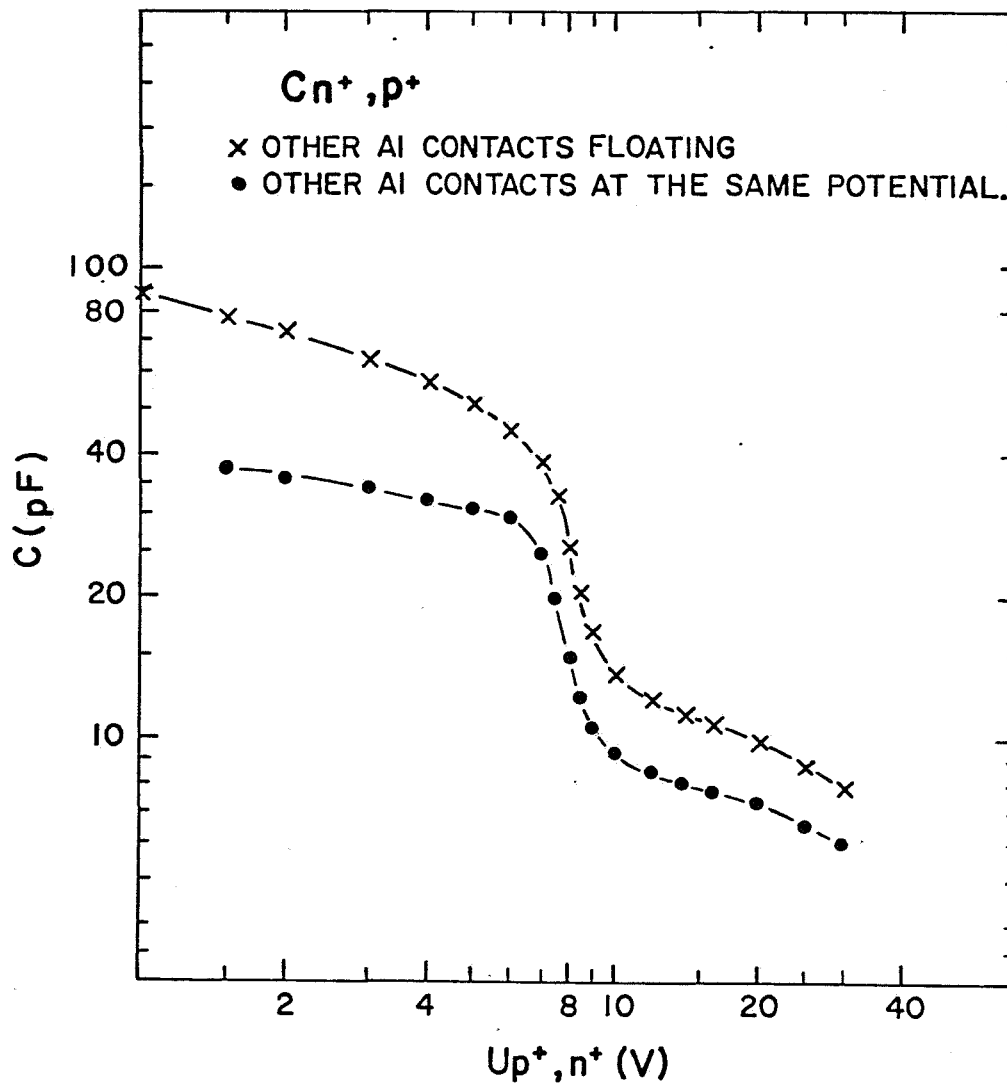


Fig. 6. Capacitance between two p^+ junctions connected together and all n^+ contacts as a function of the bias voltage. The abrupt drop of the capacitance at the depletion voltage is clearly visible.

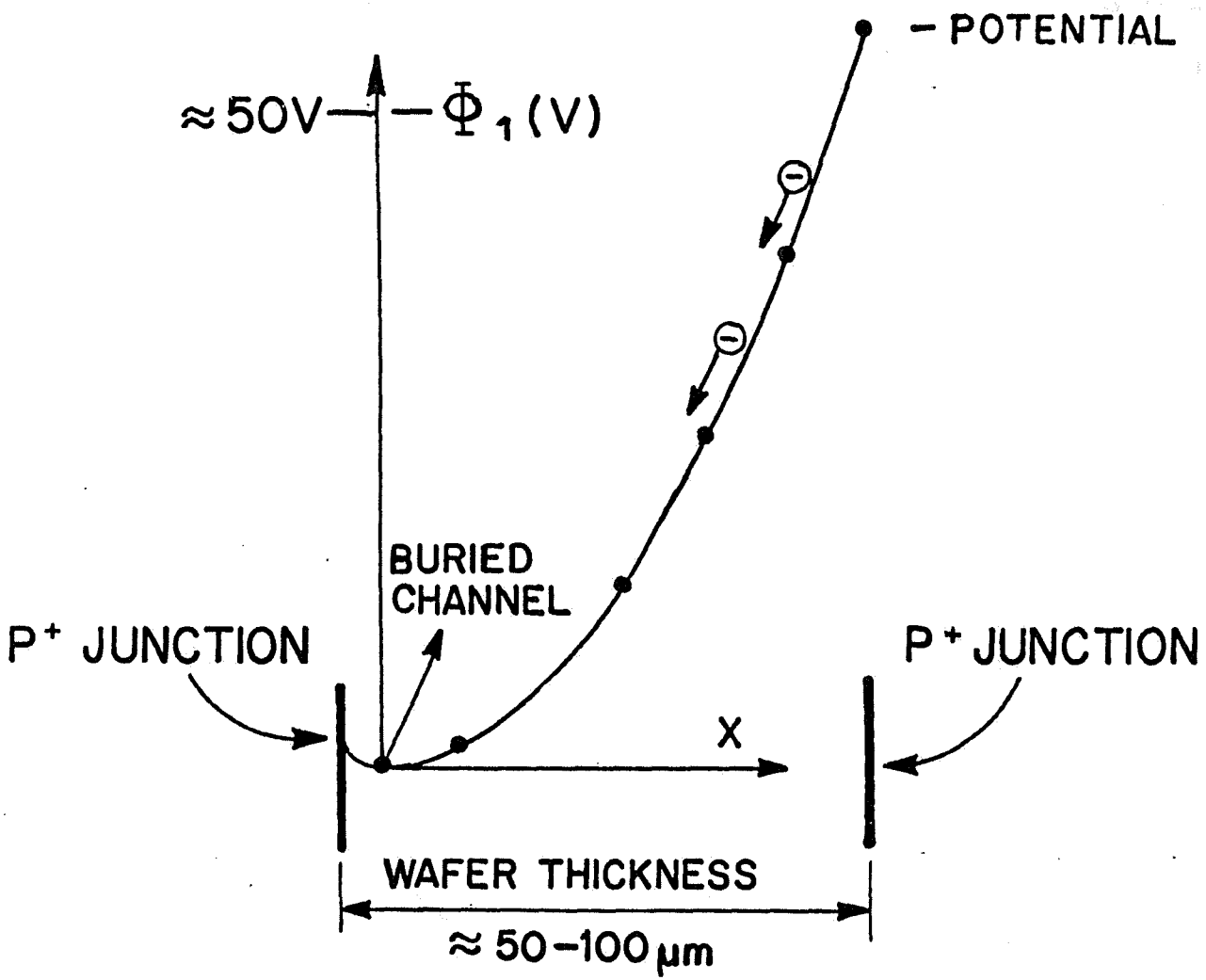


Fig. 7. Potential across a fully depleted CCD wafer. Electrons produced by ionization fall rapidly into the potential energy minimum. Then they are transported in buckets as in a standard BCCD.

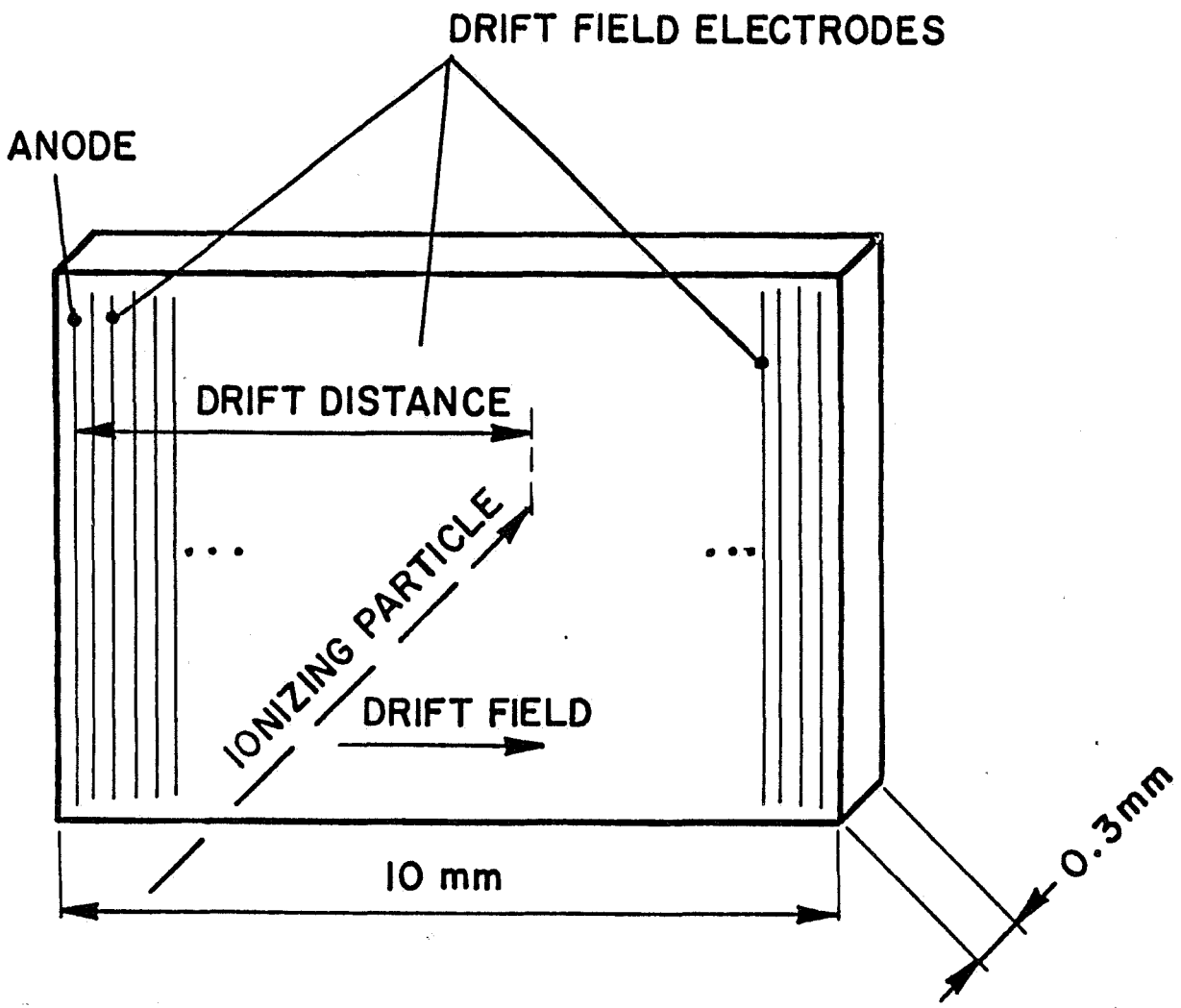


Fig. 8. Silicon Drift Chamber. The wafer is about .3 mm thick and has a front area of few cm^2. The surface is covered by a strip array of p^+ junction electrodes which provides the depletion and the drift field. (Only junctions at the extremes of the wafer are shown.) Electrons produced by the passage of a fast charged particle drift toward the anode which is the only readout channel on the wafer.

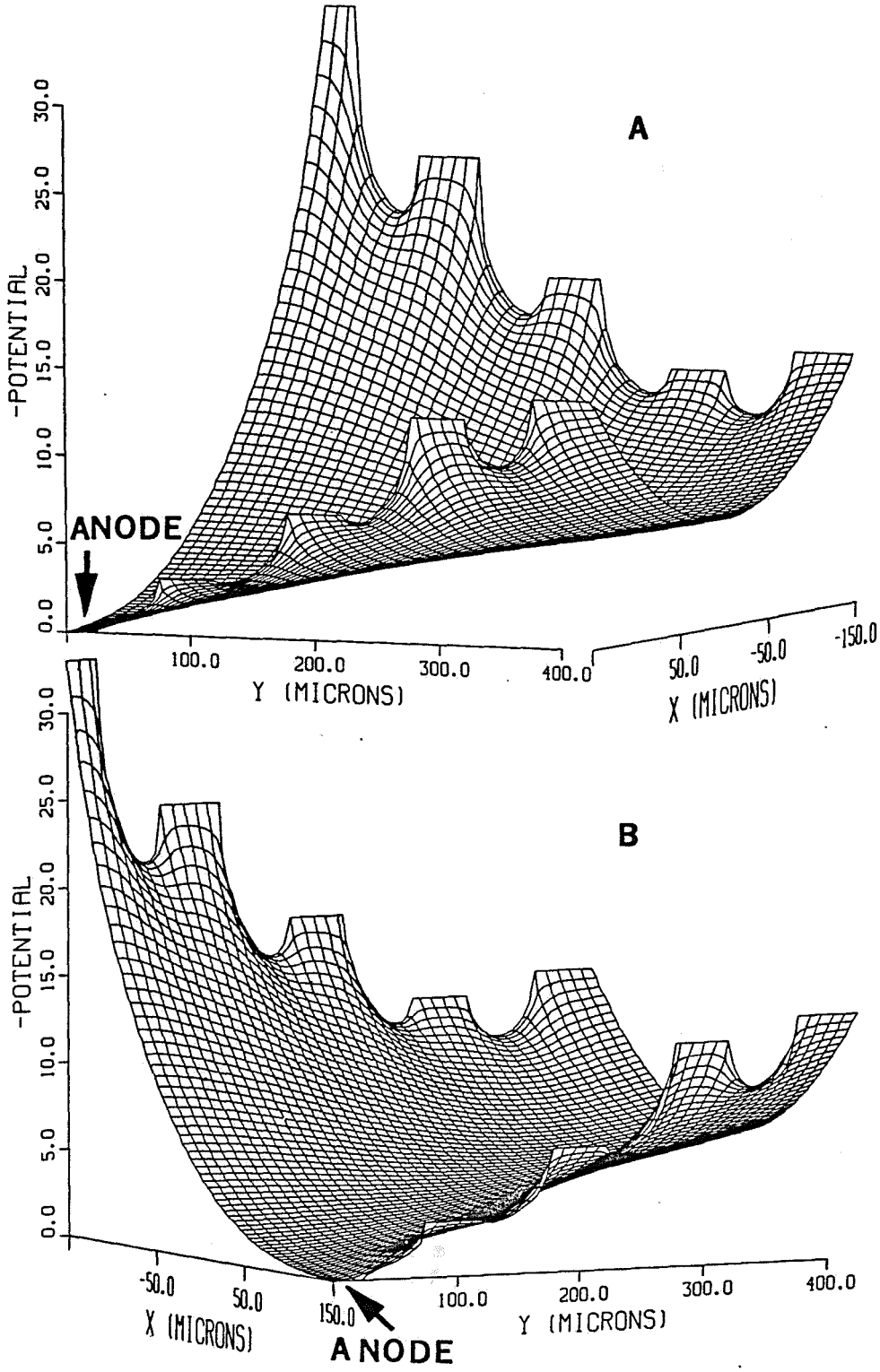


Fig. 9. a,b. The potential within the Semiconductor Drift Chamber close to the readout anode. The p^+ junctions on the back side of the wafer (opposite the anode) are biased to a higher negative potential while the junctions on the anode side of the wafer are biased less negatively. Consequently the bottom of the channel turns and electrons move toward the anode. (Two views of the same potential from different points are shown.)

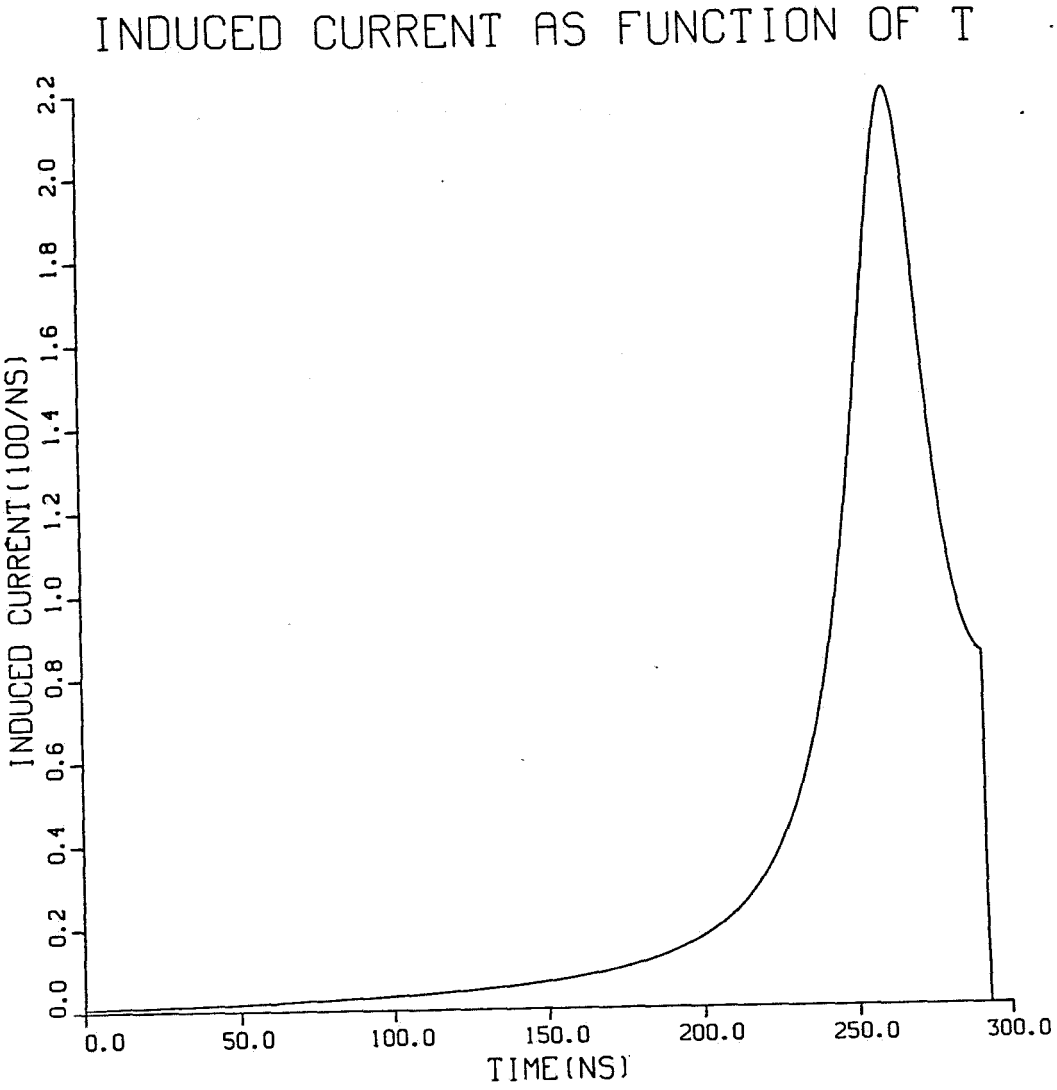


Fig. 10. Current induced on the anode of a Silicon Drift Chamber having the geometry of Fig. 8 and an electric potential shown in Fig. 9. Unit charge moves with the y-component of velocity equal to 1.3 μm/ns. The main portion of the signal is induced when the distance of the moving charge from the anode is equal approximately to the anode width.