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Mismatch and Retention Time Analysis of DRAMs Down to 4 K

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Abstract. This paper explores the retention time (RT) properties of dynamic random-access memory (DRAM) arrays at cryogenic temperatures (4 K). We provide an in-depth examination of leakage sources to elucidate RT behaviour across different temperatures, and we conduct a study on the mismatch between DRAM cells, highlighting various trade-offs, including cell area, mismatch, retention time, and power consumption. Our findings offer valuable insights for circuit designers working on large-scale quantum computing or superconducting nanowire single-photon detectors (SNSPDs) arrays, especially those aiming to store data at 4 K to avoid the wiring bottleneck associated with outputting each pixel from 4 K to room temperature for data analysis.

1. Introduction

The development of large-scale superconducting nanowire single-photon detector (SNSPD) arrays is driven by their high detection efficiency (DE) and low dark count rate (DCR), making them ideal for imaging applications. However, scaling to thousands of pixels presents challenges, particularly in connecting cryogenic pixel outputs to room temperature electronics. As pixel counts grow, power consumption becomes a limiting factor. SNSPD signals, typically in the microvolt range, require amplification via low-noise amplifiers (LNAs), either per pixel or through multiplexing for power efficiency [1].

Efficient data storage and retrieval are crucial for maintaining spatial resolution and determining hit locations within the array. As scalability increases, memory-related power consumption becomes significant, especially in high-speed applications. When SNSPDs operate as detectors rather than imagers [2], a Time-to-Digital Converter (TDC) is required to timestamp photon arrivals [3]. Since continuous data streaming is impractical, timing information must be stored in memory. This study focuses on designing a compact, energy-efficient memory system to mitigate pitch constraints in SNSPD arrays.

In large arrays, many pixels may remain inactive, reducing efficiency. Static random-access memory (SRAM), shown in Fig. 1(c), offers fast access speeds but is power-intensive and unsuitable for cryogenic applications [4]. Dynamic random-access memory (DRAM) [5], depicted in Fig. 1(b), provides higher density with fewer transistors per cell but requires periodic refreshing, leading to higher power consumption. Understanding DRAM retention time (RT) at 4 K is essential for reducing power consumption.

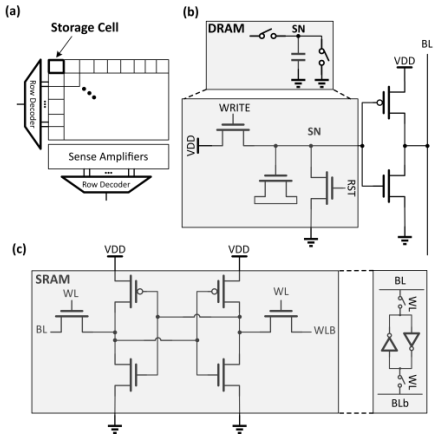

Figure 1. The two main types of solid-state memories: (a) The multiplexing scheme for the DRAM array testing, (b) the proposed DRAM cell, (c) a conventional 6T SRAM cell.

2. Measurements Methodology

The DRAM cell's working principle is illustrated in Fig. 2. Testing begins with discharging the memory (i.e., the storage capacitor) from node S_N (WRITE0 operation). Leakage from VDD to the capacitor may slightly increase V_{SN}, causing potential errors. Conversely, writing a logic 1 momentarily activates the WRITE transistor, significantly increasing V_{SN}, though leakage to the substrate may eventually lower it. The duration for which DRAM retains data, known as retention time, and its temperature dependence are discussed in Section 3. A digital buffer, shared among multiple pixels on the same readout line, enables characterization of multiple DRAMs while minimizing IOs. Characterization is performed using a Xilinx 7360 SoC FPGA, which generates read, write, and clear sequences for the DRAM die inside a CRX-4K cryogenic probe station (Lake Shore). This closed-cycle cryostat allows temperature sweeps from 293 K to 4 K. The DRAM array chip micrograph is shown in Fig. 3, with a 1.3 mm × 0.97 mm die containing 9 DRAM cells fabricated using SG13G2 BiCMOS technology (IHP). This process, characterized down to 4 K, has demonstrated strong DC, RF, and noise performance, making it viable for large quantum computing arrays [6]. Many quantum computing building blocks have shown reliable 4 K operation using this BiCMOS technology [7], [8]. To gather sufficient statistics for the retention time mismatch study in Section 3, tests were conducted on 10 different dies.

The cryogenic test setup, including the probe station, power supply, and control PCB, is highlighted in Fig. 3. The FPGA sequence configuration triggers a high read signal, initiating an internal counter that stops when the DRAM output falls below 600 mV. Digital voltage levels from 1 V to 1.4 V were applied to study their impact on retention time and variation across the array.

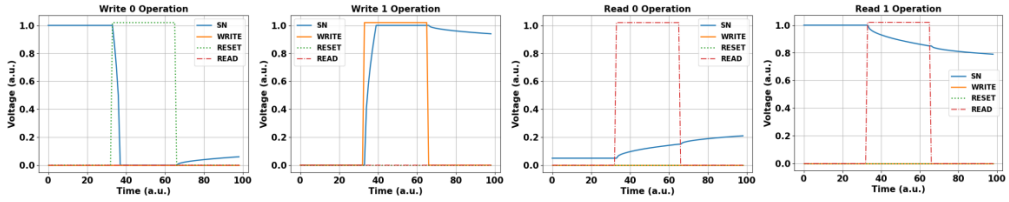

Figure 2. The characterization sequence of the proposed DRAM cell.

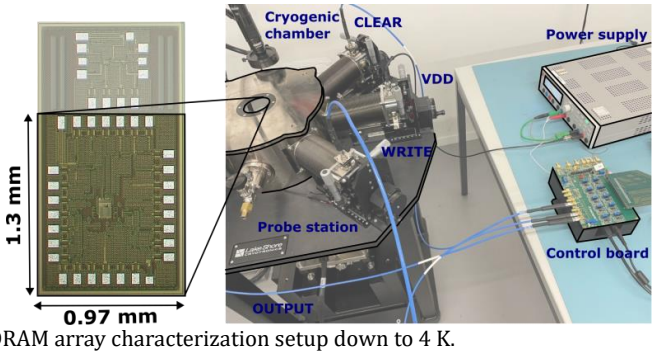

Figure 3. The DRAM array characterization setup down to 4 K.

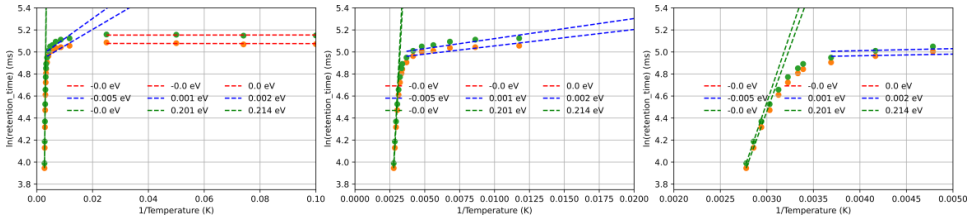

Figure 4. Retention time over temperature for the proposed DRAM cell with different temperature windows: Left: T ∈ [4 K, 350K], center: T ∈ [77 K, 350 K], right: T ∈ [200 K, 350 K].

3. Cryogenic Performance

At cryogenic temperatures (CT), CMOS transistors exhibit a steep subthreshold slope (SS) and low leakage currents, enhancing energy efficiency [9]. However, threshold voltage mismatch increases [10]. Recent studies have explored whether DRAMs can outperform SRAMs at 4 K, considering power consumption, retention time, and access latency [11]. DRAMs, traditionally valued for their density [12], demonstrate superior performance at 4 K due to significantly reduced leakage current. This advantage arises from their reliance on charge storage, unlike SRAMs, which require continuous power. Despite these benefits, DRAMs at 4 K face challenges, particularly retention time mismatch among cells. At CTs, retention time becomes highly sensitive to manufacturing variations and environmental factors. This study investigates this effect by analyzing 90 DRAM cells. The remainder of this paper is structured as follows: Section 3 discusses DRAM specifications, including retention time, mismatch, and power consumption, as functions of temperature. Section 4 presents experimental results on these parameters down to 4 K with some conclusions.

3.1 Retention time

The retention time of DRAM is highly temperature-dependent. Understanding this relationship is crucial for optimizing performance in cryogenic conditions. The leakage current follows an Arrhenius process, allowing retention time to be expressed as [13]:

$$\ln(T_{ret}) \propto \ln(I_{leak}) \propto \frac{E_a}{k_B T}, \tag{1}$$

where T is the chip temperature and k_B is the Boltzmann constant. DRAM leakage is impacted by three temperature-dependent mechanisms, with activation energy (E_a) acting as an adjustable factor. To identify the dominant leakage mechanism at a given temperature, E_a is extracted from Fig. 4, considering subthreshold leakage, gate-induced drain leakage (GIDL), and junction leakage [14]. A linear fit of $\ln(T_{ret})$ vs. temperature T allows E_a extraction, averaging contributions from the three leakage types. Characterization is performed at 1.2 V, 1.3 V, and 1.4 V. At 1.2 V, a high

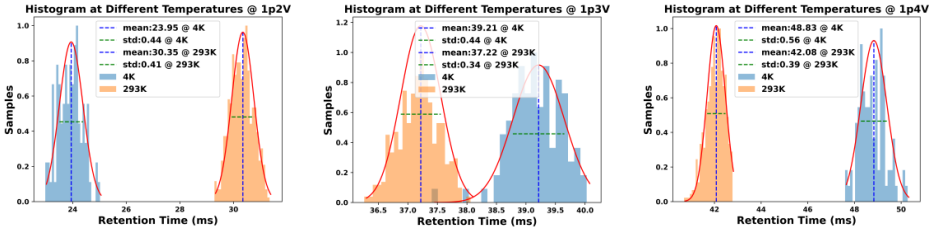

Figure 5. Single cell retention time histogram at 4 K and 293 K for three distinct supply voltages.

failure rate limits statistical accuracy due to an increase in transistor threshold voltage (V_{th}). For 1.3 V and 1.4 V, three distinct fitting regions are summarized in Table 1. The expected value for the subthreshold leakage E_a can be expressed as [11]:

$$E_{a,sub} = ln(10)k_b \frac{V_{th}(0)}{SS_0}, \quad (2)$$

where $V_{th}(0)$ is the extrapolated threshold voltage at 0 K and SS_0 is the linearized temperature dependence of the subthreshold slope. Based on CMOS transistors characterized down to 4 K, $V_{th}(0) \approx 0.7$ V and $SS_0 \approx 60$ mV/dec at 293 K, yielding an analytical $E_a \approx 0.231$ eV, consistent with values in Table 1. This suggests subthreshold leakage dominates within this temperature range, but its influence diminishes at lower temperatures, where GIDL and junction leakage emerge with minimal temperature dependence [11].

3.2 Mismatch

Transistor mismatch at cryogenic temperatures (4 K) significantly impacts storage cell design. Two types of mismatch exist:

1. Systematic mismatch, arising from any asymmetry between pair of devices or opposing drain current directions [10], mitigated through layout design. In this design, a transistor pair is used within a single cell, making it particularly relevant at 4 K.
2. Random mismatch, resulting from fabrication-induced variations like Random Dopant Fluctuation (RDF), Line Edge Roughness (LER), and Oxide Thickness Variation (OTV), leading to pixel-to-pixel and in-pixel retention time mismatch.

Equation (2) identifies subthreshold leakage as the dominant leakage path in Region 3 (209 K < T < 360 K). The remaining source of retention time mismatch in Equation (1) is the threshold voltage extrapolated at 0 K, which varies significantly at CTs [10], [15], [16]. To model these variations, Pelgrom's law and the Croon model, validated at room temperature, also accurately

Table 1. The activation energy (E_a) extraction based on the section fits in Fig. 4.

	Activation Energy (E_a) [eV]	
	VDD = 1.3 V	**VDD = 1.4 V**
Region 1: 4 K < T < 10 K	0.0	0.0
Region 2: 13 K < T < 178 K	0.001	0.002
Region 3: 209 K < T < 360 K	0.201	0.214

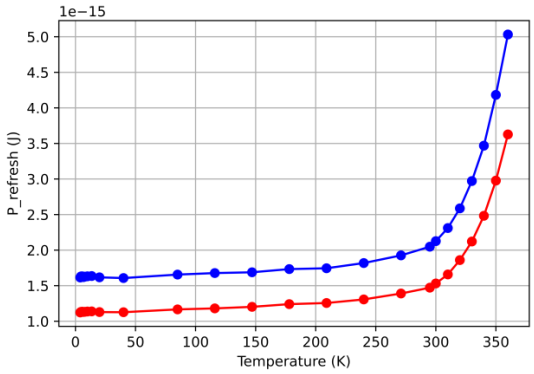

Figure 6. The estimated dynamic power of a single DRAM cell for two different supplies as a function of temperature: 1.3 V (red), 1.4 V (blue).

predict mismatch at 4 K based on device area and bias conditions [10]. Pelgrom's law describes the area dependence of threshold voltage and transconductance variability as [18]:

$$\sigma_{\Delta V_{TH}} = \frac{A_{VTH}}{\sqrt{WL}}, \tag{3}$$

where A_{VTH} is technology-dependent, and W·L is the device's active area. Studies show a minor increase in threshold voltage mismatch at 4 K, due to the increase in A_{VTH} [15].

3.2.1 Mismatch mitigation

One approach to reducing threshold voltage mismatch at CTs is enlarging transistors, but this increases cell size, limiting large-scale integration. An alternative is Fully Depleted Silicon-On-Insulator (FDSOI) technology, which exhibits lower threshold voltage variability at CT than bulk CMOS at room temperature , due to reduced dopant fluctuations [17].

3.3 Power Consumption

The dynamic power consumption of DRAM, approximated by the power needed to refresh the charge-storing node, is given by:

$$P_{refresh} = \frac{1}{f_{refresh}} \cdot C_{SN} \cdot V_{DD}^2, \tag{4}$$

where $f_{refresh} = 1/T_{retention}$, $C_{SN} \approx 100$ fF in the current design, while V_{DD} is the digital power supply. Assuming C_{SN} remains stable at CTs, a drop by a factor of 3.5 is observed in terms of dynamic power consumption at 1.4V, with a similar reduction at 1.3 V**.** This drop is illustrated in Fig. 6.

4. Results and Discussion

At 4 K, the expected threshold voltage increase requires an elevated VDD (≥1.2 V) for operation. As shown in Fig. 5, two opposing effects influence retention time: the decrease in subthreshold leakage and the increase in threshold voltage. This is analyzed at 1.2 V, 1.3 V, and 1.4 V for 293 K and 4 K. At 4 K, retention time halved at 1.2 V. When supplied at 1.3 V, retention time increased by 200%, while at 1.4 V, it increased by approximately 225%. Mismatch analysis of the 90-pixel array was conducted by measuring retention time deviations across multiple acquisitions. As shown in Figs. 7 and 8, at room temperature, the standard deviation σ ≈ 0.28 ms, independent of VDD. After

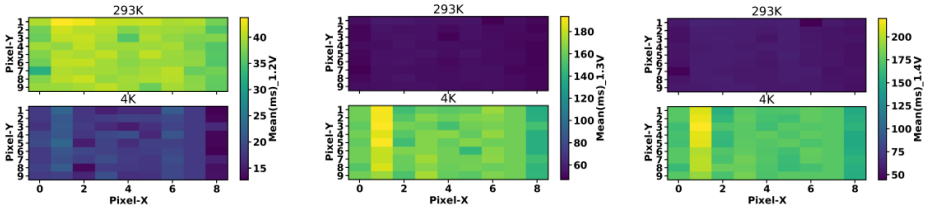

Figure 7. The DRAM array retention time distribution at both 4 K and 293 K for three different supply values (1.2 V, 1.3 V, and 1.4 V).

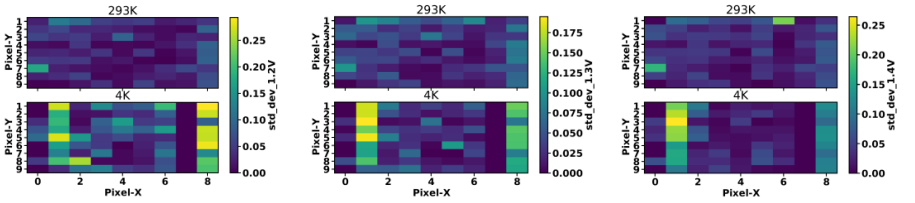

Figure 8. The DRAM array pixel-to-pixel retention time mismatch at both 4 K and 293 K for three different supply values (1.2 V, 1.3 V, and 1.4 V).

cooling, mismatch increased by 100% at 1.2 V, 25% at 1.3 V, and 100% at 1.4 V. These findings provide crucial insights into DRAM retention time and mismatch behavior at cryogenic temperatures, essential for quantum computing and SNSPD arrays operating around 4 K.

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