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LEB Ring Magnet Power Supply System Voltage and Current Regulation Design

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I. INTRODUCTION

The Supreconducting Super Collider complex includes a cascade of accelerators. Among them, the Low Energy Booster (LEB) is a 0.54 km circumference synchrotron in which protons are accelerated from 1.2 GeV/c to 12 Gev/c [1].

The LEB power system has to operate in either of two modes,10 Hz biased sine wave and a linear ramp mode. The maximum and minimum current flowing through the magnets has to be regulated, in both operational modes, within 100 ppm of the actual current. The LEB magnet system consists of 48 dipoles and 90 quadrupoles connected in series circuit.

For 10 Hz biased sine wave operation, dipoles and quadrupoles magnets resonate with 12 distributed capacitors [1][2]. The capacitors are bypassed by a 40 mHy choke to provide a path for the d-c component of the magnet current. The system is shown schematically in figure I.1.

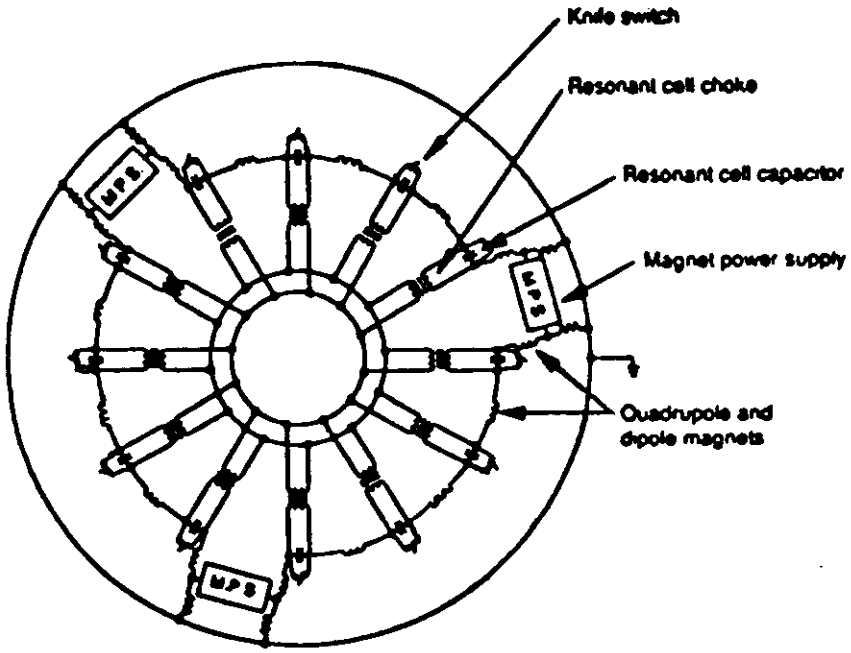


Fig. I.1. LEB Ring Magnet Power System

Three 12-pulse SCR phase-controlled power supplies are inserted into the ring to produce both current waveforms. The knife switches are closed for linear ramp mode and opened for 10 Hz biased sine wave.

The regulation system consists of two major loops; an internal one controlling the output voltage of each power supply and an external one controlling the current in the magnets. Each power supply has its own voltage loop and output filter. The voltage loop is designed to have a high frequency response and its main function is to regulate the voltage applied to the magnets. It must follow a predetermined voltage reference related to the current reference, rejecting line voltage changes, offset errors and other voltage perturbations. The external loop is the magnet current regulator. It has relatively low frequency response and very high gain in order to meet the dc accuracy requirements. A block diagram of the power supply including both mayor loops is shown in figure I.2.

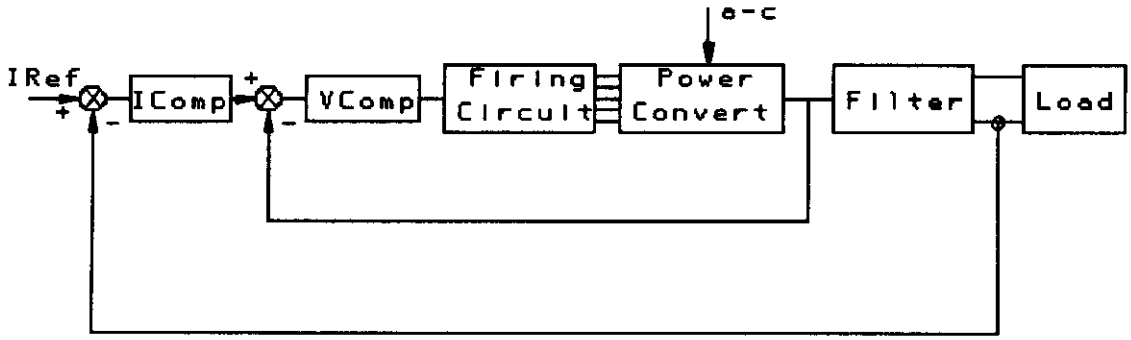


Fig.I.2 Block diagram of LEB power supply regulation loops

The same voltage loop is used for both operation modes but two different current regulation loops are needed. Voltage and current loops design for both operational modes are described in section II to IV, while section V is devoted to the firing circuit.

II. VOLTAGE LOOP DESIGN

II.1. Introduction

The aim of the voltage loop is to provide enough rejection to a-c voltage perturbations and to reduce the influence of the subharmonics of the sampling frequency (720Hz) that could be generated by the thyristor bridge converter. Due to bandwidth limitations, the voltage loop only rejects voltage perturbations up to 120 Hz while the output filter rejects the ripple at 720 Hz and other higher frequencies perturbations. Output filter and voltage loop have been designed in order to obtain less than 1% total output voltage deviation:

Total Output Voltage Deviation $\delta V/V_{max}$, Max. = 1%

Different voltage perturbations considered, filter and voltage loop attenuations and remaining deviation in power supply output voltage, are shown in table II.1

Table II.1

		Filter Attenuation	Voltage Loop Attenuation	Voltage Deviation
a-c Voltage Ampl. Perturb.	±5%	----	40dB	.1%
Phase Imbalance	±1%, 60Hz	----	20dB	.2%
	±1%,120Hz	----	20dB	.2%
	±1%,360Hz	20dB	----	.2%
Voltage Ripple at Conv. Output	25%,720Hz	50dB	----	.1%
Total PS Output Voltage Deviation				< 1%

II.2. Passive Output Filter

The designed output filter, presenting a bandwidth of 100Hz and a band tramped at 720Hz is shown in figure II.1 while the corresponding amplitude frequency response is shown in figure II.2.

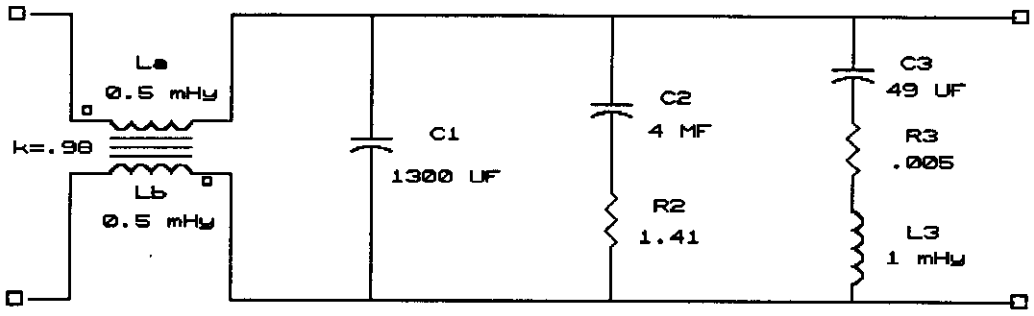


Fig.II.1 Passive Output Filter

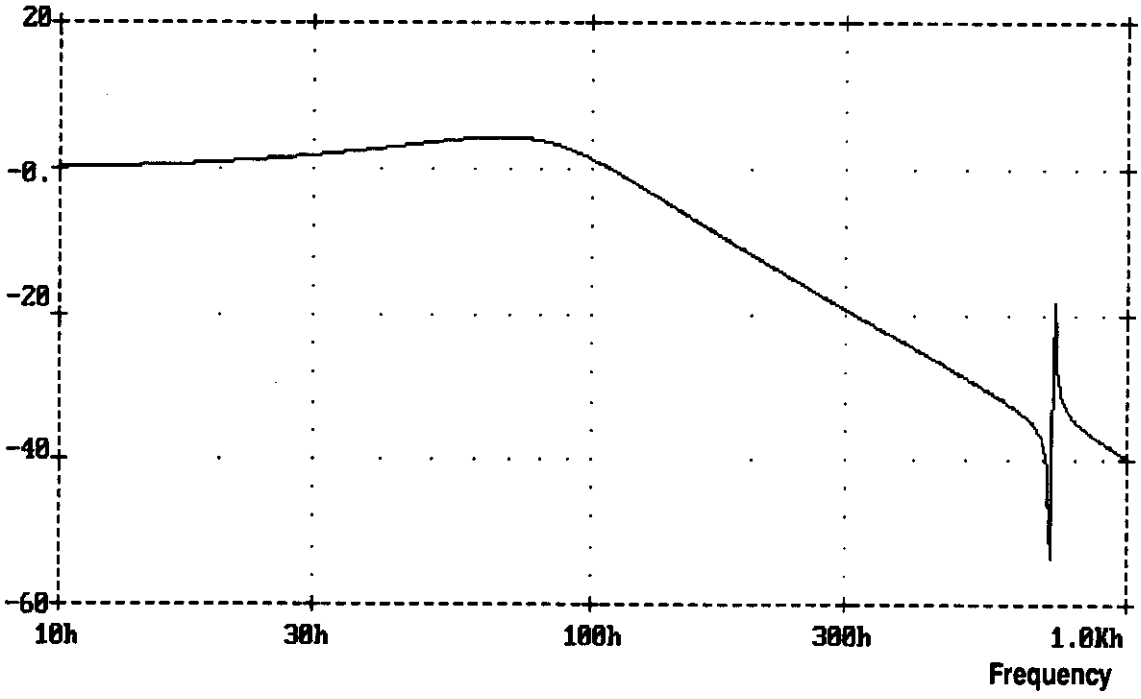


Figure II.2
Amplitude Response of the Output Filter

II.3. Voltage Loop Design

The schematic diagram of the voltage loop including output passive filter and the magnetic load is shown in figure II.3. Where V_r and V_p represent voltage reference and voltage perturbations respectively.

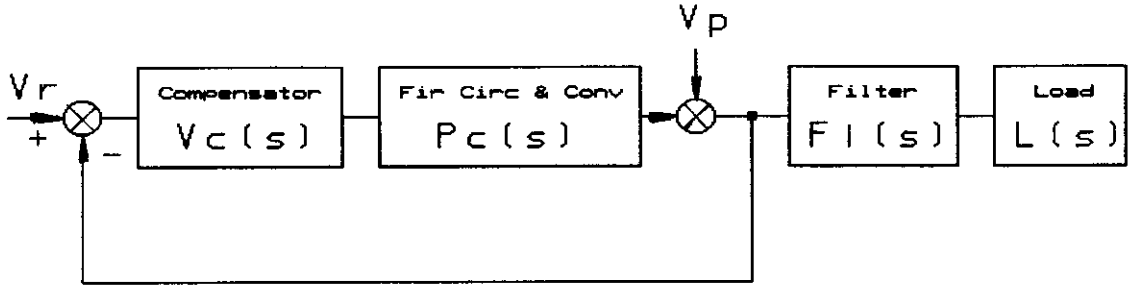


Fig.II.3 Block diagram of the voltage loop

A first step to design a regulation loop is to obtain a mathematical expression representing the plant under control. In this case it is necessary to derive a model for the firing circuit and 12-pulse power converter. The available control is the firing angle of each thyristor. Thus, we are in presence of a switching system where the sampling frequency, depending on a-c supply frequency and power converter characteristics, takes a value of f_o = 720 Hz.

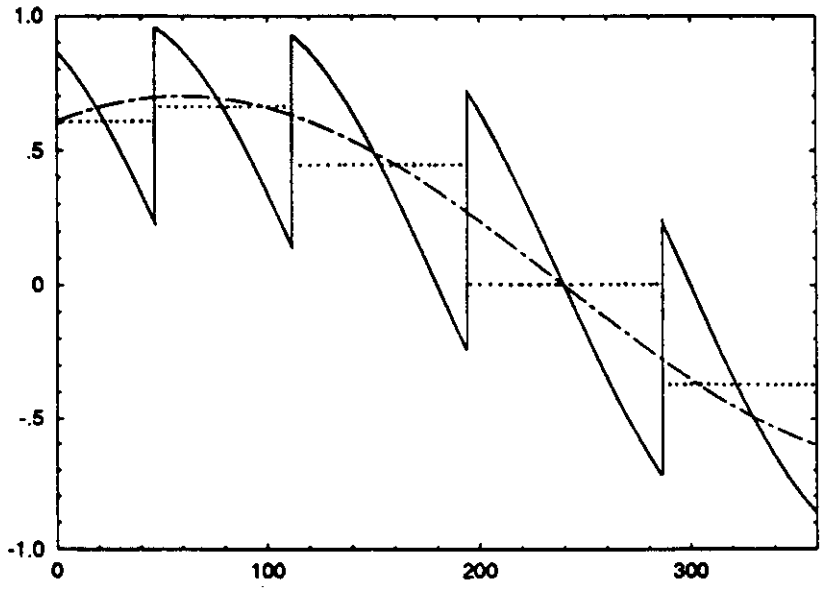


Fig. II.4 —· voltage reference
— voltage output
··· model output

The model is derived with the help of figure II.4 where have been represented an arbitrary voltage reference signal and the d-c terminal voltage of an ideal firing circuit and power converter.

A simple way for modeling this nonlinear system is to use an f_o frequency sampler and a zero order hold. The output of this model has be represented in dot line in figure II.4 and its transfer function is given by

$$P_c(s) = \frac{(1-e^{-sT})}{sT} = e^{-sT/2}\,\frac{(e^{sT/2}-e^{-sT/2})}{sT} \tag{1}$$

For low frequencies, equation 1 can be approximated by

$$P_c(s) \approx e^{-sT/2} \tag{2}$$

Thus, in the low frequency band, the ideal firing circuit and bridge converter has unitary gain and linear phase. This linear phase, taking a value of -90° at 360Hz, affects the loops stability and limits the maximum voltage loop bandwidth at about 200Hz. Output filter and load are not inside the voltage loop having non impact on loop stability.

A basic voltage compensator has been design in order to have an open loop d-c gain of 100 and a phase margin frequency of about 100Hz. The resulting transfer function for the basic compensator is given by

$$V_{cb}(s) = \frac{A}{1+s\tau_v} \tag{3}$$

where A=100 and τ_v=.16. With this basic compensator, d-c gain requirement is fulfilled and gain and phase margins have adequate values. Nevertheless, gain loop is not enough in order to reject 60Hz and 120Hz perturbations. Thus, the gain loop has to be increased at these two particular frequencies modifying as less as possible stability margins. These features can be obtained by adding to the basic compensator two passband amplifiers having at least 20 dB gain at 60Hz and 120Hz respectively.

The transfer function of the total compensator is given by

$$V_c(s) = \frac{A}{1+s\tau_v} + \frac{.25(1+\frac{s}{\omega_1})}{1+\frac{s}{Q\omega_1}+(\frac{s}{\omega_1})^2} + \frac{.25(1+\frac{s}{\omega_2})}{1+\frac{s}{Q\omega_2}+(\frac{s}{\omega_2})^2} \tag{4}$$

where A=100, τ_v=.16, Q=40, $\omega_1 = 2\pi\ 60$, and $\omega_2 = 2\pi\ 120$.

The gain and Q of both passband amplifiers have been chosen in such a way that the first term in equation 4, representing the basic compensator, was dominant at low and high frequency bands.

Figure II.5 shows gain and phase frequency response of the designed voltage regulation loop.

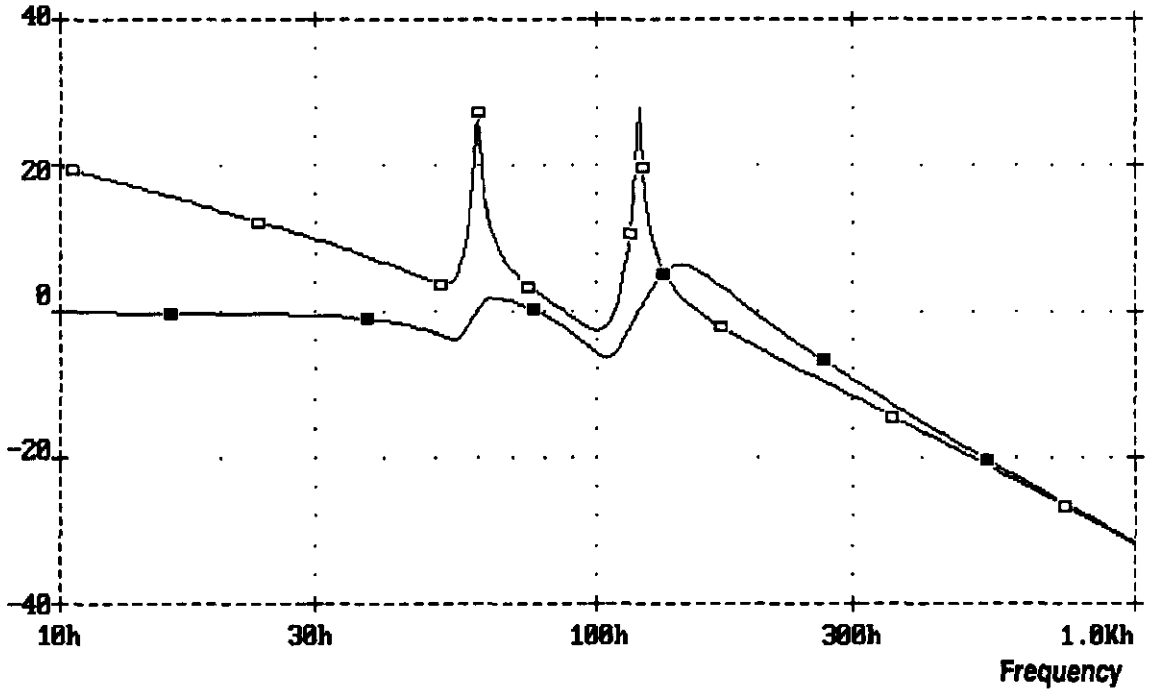


Figure II.5 a)
Gain/frequency response of the Voltage Loop
□ Open Loop, ■ Closed Loop

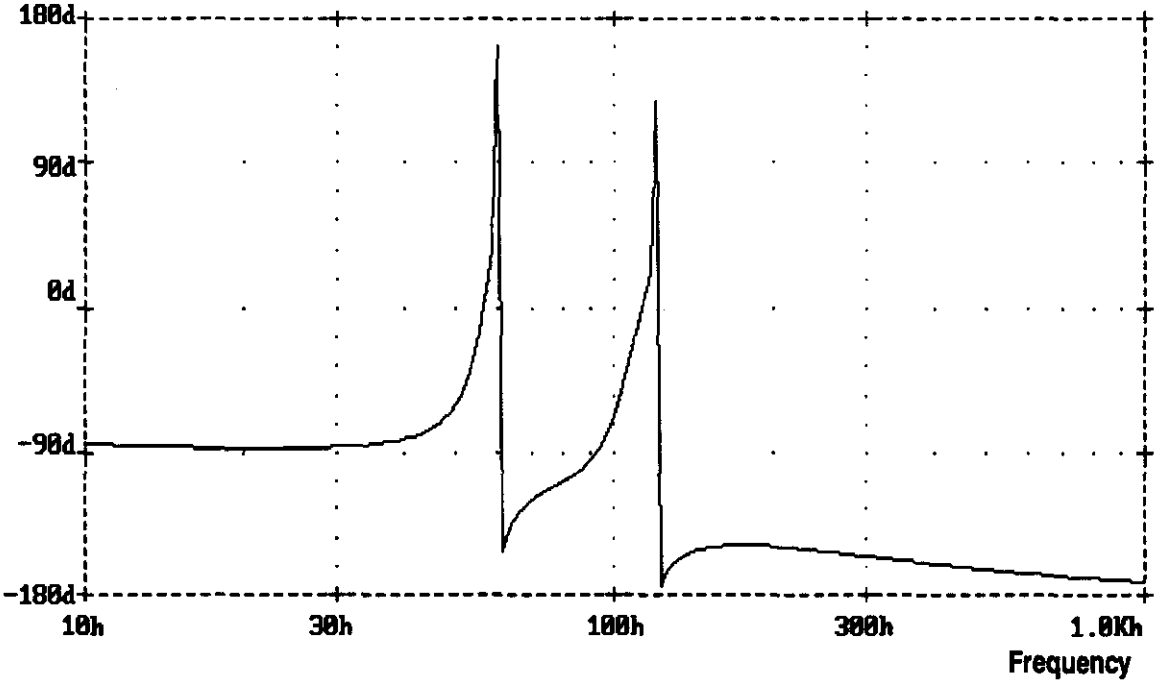


Figure II.5 b)
Open Loop Phase/frequency response of the Voltage Loop

The frequency response of power supply to a-c voltage perturbations and voltage ripple is shown in figure II.6.

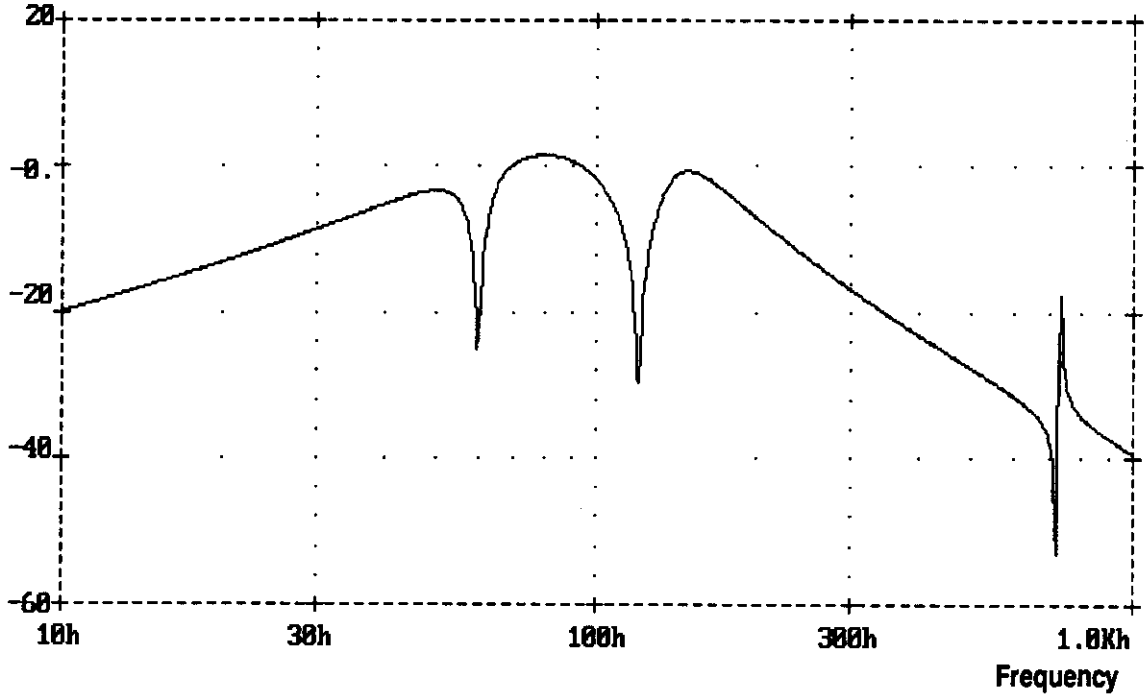


Figure II.6
Response of Power Supply to a-c voltage perturbations

II.4. Analog Implementation

The voltage compensator can be implemented using operational amplifiers in a parallel configuration in order to obtain the three terms of the corresponding transfer function (equation 4). An schematic diagram of the voltage loop implemented by operational amplifiers is shown in figure II.7 (Drawing AEB-3060005).

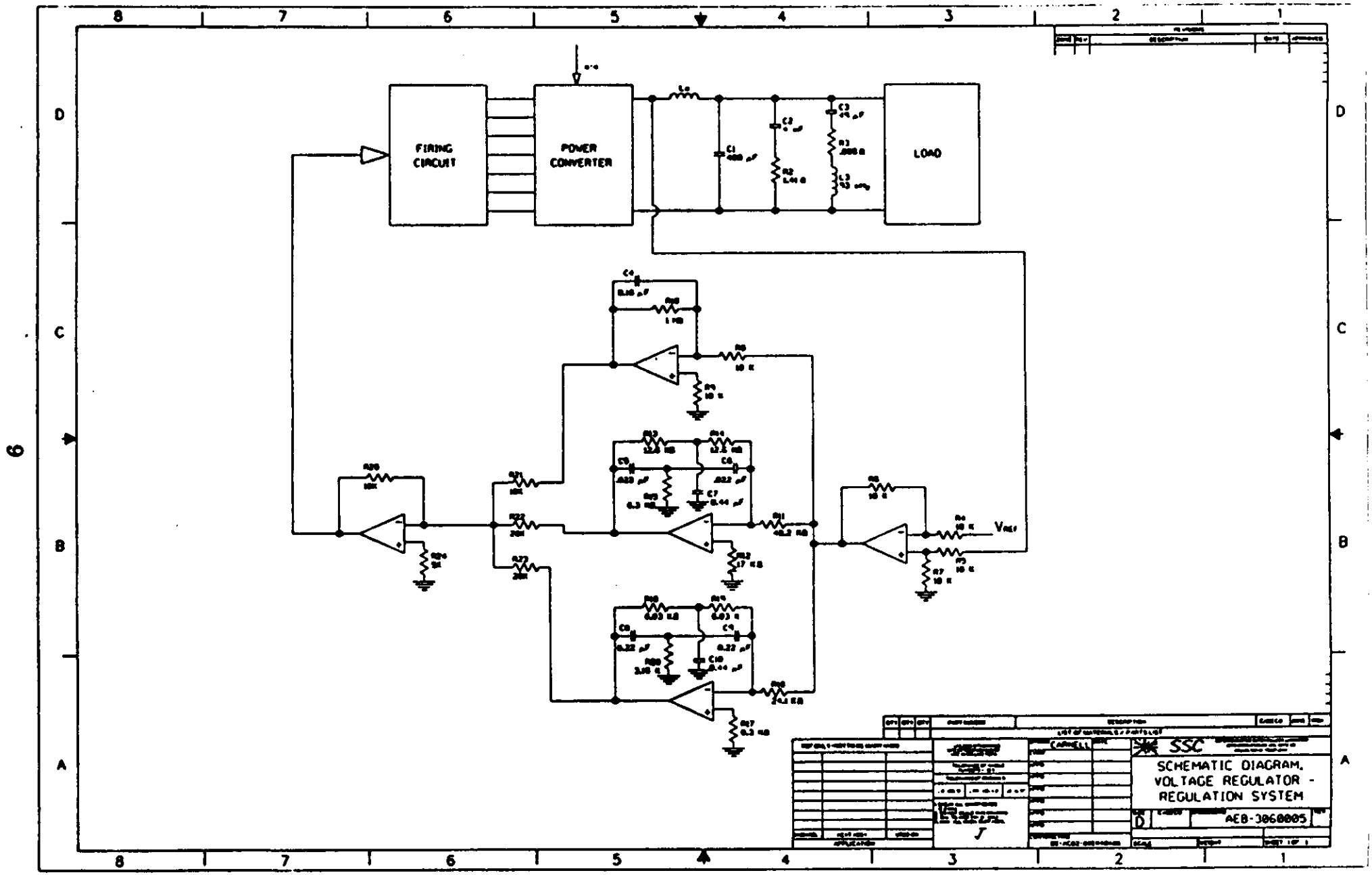


Figure II.7. Voltage Regulation System

II.5. Results and discussion

The LEB power supply voltage regulation loop has been simulated using Tutsim and Spice programs. An explanation about the simulations realized including computer programs can be found in appendixes A and B.

The frequency response of the voltage loop obtained with the Spice simulations have been shown in figures II.5 and II.6. From figures II.5. a) and b) the stability margins can be determined. The phase margin is about 30° at a frequency of 140Hz. As at high frequencies the phase is tangent to -180° the gain margin goes to infinity. this is due to the fact that the converter delay has been simulated with a first order pole.

The results obtained in appendix A width Tutsim/Fansim simulations are basically the same at those obtained with Spice simulations. In fact phase margin and frequency are the same. Nevertheless, with Tutsim/Fansim simulations, the delay introduced by the power converter is well simulated and gain margin and frequency can be determined. The gain margin obtained at a frequency of 300Hz has a value of about 10 dB. These two values are important; the frequency of 300Hz is the absolute maximum voltage loop bandwidth within stability conditions and 10 dB is the amount of gain loop increment that would just produce instability. Thus, maximum gain loop variations due to parameter changes and non-linear firing circuit behavior have to be carefully checked.

III - CURRENT LOOP DESIGN, LINEAR RAMP MODE

III.1. Introduction

The schematic diagram of the LEB ring magnet power system for linear ramp operation mode is shown in Figure III.1. The three power supplies have an output filter and voltage loop but only one of them has a current regulation loop. The reference current wave form is provided by the central computer. Figure III.2 shows a typical magnet current waveform under 1 Hz linear ramp mode.

The regulation requirements of the current are different during different sections of a cycle: Injection, Acceleration, Extraction and Invert. The most restrictive current regulation requirements occurs under constant load, either during the injection or extraction period. In the LEB the total magnet current deviation during both injection and extraction periods has to be less than 100 ppm of the actual current [3].

Total Deviation $\delta I/I$, Max. = 100ppm

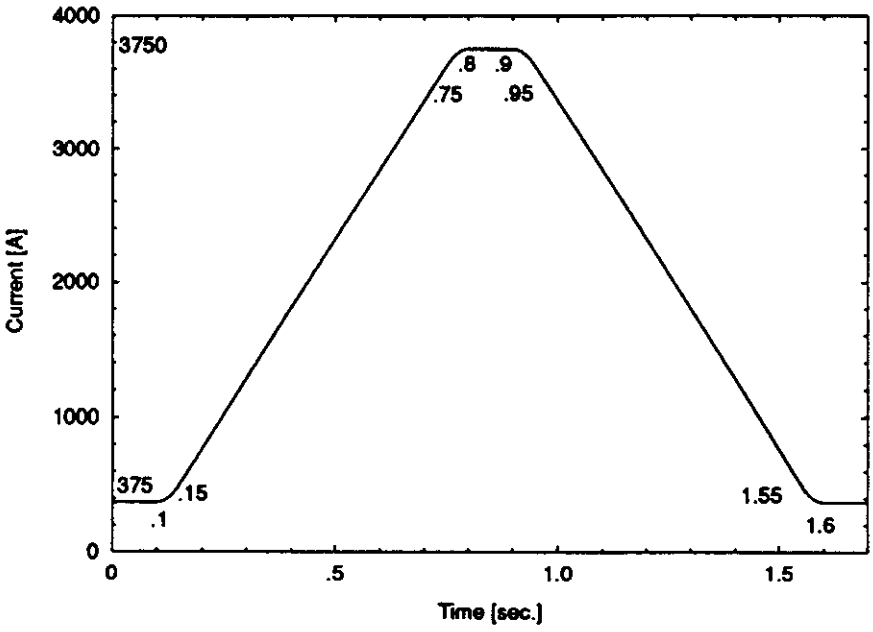
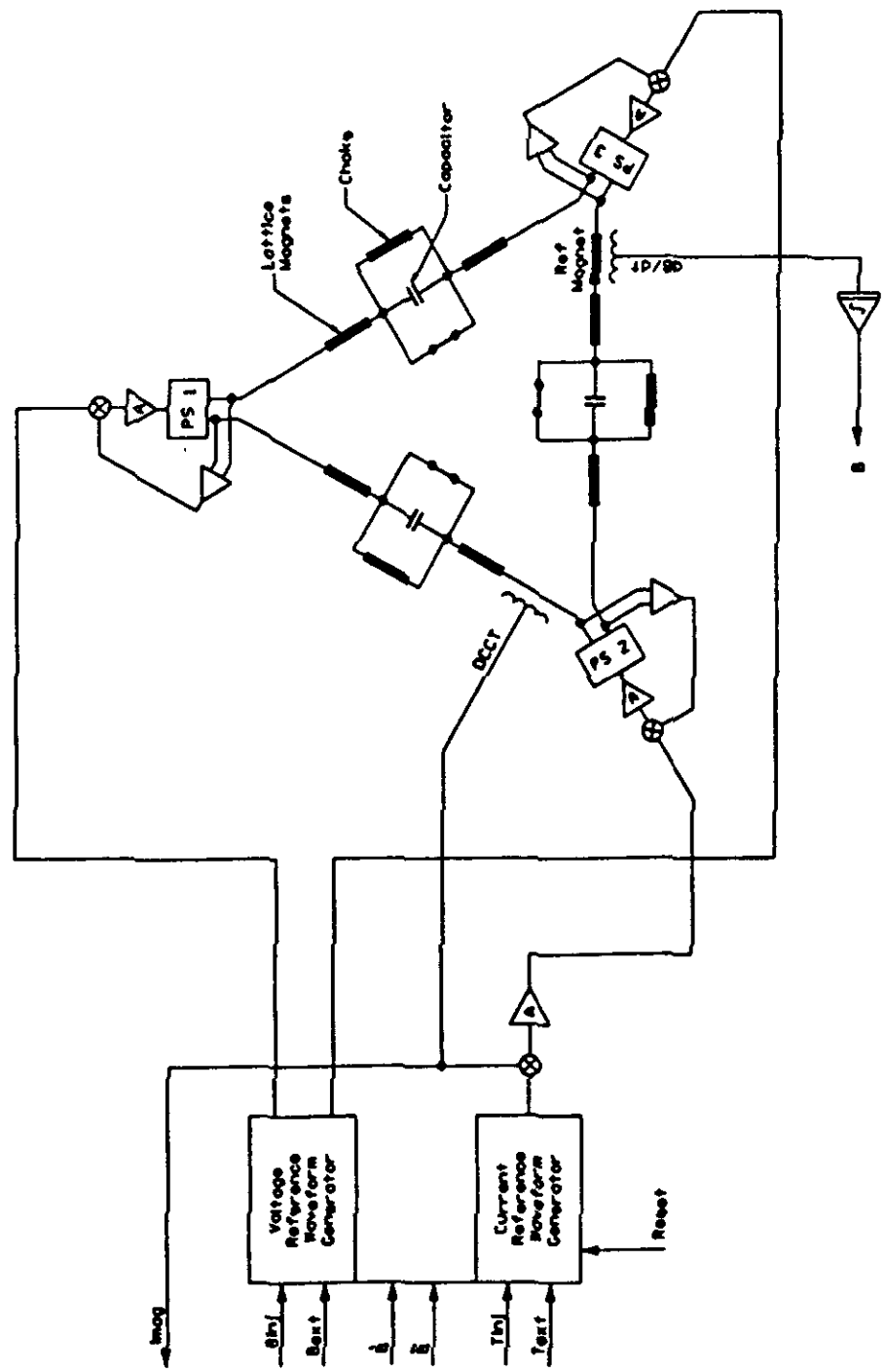


Fig.III.2 Magnet Current Waveform
1 Hz Linear Ramp Mode



LEB Ring Magnet Power System Linear Ramp Mode

Figure III.1

Main functions of the current loop are to regulate the magnet current following the reference waveform provided by the central computer, to reject d-c voltage perturbations and to reject d-c current perturbations due to changes in the load resistance.

III.2. Gain Loop Requirements

In linear ramp operation mode, knife switches in figure III.1. are closed ant the equivalent load seen by a single power supply under symmetric operation can be represented by the simplified circuit of figure III.3.

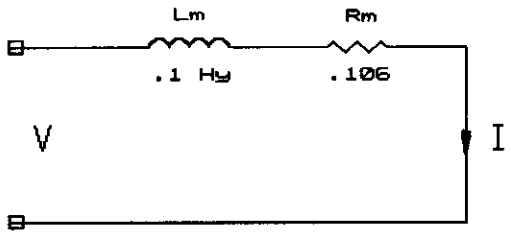


Fig. III.3. Load seen by a single power supply

The total magnet inductance seen by each power supply is L_m = .1 Hy while the resistance change with frequency, taking a value of $R_{m(dc)}$ = .106 Ω for d-c and $R_{m(ac)}$ = .132 Ω for a-c operation.

The mathematical expression of the load admittance in Laplace domain is given by

$$L(s) = \frac{\Delta I}{\Delta V} = \frac{1/R_{m(dc)}}{1 + s L_m/R_{m(dc)}} = \frac{9.43}{1 + s\,0.94} \qquad (5)$$

The load admittance presents a dominant pole at a frequency of 0.17 Hz. For frequencies higher than this value the load admittance is highly dominated by the load inductance value being almost independent of the resistance value. Thus, the change with frequency of the magnet resistance has not a significant effect on the load admittance. From expression 5, the load rejection to remainder voltage perturbations at the filter output can be readily determined.

For d-c frequency, voltage and current are just related by the d-c magnet resistance.

$$V_{dc} = I_{dc}\, R_{m(dc)} \qquad (6)$$

The regulation current requirement is 100 ppm relative to the d-c actual current flowing through the magnets. Therefore, the magnetic load only attenuate a-c voltage perturbations and this attenuation is given by

$$\frac{\Delta I/I}{\Delta V/V} = \frac{1}{1 + sL_m/R_{m(dc)}} = \frac{1}{1 + s0.94} \tag{7}$$

D-c current error as well as d-c voltage and current perturbations have to be reduced by increasing the open-loop d-c gain of the current loop. The d-c error between the reference current I_{ref} and the measured magnet current I_{mag} is

$$\frac{\Delta I_{dc}}{I_{dc}} = \frac{I_{ref} - I_{mag}}{I_{mag}} = \frac{1}{G_{dc}} \tag{8}$$

where G_{dc} represents the total open-loop d-c gain of the current regulation loop.

The current requirement of 100 ppm, is not on the absolute accuracy but on the current repeatability. If the maximum relative variation of the d-c gain loop has a value of 10% and if the d-c error variation has to be within 10 ppm, the d-c loop gain has to be at least 80 dB.

Table III.1 shows that the total magnet current deviation requirement can be fulfilled by using a current regulation loop with 80 dB d-c gain. A large amount of attenuation to a-c voltage perturbations is provided by the output filter and voltage regulation loop. The remain required attenuation has to be provided by the load characteristics or by the current regulation loop. Voltage perturbations at the filter output are usually proportional to the d-c output voltage having the same relative value at maximum or minimum load current. The voltage ripple at 720 Hz, generated by the power converter, is an exception having its maximum value when the d-c output voltage is minimum.

Table III.1

	ΔV/V or ΔI/I		Load Attenuation	Current Loop Attenuation	Current Deviation	
	Max.Cur.	Min.Cur.			Extrac.	Injec.
Voltage Perturbations						
d-c	0.1%	0.1%	----	80dB	<1ppm	<1ppm
60Hz	0.2%	0.2%	51dB	----	6ppm	6ppm
120Hz	0.2%	0.2%	57dB	----	3ppm	3ppm
360Hz	0.2%	0.2%	67dB	----	1ppm	1ppm
720Hz	0.1%	1.5%	73dB	----	<1ppm	4ppm
Load Changes	±5%	±5%	----	80dB	10ppm	10ppm
DCCT Errors	2ppm	20ppm	----	----	2ppm	20ppm
d-c Offset	2ppm	20ppm	----	----	2ppm	20ppm
d-c current error	ΔG/G=10%		----	80dB	10ppm	10ppm
Total PS Output Current Deviation					<100ppm	<100ppm

III.3. Current Loop Design

The current loop has to have enough d-c gain (80 dB) for satisfying tolerance requirements and a bandwidth frequency response large enough to follow the reference current waveform with small error.

The schematic diagram of the current loop is shown in figure III.3 where, L(s) represents the magnetic load, T(s) the voltage regulation loop, Fi(s) the output passive filter and $I_c(s)$ the cascade current compensator. In accordance with table III.1 Vp represents remainder voltage perturbations at the filter output and Ip magnet current perturbations.

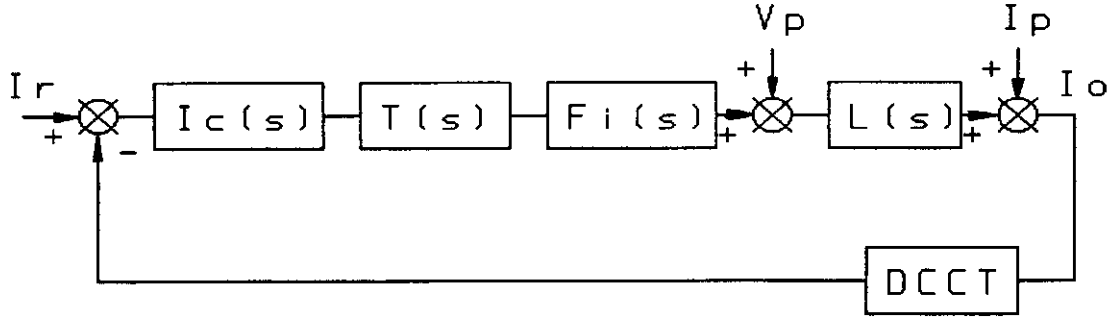


Figure III.3 Linear Ramp Mode
Schematic diagram of the current loop

For current compensator design purposes, the output passive filter can be roughly modelled by a second order pole at 100 Hz and the closed loop voltage by a single pole at 140Hz.

$$F_i(s) \approx \frac{1}{1 + 2*\xi(\frac{s}{\omega_n}) + (\frac{s}{\omega_n})^2} \qquad (9)$$

where ξ=0.5 and ω_n=630 corresponding to a frequency of 100 Hz.

$$T(s) \approx \frac{1}{1 + \frac{s}{900}} \qquad (10)$$

From Spice simulations (appendix B) it seems that a second order pole is required to model the voltage loop. This is so because in Spice simulations the power converter's delay has just be modelled with a single pole. If another delay model would have been used, as for instance a first order Pade's approximation, the results

would perhaps be different. In Tutsim simulations (appendix A) the power converter delay is well modelled and high frequencies' attenuation of the feedback voltage regulator is only 20dB/dec suggesting the use of a first order model (equation 10).

The cascade current loop compensator is designed for having a phase margin of at least 45° at the highest possible frequency for following the reference current waveform with minimum error. A lag compensator structure is selected in order to fulfill simultaneously stability conditions and d-c open loop gain.

Using the equations modelling the voltage regulation loop (eq. 10), the output filter (eq. 9), and the load (eq. 5), and taking into account gain and phase margin requirements, the current compensator can be designed. Its transfer function is given by

$$I_c(s) = 1070 \frac{(1 + s\ 0.94)}{(1 + s\ 58.5)} \qquad (11)$$

The d-c gain is high enough to satisfy the stationary state error specification, the compensator's zero cancels the pole introduced by the load, and the position of the compensator's pole has been determined by stability conditions.

The compensator design has been verified by computer simulations. It have been simulated the magnet load, the reduced order transfer functions representing the output filter and voltage regulation loop (equations 9-10), and the cascade compensator. The obtained open loop frequency responses of the current regulation loop are shown in figure III.4.

It can be seen in this figure that both stability margins are positive. A phase margin of Φ_m=60° is obtained at a phase-margin frequency of f_ϕ=30Hz while, gain margin has a value of G_m=9dB at a gain-margin frequency of f_c=80Hz.

The feedback current loop has been also simulated in a more realistic way by using Spice program. The Spice simulation of the whole voltage loop (appendix B) has been included inside of the current loop; output filter and load have been simulated by their L-C-R components and operational amplifiers have been used to implement the cascade compensator.

Amplitude and phase frequency responses of the current loop obtained with Spice simulations are shown in figure III.5. The effect of passband filters at 60 and 120Hz of the voltage cascade compensator are visible. The new bandwidth, phase margin and phase-margin frequency are practically the same as obtained with the previous figure. Nevertheless, gain margin's value is smaller presenting the feedback loop a tendency to oscillate to a frequency to about 80 Hz. This problem can be easily solved by reducing the phase-margin frequency but, the tracking error during ramp periods will increase.

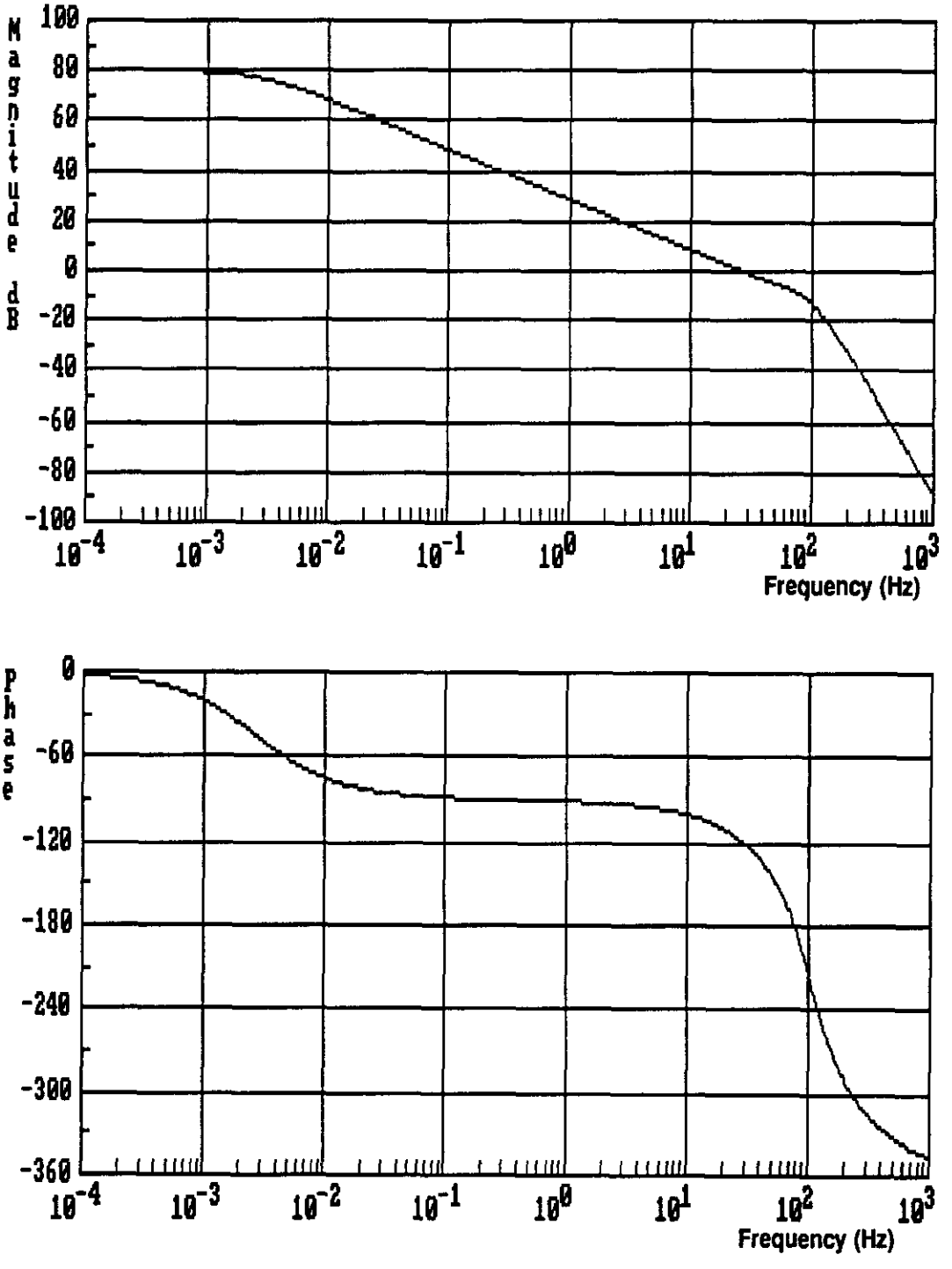


Fig. III.4. Open loop frequency response of the Current Loop Output filter and voltage loop simulated with reduced order transfer functions
a) *Gain/frequency response* b) *Phase/frequency response*

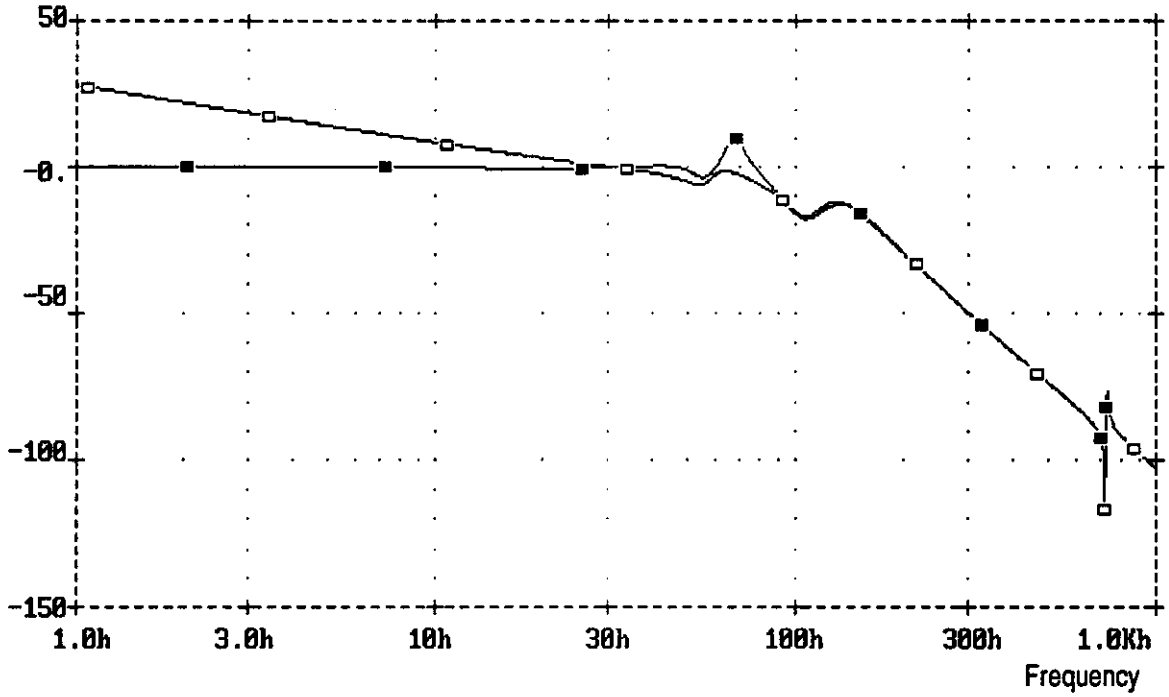


Figure III.5. a)
Gain/frequency response of the Current Loop
□ Open Loop, ■ Closed Loop

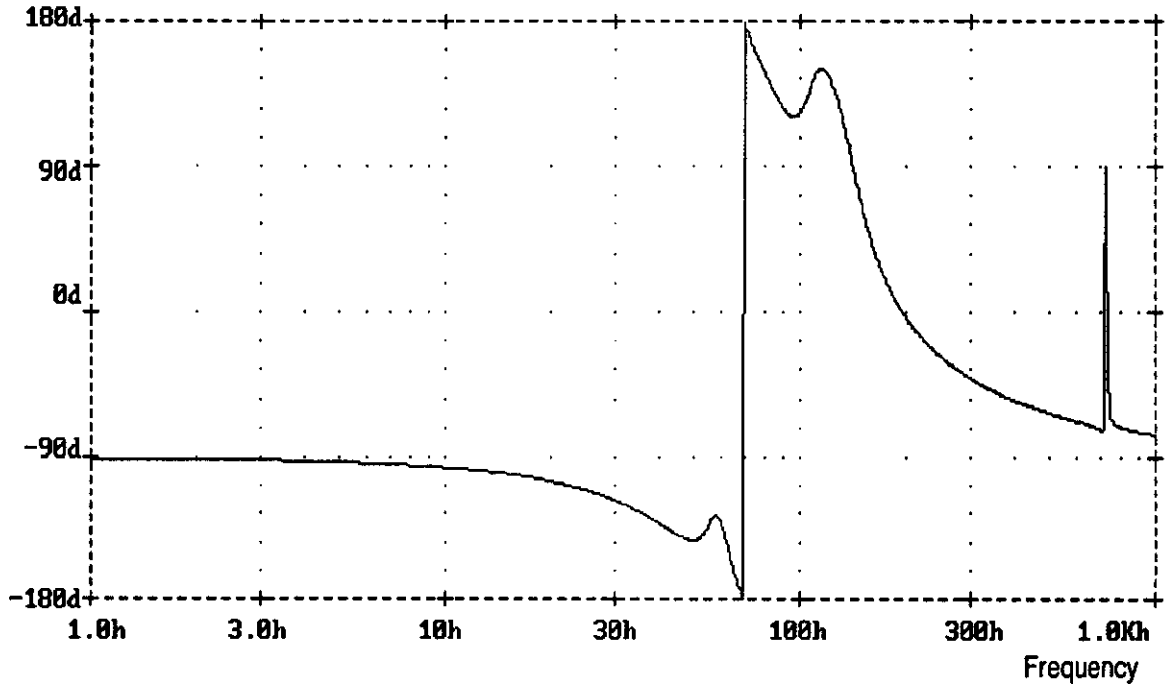


Figure III.5. b)
Open Loop Phase/frequency response of the Current Loop

III.4. Tracking Error

From equations 5-11 and figures III.4 or III.5 it can be seen that in the frequency band of interest and for tracking error analysis, the total open loop transfer function can be just approximated by equation 12 which represents a type 1 system.

$$G(s) \approx \frac{170}{s} \tag{12}$$

Thus, the output current presents an approximate constant error under ramp periods given by [4]

$$e(t)_{ss} \approx \frac{dI/dt}{170} \approx \frac{9650}{170} \approx 60\,Amps \tag{13}$$

where dI/dt represents the maximum current's first derivative taking a value of 9.5KA for a typical 1Hz cycle waveform.

The dynamic behavior simulation of the feedback regulation loop is presented in figure III.6 where it is shown a typical 1 Hz current reference waveform and the output current flowing through the magnets.

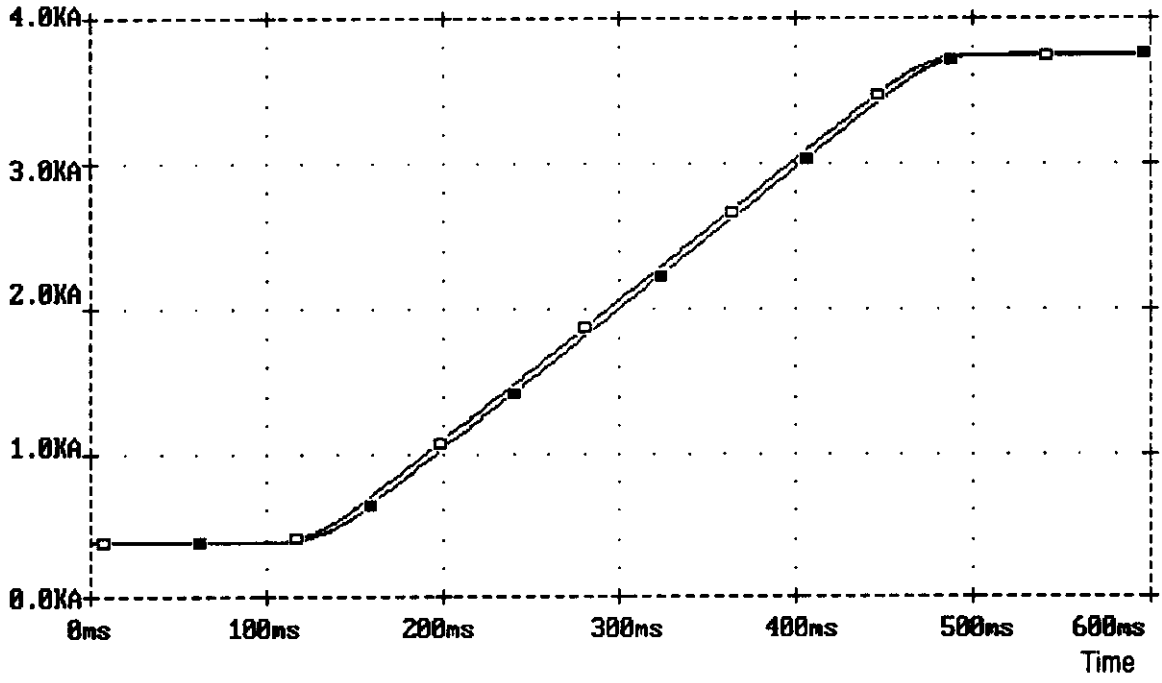


Figure III.6
Current waveforms □ reference current, ■ magnet current

Expansions of figure III.6, showing the current transient behavior at the ramp beginning and when the top is reached are shown in figure III.6. a) and b) respectively. The tracking error obtained from this figure agree with the value predicted by equation 13.

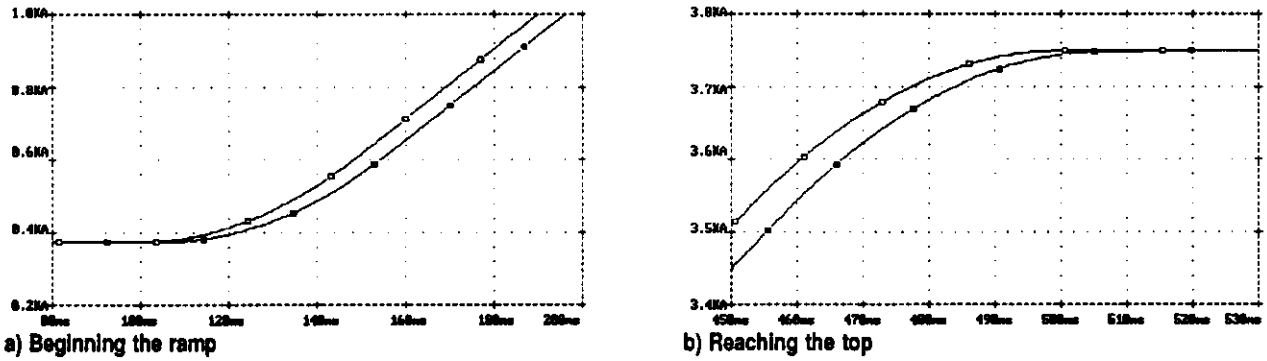


Figure III.7
Current waveform expansions □ reference current, ■ magnet current

III.5. Rejection to perturbations

The rejection characteristics of the feedback system have been analyzed and the simulation results are shown in figures III.8 and III.9.

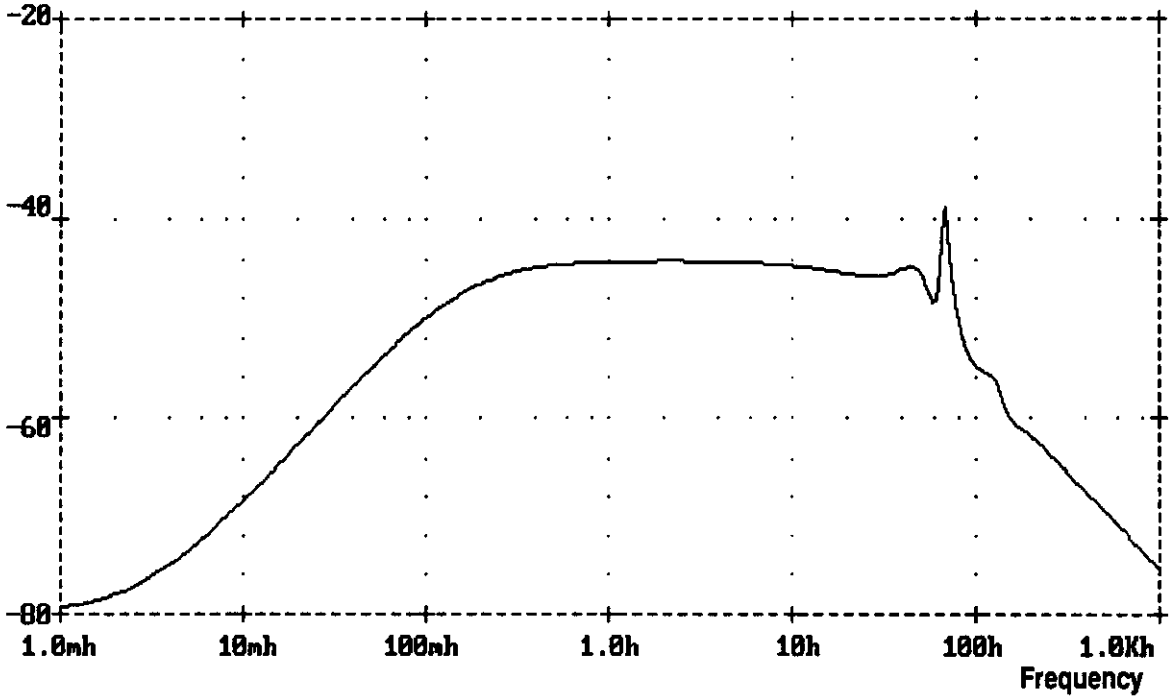


Fig.III.8. Rejection characteristics of the current loop to voltage perturbations injected at the filter output.

In figure III.8 it is investigated the current loop attenuation to remainder voltage perturbations after taking into account voltage loop rejection and filter attenuation. Remainder voltage perturbations are injected at the filter output (Vp in figure III.3). It is seen in the figure that the requirements of table III.1 are fulfilled.

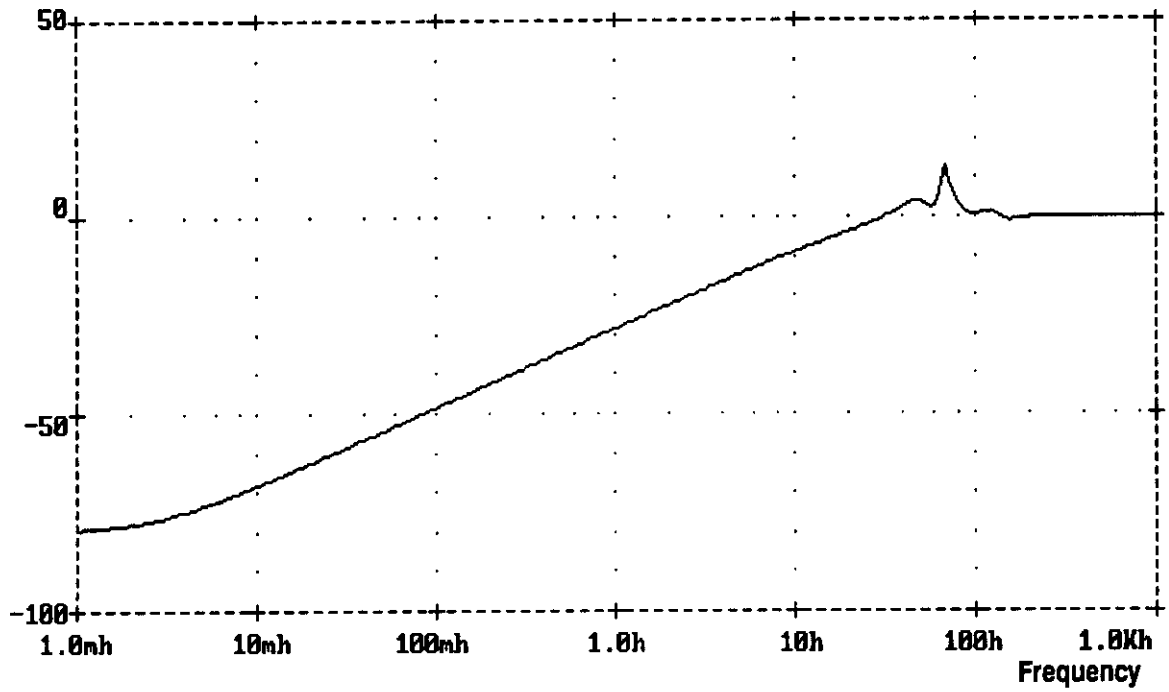


Fig.III.9. Rejection characteristics of the current regulation loop to load current perturbations.

The rejection characteristics to load current perturbations are presented in figure III.9 showing an attenuation of 60dB for extremely low perturbation's frequencies. In this way, all the requirements of table III.1 are fulfilled and the current regulator's design for linear ramp operation mode is completed.

III.6. Stability improvement

The gain margin obtained from Figure III.5 is too small and the closed loop frequency response (figure III.5.a) has a gain higher than one at about 80Hz showing a system's tendency to oscillate at this frequency. This problem can be easily solved by a slightly modification of the compensator design. Its new transfer function is given by

$$I_c(s) = 1070 \frac{(1 + s\ 0.94)}{(1 + s\ 110)} \qquad (14)$$

The frequency response of the current loop obtained by using this cascade compensator's transfer function is shown in figure III.10.

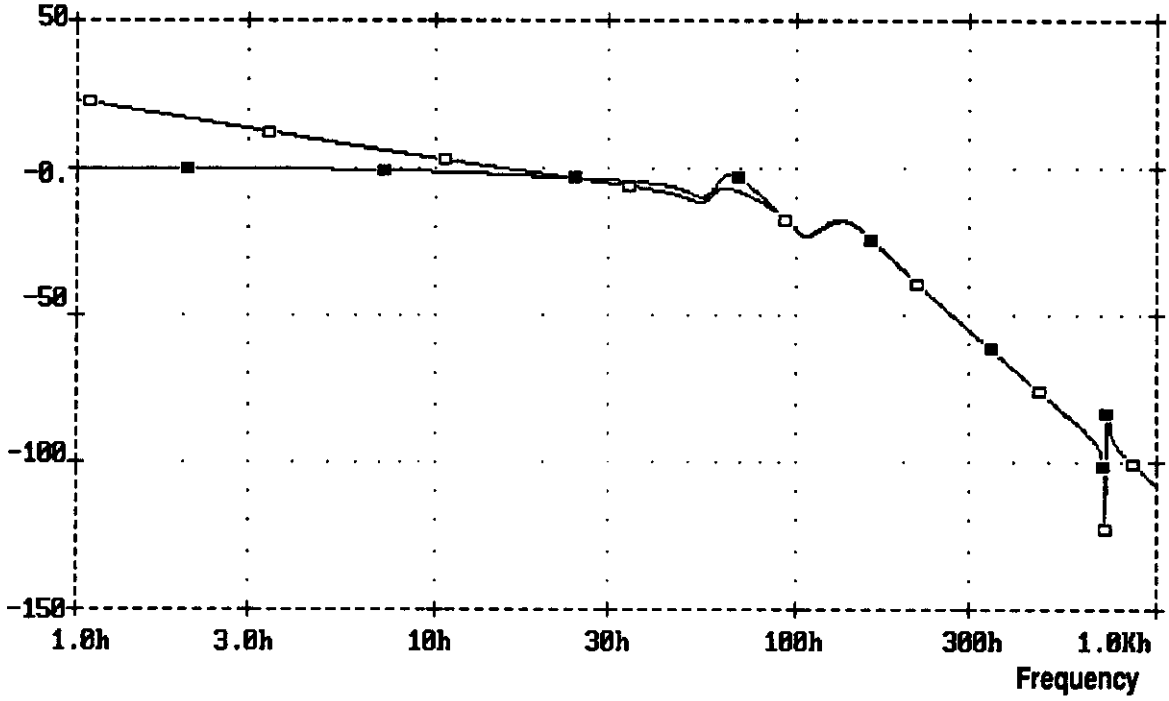


Figure III.10
Gain/frequency response of the Current Loop
□ Open Loop, ■ Closed Loop

Comparing figures III.10 and III.5.a) the improvement in stability becomes apparently. But, the bandwidth has been reduced and a higher tracking error has to be expected. In fact, equation 12 is transformed into 15 and, replacing the new ramp error coefficient in equation 13, an almost double tracking error is obtained.

$$G(s) \approx \frac{90}{s} \qquad (15)$$

The dynamic behavior of the feedback regulation loop is shown in figure III.11. Comparing this figure with figure III.6 it can be clearly seen that the tracking error during the linear ramp period has been increased.

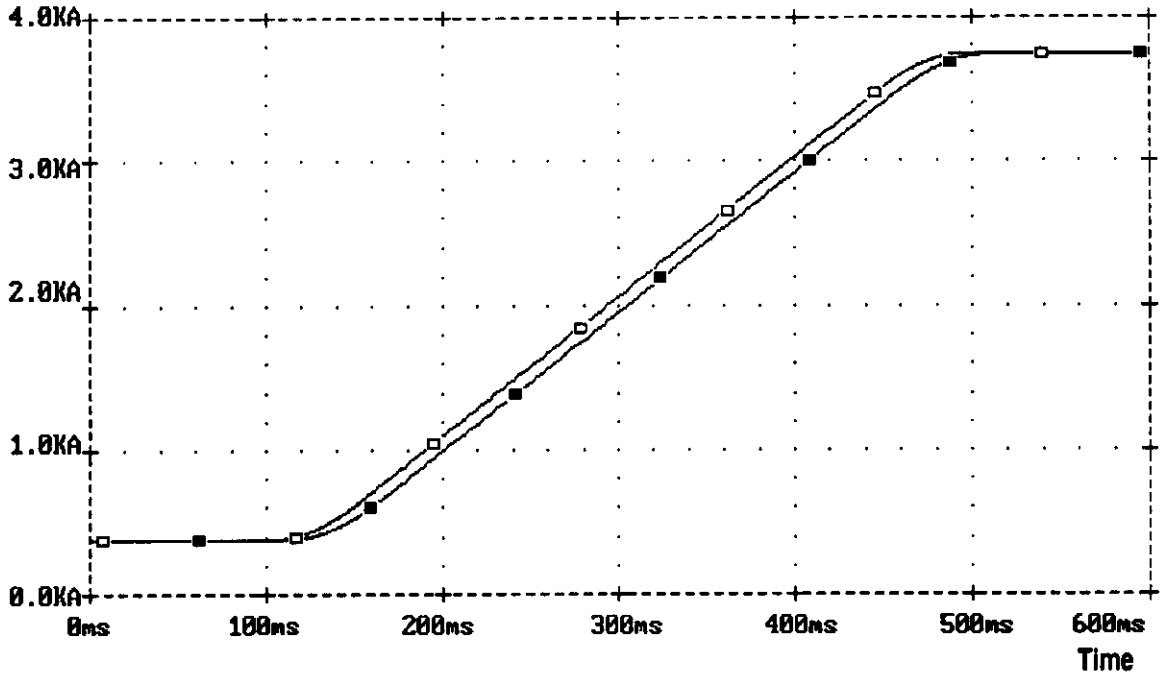


Figure III.11
Current waveforms □ reference current, ■ magnet current

The rejection characteristics of the feedback system are shown in figures III.12 and III.13. This figures are different than those obtained in the previous case presenting a lower pick at 80Hz. Nevertheless, all the requirements of table III.1. are fully satisfied.

The current regulation loop of the LEB ring magnet power supply, under linear ramp mode, has been simulated using the program Spice. An schematic diagram of the Spice simulation and the Spice program listing can be found in appendix C.

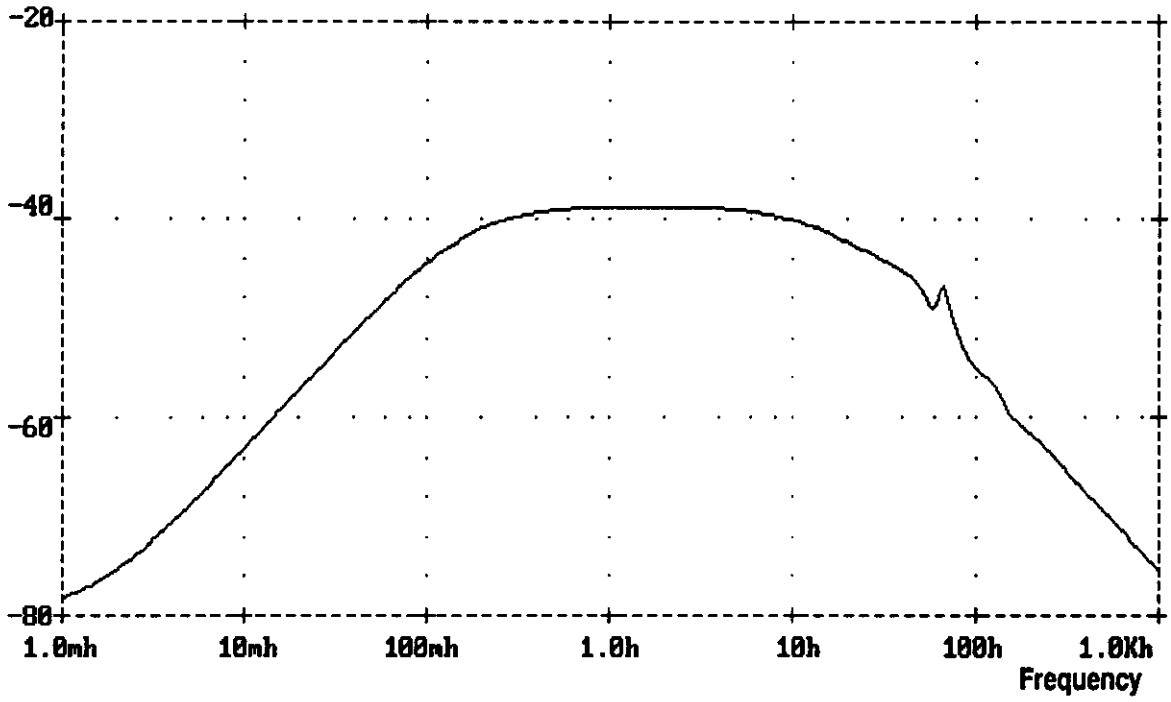


Fig.III.12. Rejection characteristics of the current loop to voltage perturbations injected at the filter output.

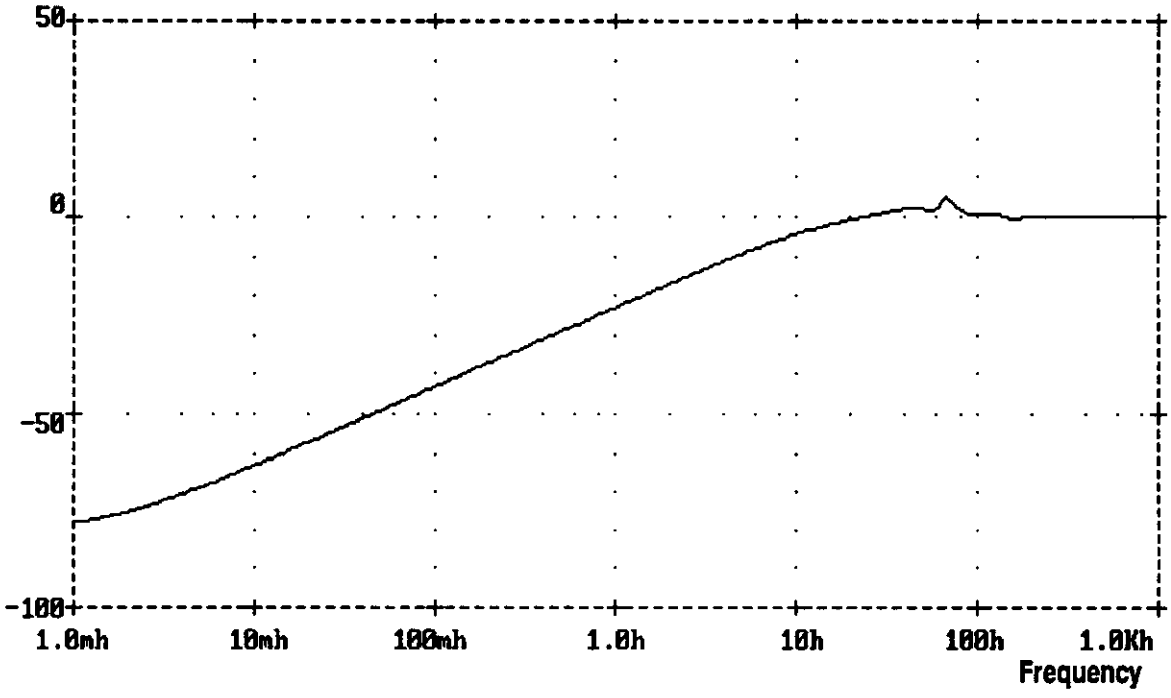


Fig.III.13. Rejection characteristics of the current regulation loop to load current perturbations.

IV. CURRENT LOOP DESIGN, SINE WAVE MODE

IV.1. Introduction

When the LEB is operated under 10 Hz mode, a biased sine wave current is required to flow through the magnets. Figure IV.1 shows a typical required magnet current waveform.

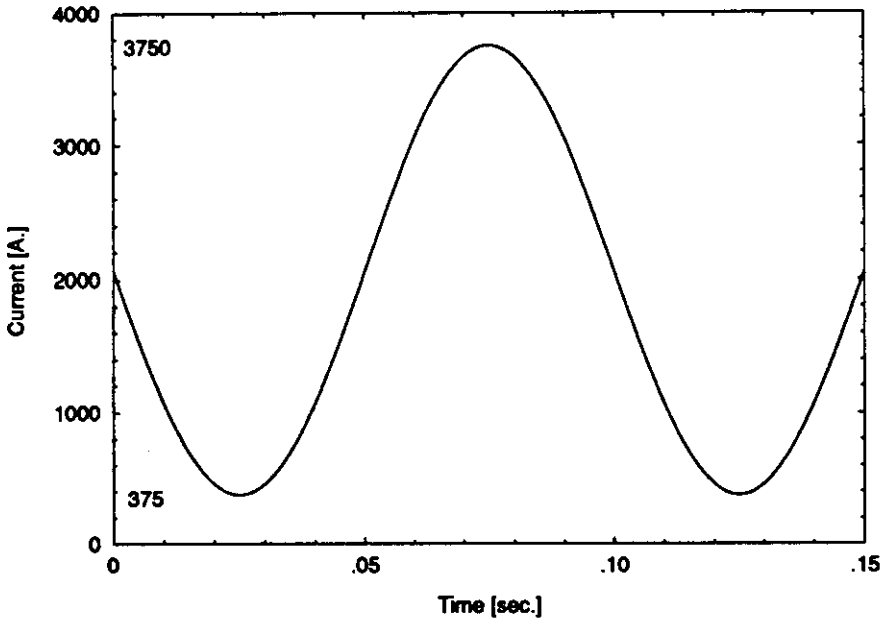
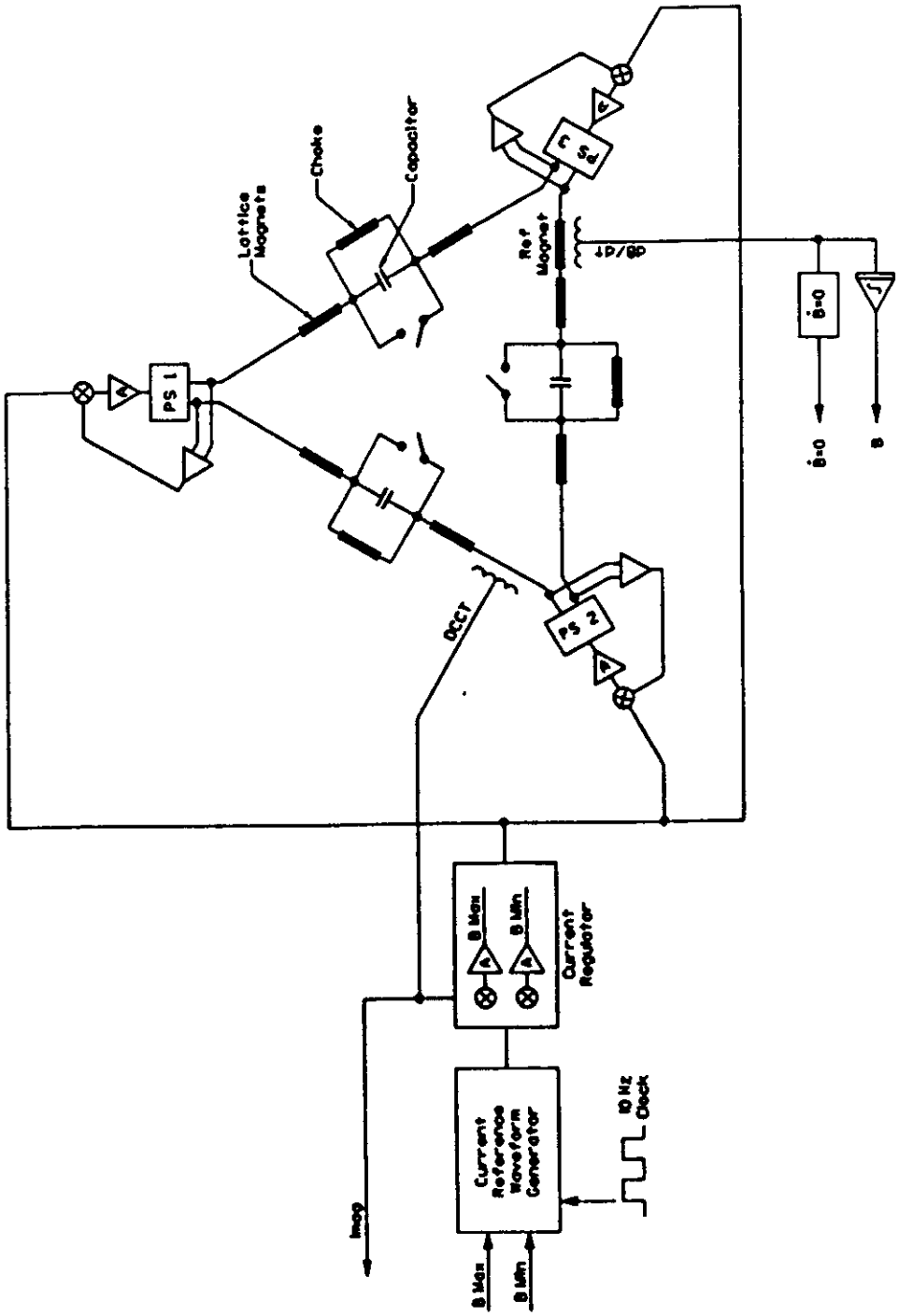


Figure IV.1 Magnet Current Waveform
10 Hz Biased Sine Wave mode

To avoid drawing a large reactive power from the a-c source it is necessary to use a circuit which is resonant at 10 Hz and in addition provides a path for the d-c bias current [2], [3]. These requirements are satisfied by the distributed resonant circuit shown in figure IV.2, where the knife switches are open. The three power supplies have an output filter and voltage loop but, considering that they are connected in series circuit, the current of only one of them is regulated by a closed loop.



LEB Ring Magnet
Power System
Biased Sine Wave Mode

Figure IV.2
LEB Ring Magnet Power System
Biased Sine Wave Mode

IV.2. Regulation Requirements

The regulation requirements of the current are different during different sections of a cycle: Injection, Acceleration, Extraction and Invert. The most restrictive current regulation requirements occurs under constant load, either during the injection or extraction period. In the LEB the total magnet current deviation during both injection and extraction periods has to be less than 100 ppm of the actual current [3].

Total Deviation $\delta I/I$, Max. = 100ppm

Main functions of the current loop are to regulate the minimum and maximum magnet current as close as possible to the reference values provided by the central computer, to reject d-c voltage perturbations and to reject d-c current perturbations due to changes in resonant circuits or load parameters.

Table IV.1 shows that the total magnet current deviation requirement can be fulfilled by using current regulation loops with 80dB d-c gain. A large amount of attenuation to a-c voltage perturbations is provided by the output filter and voltage regulation loop. The remain required attenuation has to be provided by the load characteristics or by the current regulation loop. Voltage perturbations at the filter output are usually proportional to the d-c output voltage having the same relative value at maximum or minimum load current. The voltage ripple at 720 Hz, generated by the power converter, is an exception having its maximum value when the d-c output voltage is minimum.

The DC Current Transducer is the same for linear ramp and biased sine wave modes and has been specified in section III.3.

Table IV.1

	ΔV/V or ΔI/I		Load Attenuation	Current Loop Attenuation	Current Deviation	
	Max.Cur.	Min.Cur.			Extrac.	Injec.
Voltage Perturbations						
d-c	0.1%	0.1%	----	80dB	<1ppm	<1ppm
60Hz	0.2%	0.2%	43dB	----	14ppm	14ppm
120Hz	0.2%	0.2%	49dB	----	7ppm	7ppm
360Hz	0.2%	0.2%	59dB	----	2ppm	2ppm
720Hz	0.1%	1.5%	65dB	----	<1ppm	9ppm
Load Changes	±5%	±5%	----	80dB	10ppm	10ppm
DCCT Errors	2ppm	20ppm	----	----	2ppm	20ppm
d-c Offset	2ppm	20ppm	----	----	2ppm	20ppm
d-c current error	ΔG/G=10%		----	80dB	10ppm	10ppm
Total PS Output Current Deviation					<100ppm	<100ppm

IV.3 Current Loop Design

In 10 Hz biased sine wave mode, the central computer provides the maximum and minimum values of the 10 Hz sinusoidal current waveform. The total deviation on the maximum and minimum values of the magnet current, has to be less than 100 ppm of the actual current. A current regulation system with a high open-loop gain at 10 Hz is necessary for satisfying this regulation requirement. A conventional regulator, as used for the linear ramp, is not suitable for this application. In fact, the requirements of high open-loop gain at 10 Hz and adequate closed-loop stability can not be simultaneously fulfilled by using conventional techniques.

The regulation problem has been solved by applying frequency conversion techniques. The designed current regulator presents an equivalent open-loop high gain for 10 Hz sine wave while the closed-loop bandwidth is limited to less than 1 Hz.

The biased sine wave magnet current (fig. IV.1.) can be express as

$$I(t) = I_{dc} - I_{ac}\sin(\omega_p t) \qquad (16)$$

where $\omega_p=2\pi$ 10 Hz and I_{dc} and I_{ac} represent d-c and a-c current components respectively.

The load behavior is different for d-c and a-c current components. In order to obtain similar transient responses to d-c and a-c current changes, two independent compensated loops are used to regulate the 10 Hz a-c current amplitude and the d-c current value.

The schematic diagram of the current loop is shown in figure IV.3, where, L(s) represents the magnetic load and resonant cells, T(s) the voltage regulation loop, F(s) the output filter and G(s), $C_{ac}(s)$ and $C_{dc}(s)$ cascade current compensators.

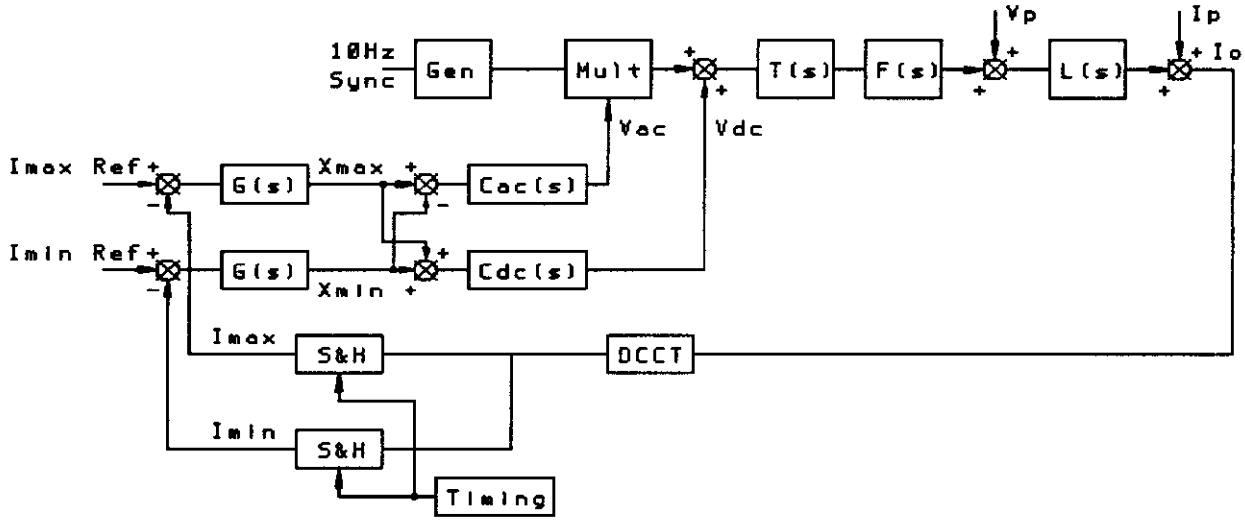


Figure IV.3. Block diagram of the current loop
10 Hz. Biased Sine Wave mode

The central computer provides a 10 Hz synchronization signal and the maximum and minimum values of the 10 Hz sinusoidal current waveform ($I_{max\ ref}$ and $I_{min\ ref}$). In the regulation system, shown in figure IV.3, maximum and minimum values of the output current (I_{max} and I_{min}) are measured and compared with the reference values.

The maximum and minimum output currents measurements are performed by using a 10 Hz timing circuit and two sample and hold circuits. Maximum and minimum errors, processed by the G(s) controller, are added and subtracted for driving the d-c controller and the a-c controller respectively.

The 10 Hz sinusoidal generator is synchronized with the signal provided by the central computer. A multiplier excited by the a-c controller regulates the 10 Hz a-c current amplitude while the d-c component is regulated by adding the d-c controller's output to the 10 Hz sine wave. Both current loops are stabilized by using cascade compensators designed in order to fulfill current requirements and provide adequate stability and transient behavior.

IV.4. Load Analysis

The equivalent load seen by a single power supply under symmetric operation is represented in figure IV.4. Where the equivalent ac parameters of the magnets and resonant cells seen by a single power supply are [2]: L_m=100mHy, R_m=132mΩ, L_r=160mHy, R_l=240mΩ, C_r=4.125mF and, R_c=12mΩ. The resistance of the magnets and resonant chokes depends on the frequency and under dc operation, they have the following values: $R_{m(dc)}$=106mΩ, and $R_{l(dc)}$=160mΩ.

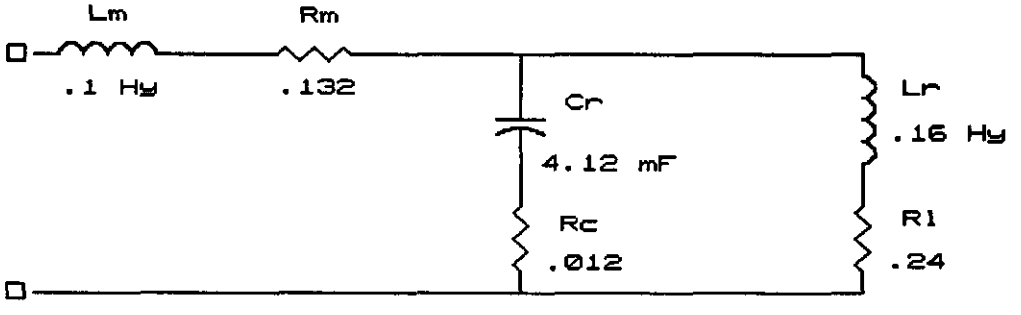


Figure IV.4
Load seen by a single power supply

The mathematical expression of the load admittance in Laplace domain is given by

$$Y_l(s) = \frac{2.69\ (1 + s\,1.04\ 10^{-3} + s^2\,6.6\ 10^{-4})}{1 + s\,0.7 + s^2\,5.35\ 10^{-4} + s^3\,1.77\ 10^{-4}} \qquad (17)$$

For d-c frequency, voltage and current are related by the total d-c resistance.

$$V_{dc} = I_{dc}\ (R_{m(dc)} + R_{l(dc)}) \qquad (18)$$

Taking into account that voltage perturbations (Vp) are relative to the d-c output voltage (Fig. IV.3 and Table IV.1) the load does not attenuate d-c voltage or current perturbations. Considering the dc load resistive values, the expression of the load attenuation to voltage perturbations is given by

$$\frac{\Delta i/I}{\Delta v/V} = \frac{0.72\ (1 + s\,1.04\ 10^{-3} + s^2\,6.6\ 10^{-4})}{1 + s\,0.7 + s^2\,5.35\ 10^{-4} + s^3\,1.77\ 10^{-4}} \qquad (19)$$

The load attenuation to remain voltage perturbations at the filter output (Vp) is shown, in the frequency domain, in figure IV.5. In the high frequency band, the resonant chokes are shortcircuited by the resonant capacitors and the load attenuation can be approximated by

$$\left.\frac{\Delta i/I}{\Delta v/V}\right|_{for\ f>10\,Hz} \simeq \frac{R_{m(dc)} + R_{l(dc)}}{s\ L_m} \simeq \frac{2.66}{s} \qquad (20)$$

Therefore, the attenuation obtained in the high frequency band is 8 dB less for 10 Hz sine wave mode than for linear ramp mode (equation 7).

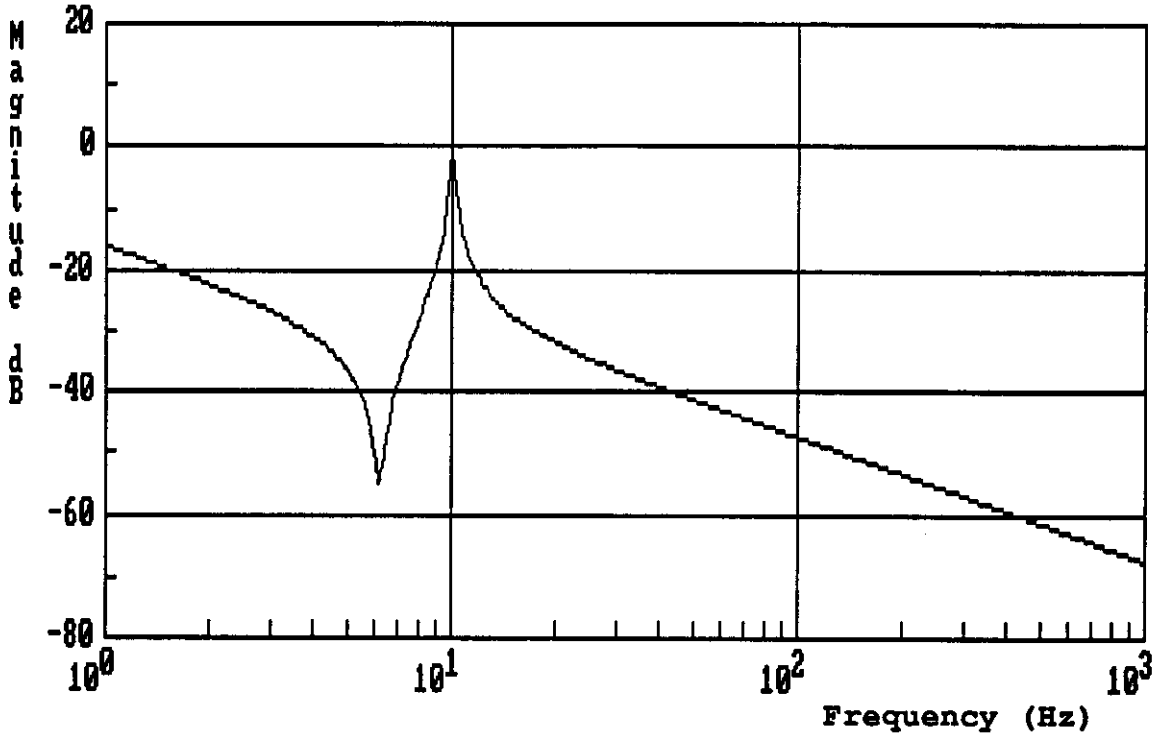


Figure IV.5. Load Rejection characteristics to voltage perturbations injected at the filter output.

D-c current error as well as d-c voltage and current perturbations have to be reduced by increasing the open-loop d-c gain of the current loop. The d-c error between the reference current I_{ref} and the measured magnet current I_{mag} is

$$\frac{\Delta I_{dc}}{I_{dc}} = \frac{I_{ref} - I_{mag}}{I_{mag}} = \frac{1}{G_{dc}} \qquad (21)$$

where G_{dc} represents the total open-loop d-c gain of the current regulation loop.

The current requirement of 100 ppm, is not on the absolute accuracy but on the current repeatability. If the maximum relative variation of the d-c gain loop has a value of 10% and if the d-c error variation has to be within 10 ppm, the d-c loop gain has to be at least 80 dB.

IV.5. Sampler and Hold

Two sampler-and-hold circuits are used for measuring the maximum and minimum value of the 10 Hz sine wave magnet current. The transfer function associated to these 10 Hz frequency sampler and zero-order hold is given by [4]

$$G_{zoh}(s) = \frac{1 - e^{-sT}}{sT} = e^{-sT/2} \frac{(e^{sT/2} - e^{-sT/2})}{sT} \qquad (22)$$

where T=0.1 sec.

For low frequencies, equation 22 can be approximated by

$$G_{zoh}(s) \approx e^{-sT/2} = e^{-s\,0.05} \qquad (23)$$

Thus, in the low frequency band, the sampler-and-hold circuit can be modelled by a linear phase. This phase, taking a value of -90° at 5Hz affects the system stability and limits the current loop bandwidth.

IV.6. d-c Load Behavior

The mean value of the current output is calculated by adding the measurements of the maximum and minimum 10 Hz output current. These measurements are performed by using a 10 Hz timing circuit and two sampler and holds. In the low frequency band, this measurement system can be modelled by its average delay of 50msec (equation 23).

The load admittance (equation 17) can be also written as

$$Y_l(s) = \frac{2\,69 \left(1 + \frac{s}{Q_z \omega_z} + (\frac{s}{\omega_z})^2\right)}{(1 + s\tau_l)\left(1 + \frac{s}{Q_p \omega_p} + (\frac{s}{\omega_p})^2\right)} \qquad (24)$$

where τ_l=0.7, Q_z=25, ω_z=2π 6.2Hz, Q_p=40 and ω_p=2π 10Hz.

For designing the mean-value current controller, the d-c resistance of magnets and chokes has to be considered. The correction due to resistance changes with frequency can be performed by multiplying equation 24 by the following factor

$$A(s) = \left[\frac{R_{m(ac)} + R_{l(ac)}}{R_{m(dc)} + R_{l(dc)}}\right] \left[\frac{1 + s\frac{L_m + L}{R_{m(ac)} + R_{l(ac)}}}{1 + s\frac{L_m + L}{R_{m(dc)} + R_{l(dc)}}}\right] = 1.4 \left[\frac{1 + s\,0.7}{1 + s\,0.98}\right] \qquad (25)$$

Notice that the above factor takes the value of 1 for frequencies higher than 0.23 Hz. Thus for the analysis at the 10 Hz frequency band, equations 17 and 24 can be used without any correction.

For designing the d-c current loop, the load admittance can be approximated by

$$Y_i(s) \simeq \frac{3.76}{1 + 0.98\,s} \tag{26}$$

Considering the current-loop bandwidth limitation, the closed loop voltage and the output passive filter can be roughly modelled by a unitary gain. Therefore, the transfer function between the d-c controller's output (Vdc) and the mean value of the magnet current can be approximated by

$$T_{dc}(s) \simeq \frac{7.5}{1 + 0.98\,s}\, e^{-s0.05} \tag{27}$$

where the sample-and-hold delay (equation 23) and a gain factor of 2 due to the addition of maximum and minimum current measurements have been included.

IV.7. a-c Load Behavior

The dynamic behavior of the power supply and load is different for d-c and a-c current components. The first step to design the a-c amplitude regulation loop is to obtain a mathematical model of the system including modulation and detection processes. The block diagram of figure IV.6 will be used for this purpose. The closed loop voltage regulator and output passive filter are transparent for the low frequency band to be considered in the current regulation loop analysis. Therefore, they were not included in figure IV.6.

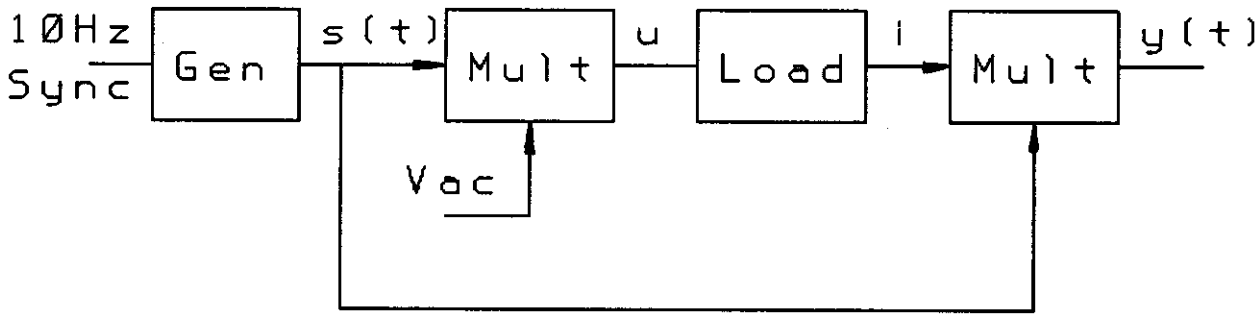


Figure IV.6. Block diagram representing the modulation and detection process

The signal demodulation has been implemented, in the above figure, with a synchronous or a linear phase detector [5]. In fact, as the carrier frequency is available, this efficient method for amplitude or phase detection can be readily implemented.

The amplitude modulation and detection are nonlinear processes that can be handled by the Laplace transform using s-plane convolution [6]. The same structure employing a multiplier excited by the 10 Hz sine wave is used in figure IV.3 for implementing both, modulation and detection processes.

Let the carrier signal s(t) be represented by

$$s(t) = \cos(\omega_p t) \tag{28}$$

where $\omega_p=2\pi$ 10Hz.

The Laplace transform of this carrier signal is given by

$$S(s) = \frac{s}{s^2 + \omega_p^2} \tag{29}$$

Let $v_{ac}(t)$ be the modulation function, with Laplace transform denoted by $V_{ac}(s)$. The transform of the product is expressed by the following s-plane convolution

$$U(s) = \frac{1}{2\pi j} \int S(\lambda)\, V_{ac}(s-\lambda)\, d\lambda = \frac{1}{2\pi j} \int \frac{\lambda}{\lambda^2 + \omega_p^2}\, V_{ac}(s-\lambda)\, d\lambda \tag{30}$$

The integral is evaluated by summing residues at poles of $S(\lambda)$, giving the result

$$U(s) = \frac{V_{ac}(s+j\omega_p) + V_{ac}(s-j\omega_p)}{2} \tag{31}$$

The transform of the output current is given by

$$I(s) = U(s)\, Y_l(s) \tag{32}$$

where $Y_l(s)$ represents the load admittance (equation 24).

Now let this modulated current-output signal be demodulated in a synchronous detector. Convolution in the s plane is used again, to obtain the transform of the product.

$$Y(s) = \frac{1}{2\pi j} \int S(\lambda)\, I(s-\lambda)\, d\lambda = \frac{1}{2\pi j} \int \frac{\lambda}{\lambda^2 + \omega_p^2}\, I(s-\lambda)\, d\lambda \tag{33}$$

This integral is readily evaluated by using residues at poles of $S(\lambda)$, giving

$$Y(s) = \frac{I(s+j\omega_p) + I(s-j\omega_p)}{2} \tag{34}$$

and using equations 13 and 14 it is

$$Y(s) = \frac{Y_l(s+j\omega_p)}{4} (V_{ac}(s+j2\omega_p) + V_{ac}(s)) + \frac{Y_l(s-j\omega_p)}{4} (V_{ac}(s-j2\omega_p) + V_{ac}(s)) \tag{35}$$

A low-pass filter is usually employed at the detector output. Thus, the open loop transfer function can be approximated by

$$T(s) = \frac{Y(s)}{V_{ac}(s)} \approx \frac{Y_l(s+j\omega_p) + Y_l(s-j\omega_p)}{4} \tag{36}$$

By replacing equation 24 in 36 the expression of the transfer function, between multiplier input and detector output, is finally obtained

$$T(s) \approx \frac{5\left((s+1.16)^2+(40.5)^2\right)\left((s+0.737)^2+(108)^2\right)}{(s+\frac{\omega_p}{2Q_p})\left((s+\frac{1}{\tau_l})^2+(\omega_p)^2\right)\left((s+\frac{\omega_p}{2Q_p})^2+(2\omega_p)^2\right)} \tag{37}$$

where τ_l=0.7, Q_p=40 and ω_p=2π 10 Hz.

The filter following the synchronous detector will normally be a low-pass filter with cutoff considerably below frequency ω_p. Therefore, as an approximation, the transfer function T(s) is

$$T(s) = \frac{Y(s)}{V_{ac}(s)} \approx \frac{1.95}{1 + s1.26} \tag{38}$$

Let the signal i(t) be a non-biased sinusoid with amplitude $\hat{I}$ and the same frequency and phase that the carrier signal s(t). From equation 33, the signal at the detector output is readily evaluated having a d-c component of amplitude $\hat{I}/2$.

A timing circuit and two sample and hold circuits are used in figure IV.3 for current measurements. The timing circuit generates sample pulses synchronized with the maximum and minimum of the magnet current. Two sample-and-hold circuits measure the maximum and minimum current respectively. Thus, this measuring system works in a similar way as a synchronous detector but has a different d-c gain. In fact, if the magnet current is a non-biased sinusoid with amplitude $\hat{I}$ and the same frequency and phase of the carrier signal s(t), the difference between maximum and minimum sample-and-hold outputs will yield a d-c component of amplitude $2\hat{I}$. Therefore, the open-loop transfer function $T_{ac}(s)$ between multiplier input and detector output, corresponding to the block diagram of figure IV.3, can be approximated by

$$T_{ac}(s) \approx \frac{7.8}{1 + 1.26s} e^{-s0.05} \tag{39}$$

where the gain of the addition circuit and the delay introduced by the sample and hold have been included (equation 23).

IV.8. Interaction between maximum and minimum current loops

The following step in the regulation design is to minimize the interaction between maximum and minimum current loops. The maximum and minimum magnet currents can be expressed as a function of the inputs of a-c and d-c controllers (Figure IV.3)

$$I_{max} = X_{max} T_c + x_{min} T_d$$
$$I_{min} = X_{max} T_d + X_{min} T_c \qquad (40)$$

where

$$T_c = \frac{C_{ac} T_{ac} + C_{dc} T_{dc}}{2}$$
$$T_d = \frac{C_{ac} T_{ac} - C_{dc} T_{dc}}{2} \qquad (41)$$

Therefore, the loop interaction can be minimized by making

$$C_{ac} T_{ac} = C_{dc} T_{dc} \qquad (42)$$

From equations 27 and 39, the above condition is readily satisfied by choosing

$$C_{dc} = 1.04 \left(\frac{1 + s\,0.98}{1 + s\,1.26} \right); \qquad C_{ac} = 1 \qquad (43)$$

IV.9. Compensator design

The last step is to design the cascade compensator G(s). A lag compensator structure has been designed in order to have a bandwidth of 0.5 Hz and fulfill simultaneously the stability conditions and the d-c open loop gain. Its transfer function is given by

$$G(s) = 1300 \frac{1 + 1.26\,s}{1 + 3200\,s} \qquad (44)$$

The d-c gain is high enough to satisfy the stationary state error specification, the compensator's zero cancels the pole introduced by the load, and the position of the compensator's pole has been determined by stability conditions and bandwidth requirements.

The resulting total open loop transfer function is the same for both loops and can be approximated by

$$G_t(s) \approx 1300 \frac{1 + 1.26\,s}{1 + 3200 s} \frac{7.8}{1 + 1.26\,s} e^{-s0.05} \approx \frac{10160}{1 + 3200 s} e^{-s0.05} \qquad (45)$$

The current regulation loop has been verified by computer simulations. The first simulation step is to analyzed the simplified transfer function design. The frequency response of the total open loop transfer function is shown in figure IV.7.

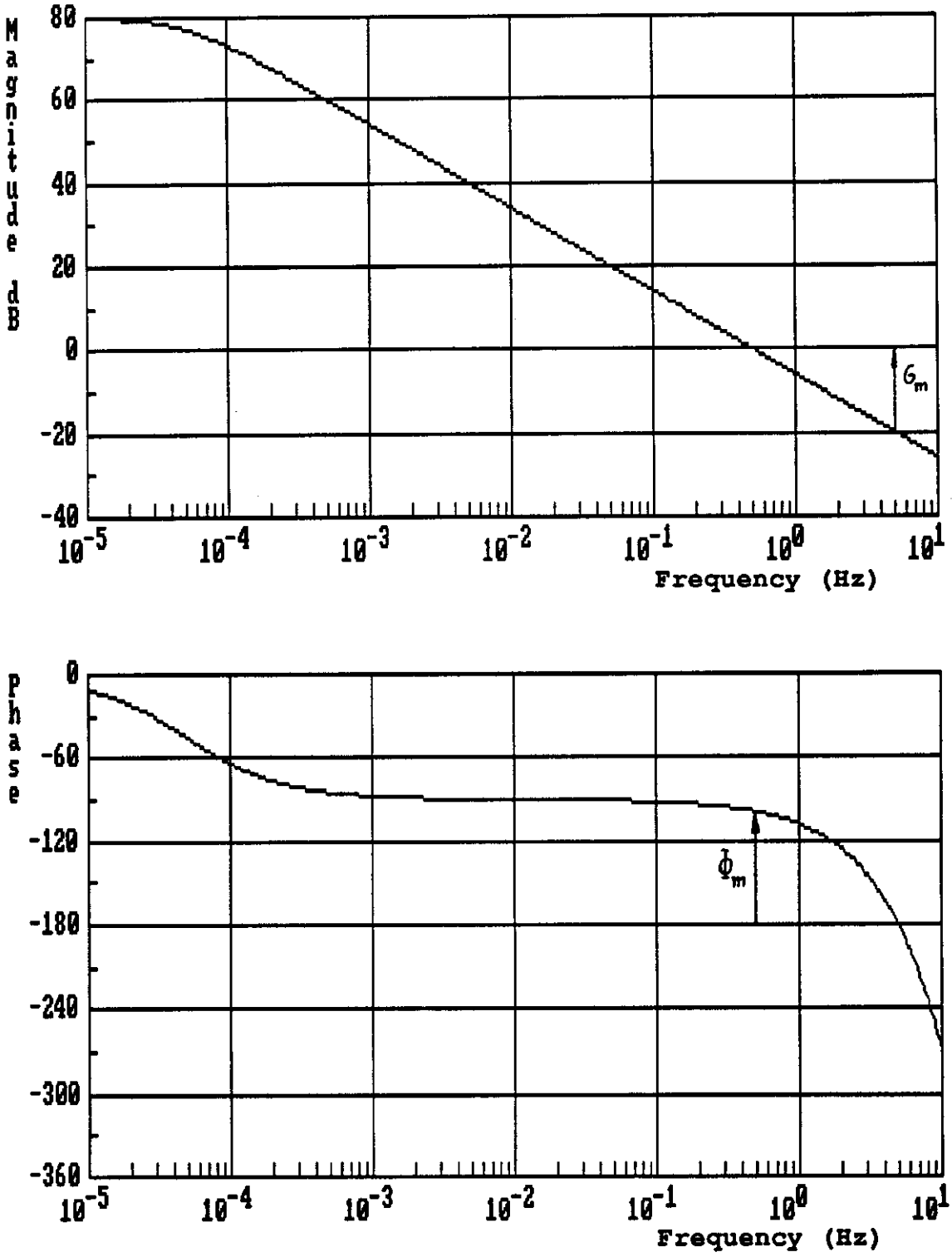


Fig. IV.7. Open-loop frequency response of the Mean-value Current Loop by using simplified transfer function analysis
a) Gain/frequency response b) Phase/frequency response

The closed loop system is stable. A phase margin of Φ_m=81° is obtained at a phase-margin frequency of f_ϕ=0.5 Hz while, gain margin has a value of G_m=20 dB at a gain-margin frequency of f_c=5 Hz.

The closed-loop frequency response of the current loop by using simplified transfer function analysis is represented in figure IV.8. Both current regulation loops will be decoupled presenting similar dynamic behavior with a bandwidth of about .5 Hz.

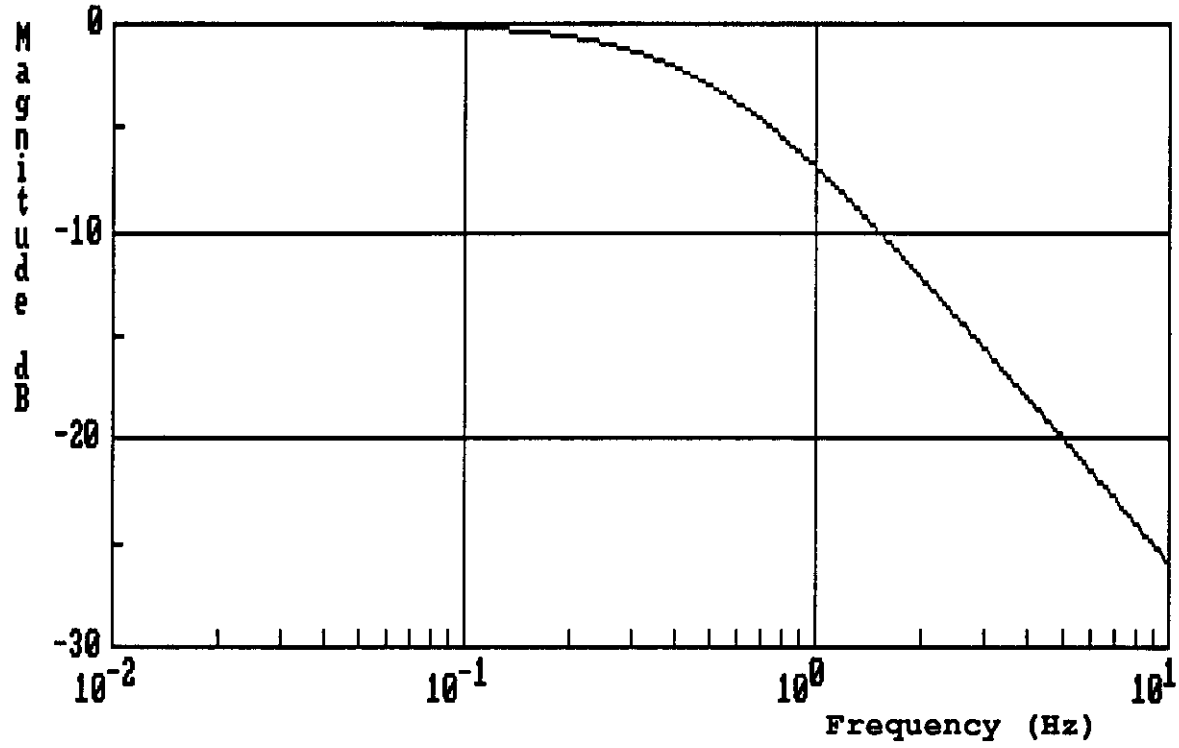


Figure IV.8. Closed-loop frequency response of the Mean-value Current Loop by using simplified transfer function analysis

IV.10. Simulation Results

The feedback current loop has been more accurately simulated by using Tutsim and Spice programs. The time-domain analysis has been performed by adding rectangular pulses to maximum and minimum current references and using Tutsim and Spice programs. Frequency response analysis has been performed by processing with Fansim the time-domain data generated with Tutsim. A description about the implemented simulation programs can be found in appendix D.

d-c Regulation Loop

The dynamic behavior of the d-c current loop has been analyzed by adding a rectangular pulse to both maximum and minimum current references. The simulated time response is shown in figure IV.9.

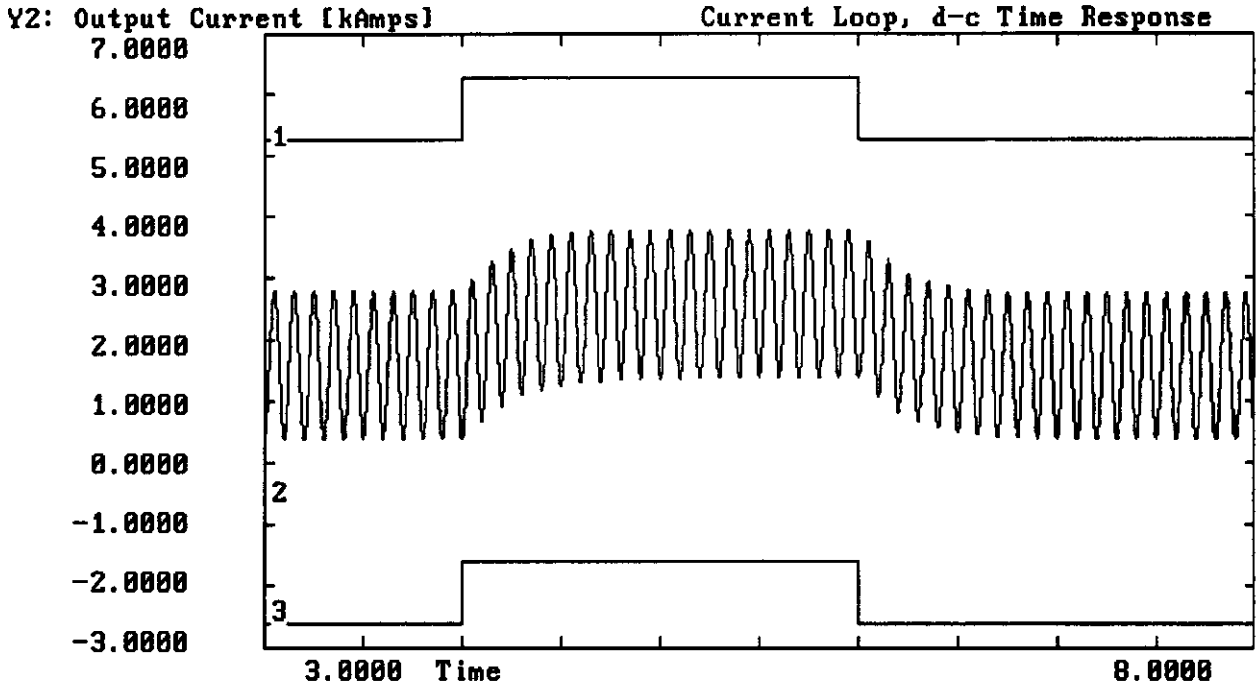


Figure IV.9. Time response of the d-c mean-value current loop
1. Maximum current reference
2. Output current
3. Minimum current reference

The closed-loop frequency response of the d-c current regulation loop, as estimated with Fansim, is shown in figure IV.10. Figures IV.8 and IV.10 show the similarity between the results obtained by transforming, using FFT routines, the simulated time response of the mean-value current loop and those obtained with transfer function analysis.

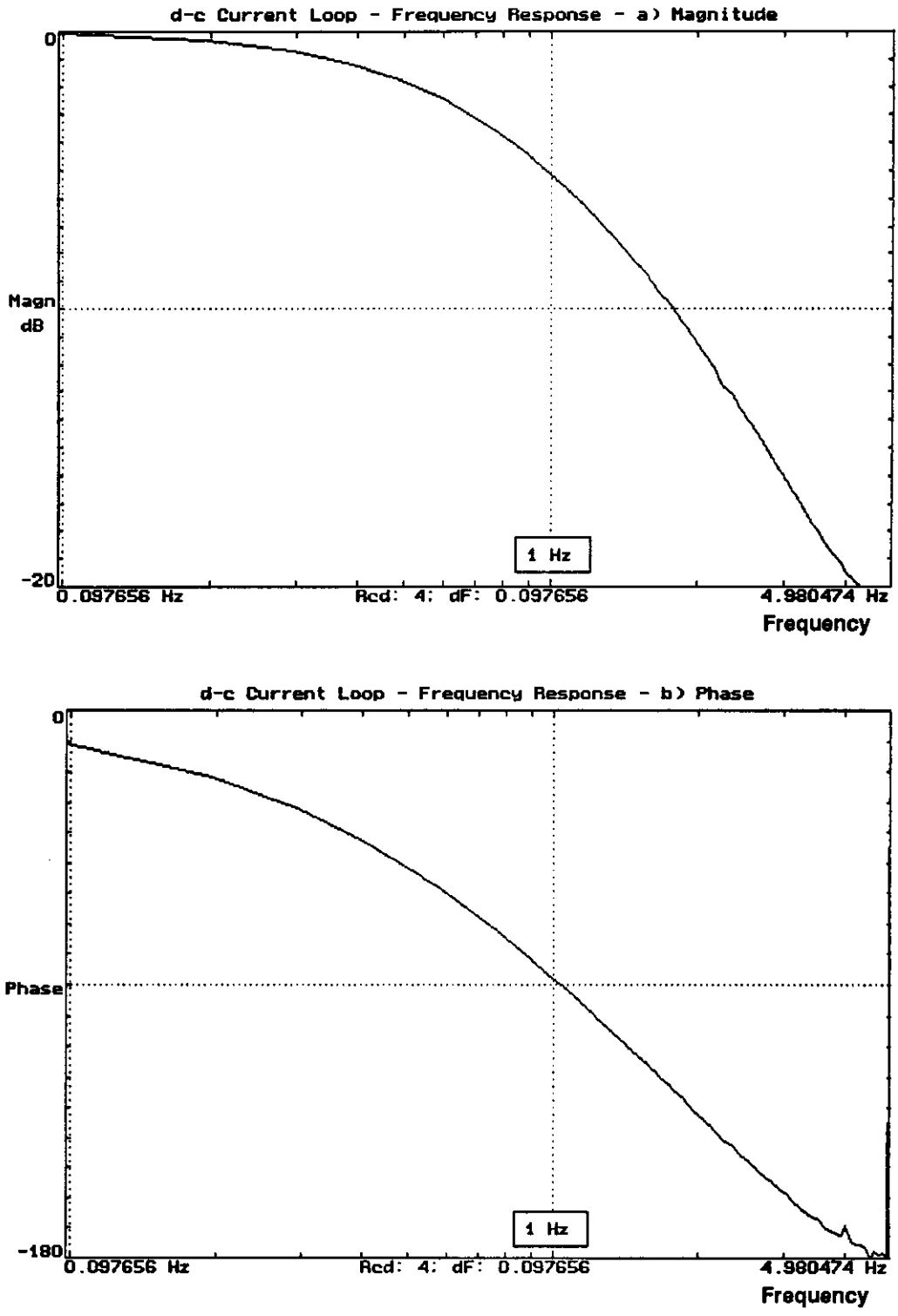


Figure IV.10. Closed-loop frequency response of the d-c Current Regulation Loop estimated with Fansim

a-c Regulation Loop

Likewise, the a-c amplitude current loop has been simulated with Tutsim and Fansim programs. The time-domain analysis has been performed by adding and subtracting a rectangular pulse to maximum and minimum current references respectively. The time response of the a-c amplitude current loop is shown in figure IV.11. Frequency response analysis has been performed by processing with Fansim the time-domain data obtained with Tutsim and the results are shown in figure IV.12. This figure is similar to that obtained with simplified transfer function analysis (Figure IV.8), having a bandwidth frequency of about 0.5 Hz.

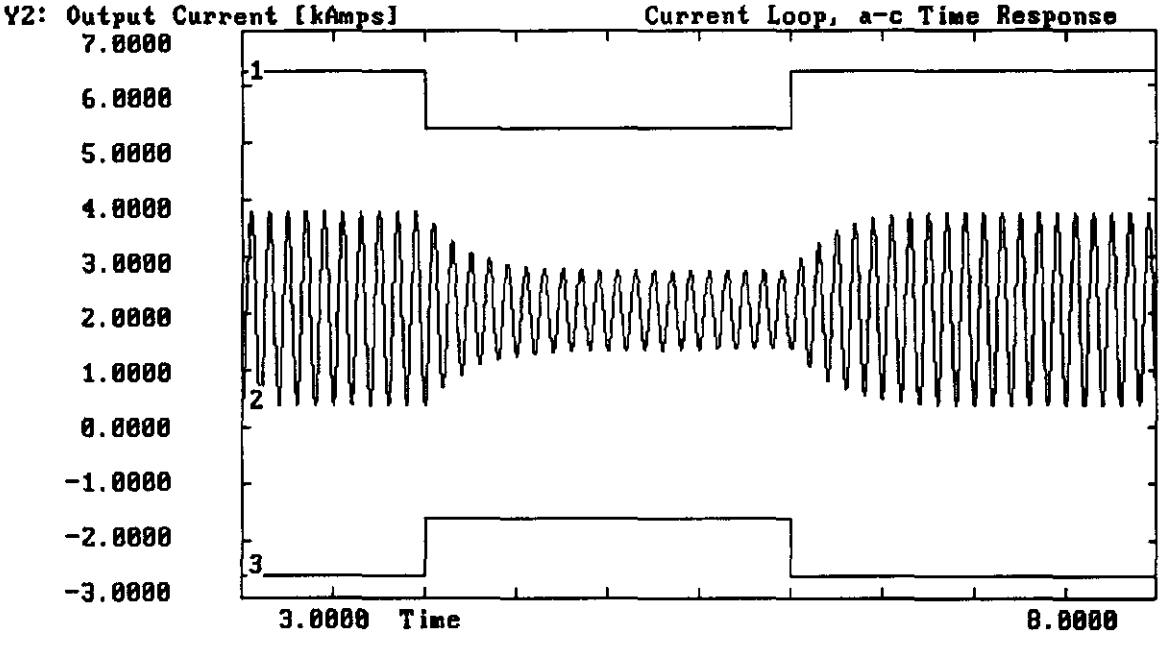


Figure IV.11. Time response of the a-c Amplitude Current Loop
1. Maximum current reference
2. Output current
3. Minimum current reference

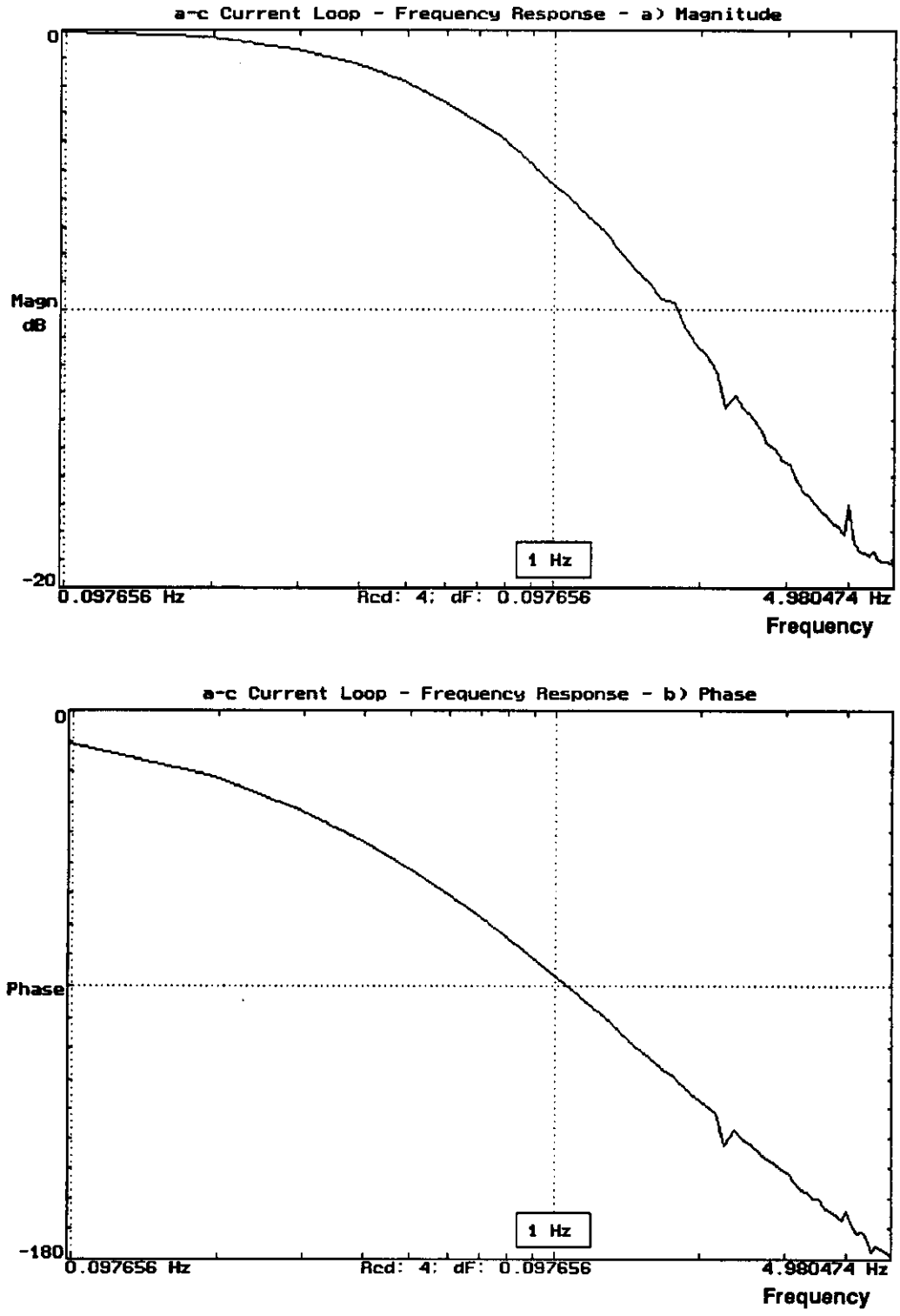


Figure IV.12. Closed-loop frequency response of the a-c Current Regulation Loop estimated with Fansim

Interaction between maximum and minimum current loops

The interaction between maximum and minimum current loops has been analyzed by adding a rectangular pulse to the maximum or minimum current references. The simulation results are presented in figure IV.13 showing that there is no interaction between maximum and minimum current loops.

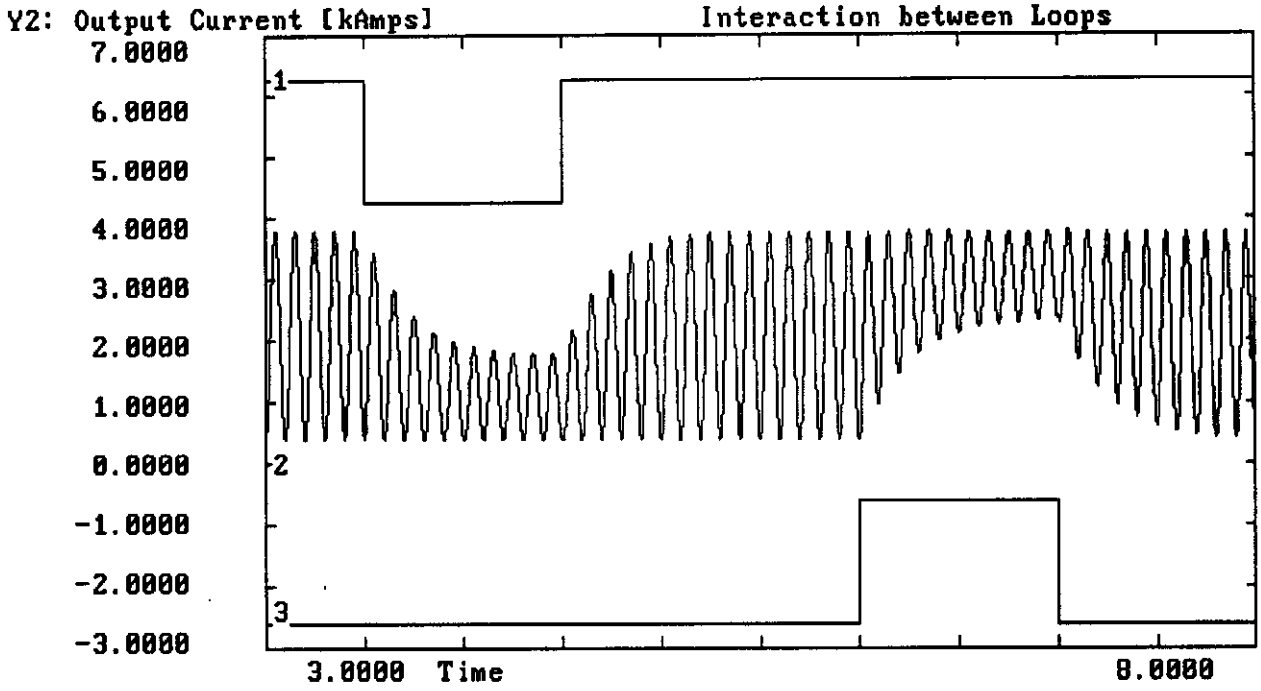


Figure IV.13. Interactions between Max. and Min. Current Loops
1. Maximum current reference
2. Output current
3. Minimum current reference

The block diagram of figure IV.3 has been also simulated with the Spice program implementing with operational amplifiers the cascade compensators. Power supply output voltage and magnet current under stationary state operation are shown in figure IV.14.

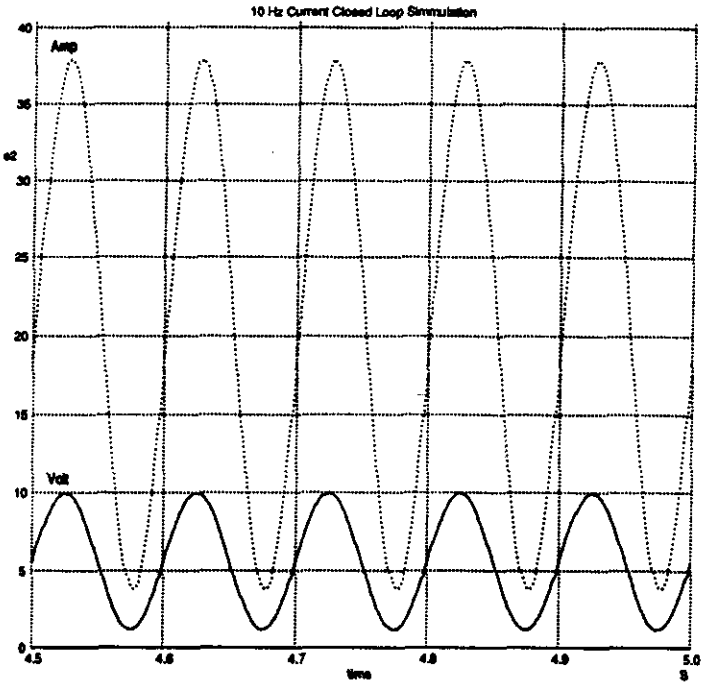


Figure IV.14. Stationary State Operation
— Output Voltage, ····Magnet Current

The transient behavior of the magnet current and output voltage are shown in figures IV.15 and IV.16 respectively. For more details about Spice simulations, see appendix D.

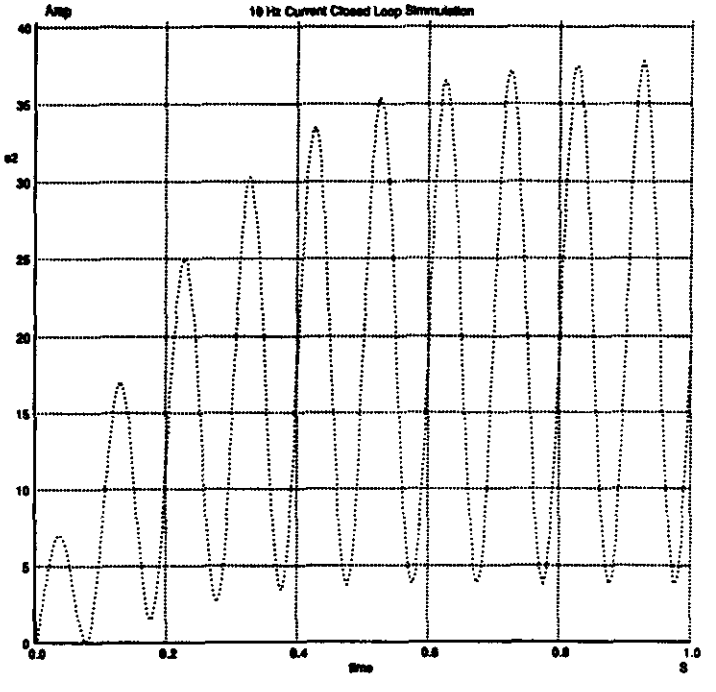


Figure IV.15. Magnet Current Transient behavior

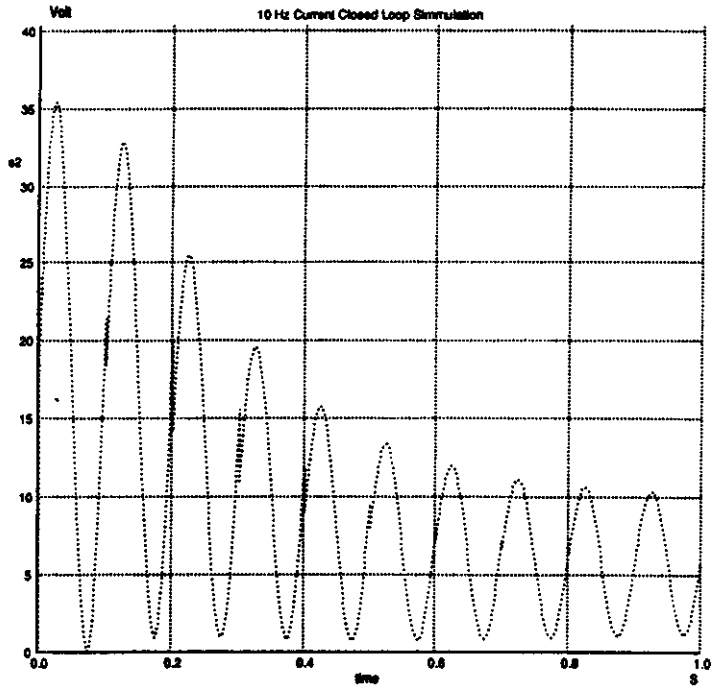


Figure IV.16. Output Voltage Transient behavior

The analysis and design of the current regulation loops for biased sine wave current mode of LEB have been presented in this section. The d-c and a-c components of the magnet current are regulated by independent loops and the interaction between both loops has been minimized. This feature as well as the similar dynamic behavior of d-c and a-c current loops are corroborated by computer simulations.

V. FIRING CIRCUITS

V.I. Introduction

In order to control the power deliver to the magnets with high efficiency, switching control techniques must be used. Considering the amount of power involved, phase control techniques and thyristor bridge converters are highly recommended. These nonlinear switching systems imposed certain restrictions on the frequency response bandwidth.

Twelve-pulse power bridge converters will be used in all magnet power supplies. The twelve-pulse converter is obtained by using two 6-pulse converters in series or parallel connection. The firing circuit has to fire the 12 thyristors of the bridge converter in such a way that the mean value of the output voltage can follow as close as possible, the voltage reference. For simplicity, only 6-pulse converters will be analyzed.

The output current will be usually unidirectional but the output voltage has to have the possibility of polarity changes. Thus, two-quadrant bridge converters will be used and freewheel diodes are not allowed.

The load is highly inductive and continuous current operation is supposed. In these conditions, neglecting the overlapped angle, the mean value of the output voltage will be related with the firing angle by the following equation [7]

$$V_o = V \frac{Sin\,(\pi/m)}{\pi/m} \cos\alpha \qquad (46)$$

where V_0 represents the mean value of the output voltage, V the maximum value of the a-c voltage, m the number of phases, and α the thyristor firing angle.

Equation 1 is interesting because it reveals that even in this ideal case, the mean output voltage is a nonlinear function of the firing angle. It is also important to note that the equivalent gain of the bridge converter is directly proportional to the peak value of the a-c voltage.

V.II. Firing Circuits Requirements

The most important firing circuits requirements for the ring magnet power supplies are:

- To have a minimum firing angle jitter to reduce subharmonic frequencies generated by the power converter.
- To have enough frequency bandwidth in order that the output follows the input reference with minimum error.

If the voltage loop has to reject voltage perturbations at 60 Hz and 120 Hz, the firing circuit bandwidth has to be higher than 200 Hz.

V.II.1. Firing Circuit Model

The frequency bandwidth limitation of the firing circuit can be better understood by developing a simple model for an ideal firing circuit and power converter. It is important to point out that the only available control is the firing angle of each thyristor. Thus, we are in the presence of a switching system where the sampling frequency is imposed by the characteristics of the a-c supply and the power converter. For a 60 Hz a-c supply and a 12-pulse converter, the sampling frequency has a value of f_0 = 720 Hz.

The model is derived with the help of figure V.1 where have been represented an arbitrary voltage reference signal and the d-c terminal voltage of an ideal firing circuit and power converter.

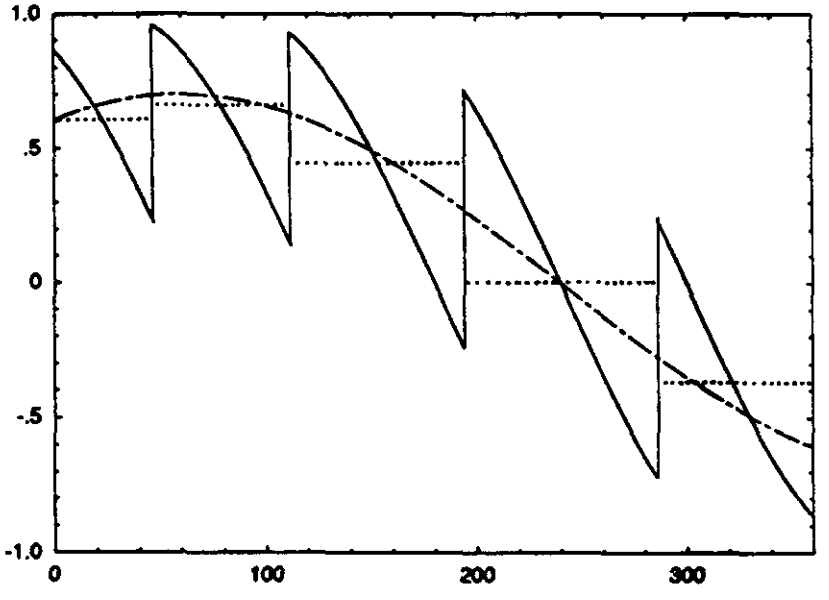


Fig. V.1 · - voltage reference
– voltage output
··· model output

A simple way for modeling this nonlinear system is to use a f_0 frequency sampler and a zero order hold. The output of this model has been represented in dot line in figure V.2 and its transfer function is given by [4]

$$F(s) = \frac{(1-e^{-sT})}{sT} = e^{-sT/2}\,\frac{(e^{sT/2}-e^{-sT/2})}{sT} \qquad (47)$$

For low frequencies, this transfer function can be approximated by

$$F(s) \approx e^{-sT/2} \tag{48}$$

Thus, in the low frequency band, the ideal model for the firing circuit and bridge converter has unitary gain and linear phase. This linear phase, taking a value of -90° at 360 Hz, plays an important role in closed loop operation limiting the maximum frequency bandwidth of the regulation loops.

V.III. Review of Firing Circuits Techniques

In order to regulate the output voltage of a phase-controlled power converter, it is necessary to control the thyristor firing angles. Different methods are available for achieving this goal and, they can be classified as closed loop and open loop techniques.

V.III.1. Closed Loop Techniques

These techniques make use of the information contained in the output voltage waveform for generating the firing pulses. An extremely simple circuit results and the addition of external signals synchronized with the a-c supply are not required. The operating principle of this method can be easily understood from the analysis of figure V.2 [7].

The main advantage of this technique is its simplicity. The disadvantages are related with its inherent closed loop operating principle which generates instability problems. These problems can be solved by reducing the closed loop gain or increasing the circuit complexity [8][9]. In any case, the resulting passband frequency response is usually reduced and several sampling periods are required in order to modify the thyristor bridge operation from rectification to inversion or reciprocally.

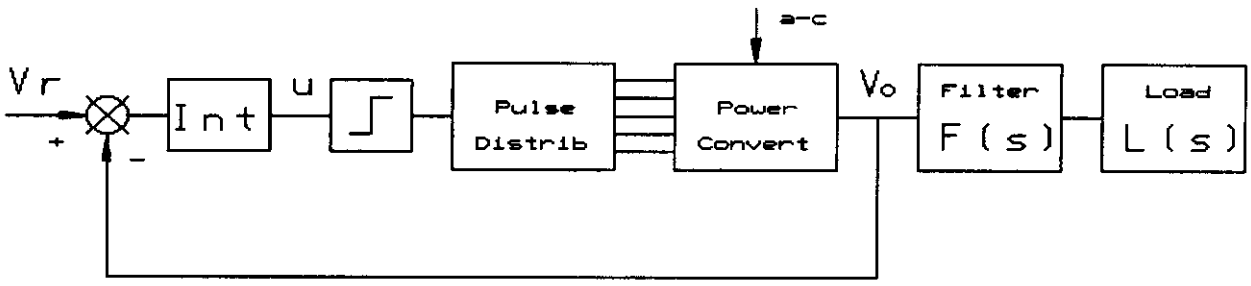


Fig. V.2.a) Block Diagram of a closed loop firing circuit

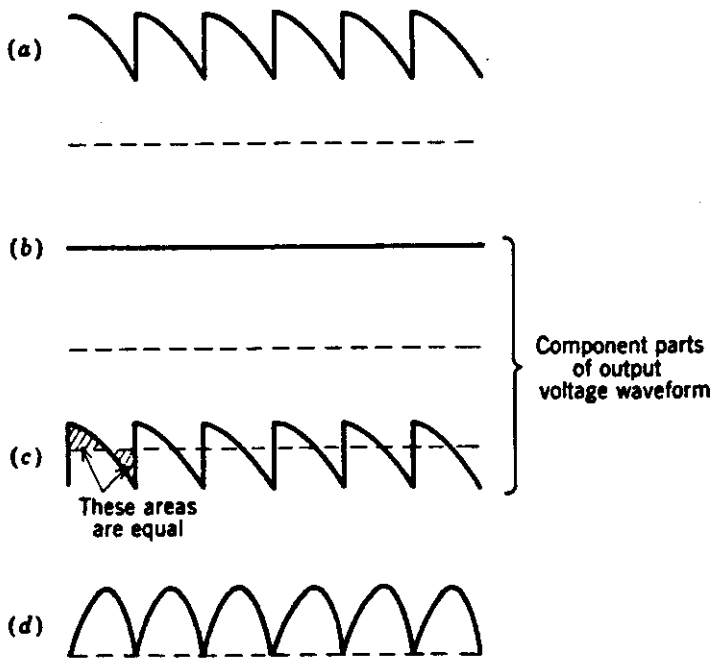


Fig. V.2.b) Voltage waveforms corresponding to a closed loop firing circuit
a) converter output voltage waveform
b) direct voltage component
c) a-c ripple voltage component
d) integrated ripple voltage waveform

V.III.2. Open Loop Methods

The basic principle of these methods consists in comparing the reference voltage with an external signal (sawtooth or cosine wave) synchronized with the a-c supply. At the intersection point of the external signal with the reference voltage a firing pulse is generated. A block diagram of an open loop firing circuit is shown in figure V.3.

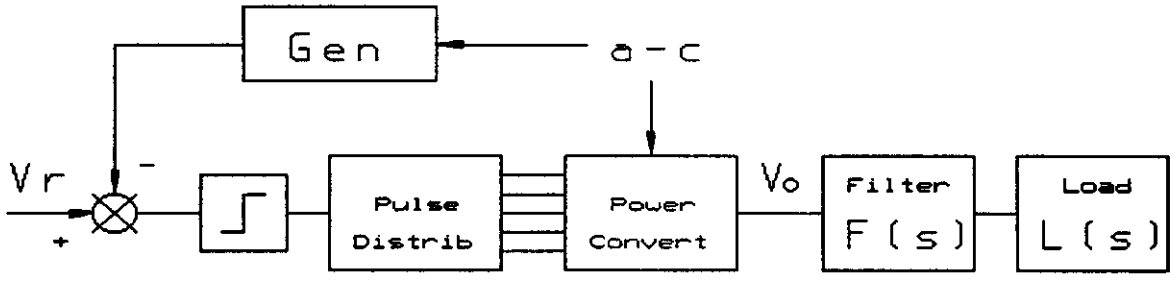


Fig. V.3. Block diagram of an open loop firing circuit

The range of possible firing angles of each thyristor is theoretically comprised between 0° and 180°. Thus, a monotonic increasing or decreasing external signal extended over 180° is required. The more usual signals applied are cosine wave or sawtooth signals [7].

When several thyristors are used, one possible solution is to use an individual phase control for firing each thyristor. If this method is applied to 12-pulse thyristor bridge, 12 external signals shifted by 30° are required in order to generate the 12 firing pulses [10]. Different kinds of implementations and simplifications reducing the required number of external signals and comparators have been presented in the literature. Among them two of the more interesting methods are analyzed here.

III.2.-a) The cosine wave crossing method

Firing pulses are generated in this method by comparing the voltage reference with external cosine wave signals directly derived from the a-c supply [1], [8]. The operating principle is illustrated in figure V.4 where, for the case of a 6-pulse power converter, have been represented the a-c supply waveforms, the reference voltage, external cosine wave signals and the output voltage.

The most important characteristics of this method are:

- It is seen in the figure that when the reference changes its value, the firing angle is immediately set at the new value. Thus, the circuit presents the maximum speed theoretically available.
- There are no stability problems because it is an open loop method.
- As the external signal, has a cosine waveform, it is easy to verify that the equivalent gain of the whole system is constant. In fact, this gain defined as the ratio between the mean output voltage V_o and the reference voltage V_r, is constant and independent of the firing angle [11].
- If, as usual, the external signal is directly derived from the a-c supply, its amplitude will be also proportional to the a-c voltage amplitude. In these conditions, it can be easily proved that a feed forward compensation for a-c voltage perturbations is automatically achieved [11].

Some important problems related with this method are its sensitivity to peaks and other transient perturbations that can appear in the a-c voltage. The method is also sensitive to harmonic distortion terms in the a-c voltage. These problems can be reduced by increasing the circuit complexity including integration, filters or other similar techniques for obtaining noise-free external cosinusoidal signals.

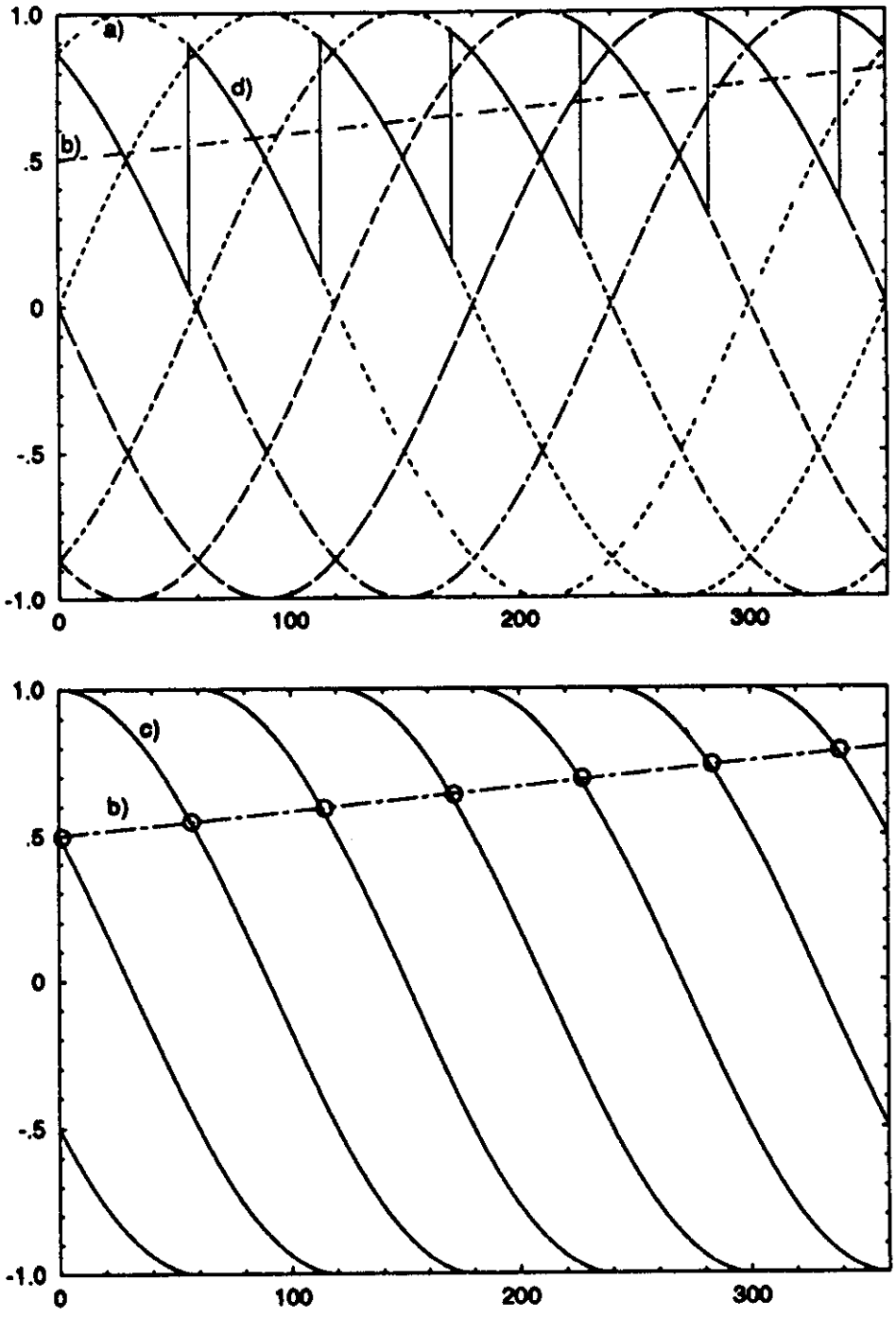


Figure V.4.
Waveforms illustrating the basic principle of the cosine wave crossing method.
a) a-c supply waveforms; b) reference voltage; c) external cosine wave signals; d) output voltage.

V.III.2.-b) Phase Locked Loop (PLL) Techniques

The principle of individual phase control, can be also applied by using saw-tooth signals instead of cosine waveforms. In this case a firing angle proportional to the reference signal is obtained and the equivalent gain of the whole system is nonlinear. The operation principle is shown in figure V.5 for the case of a 6-pulse power converter.

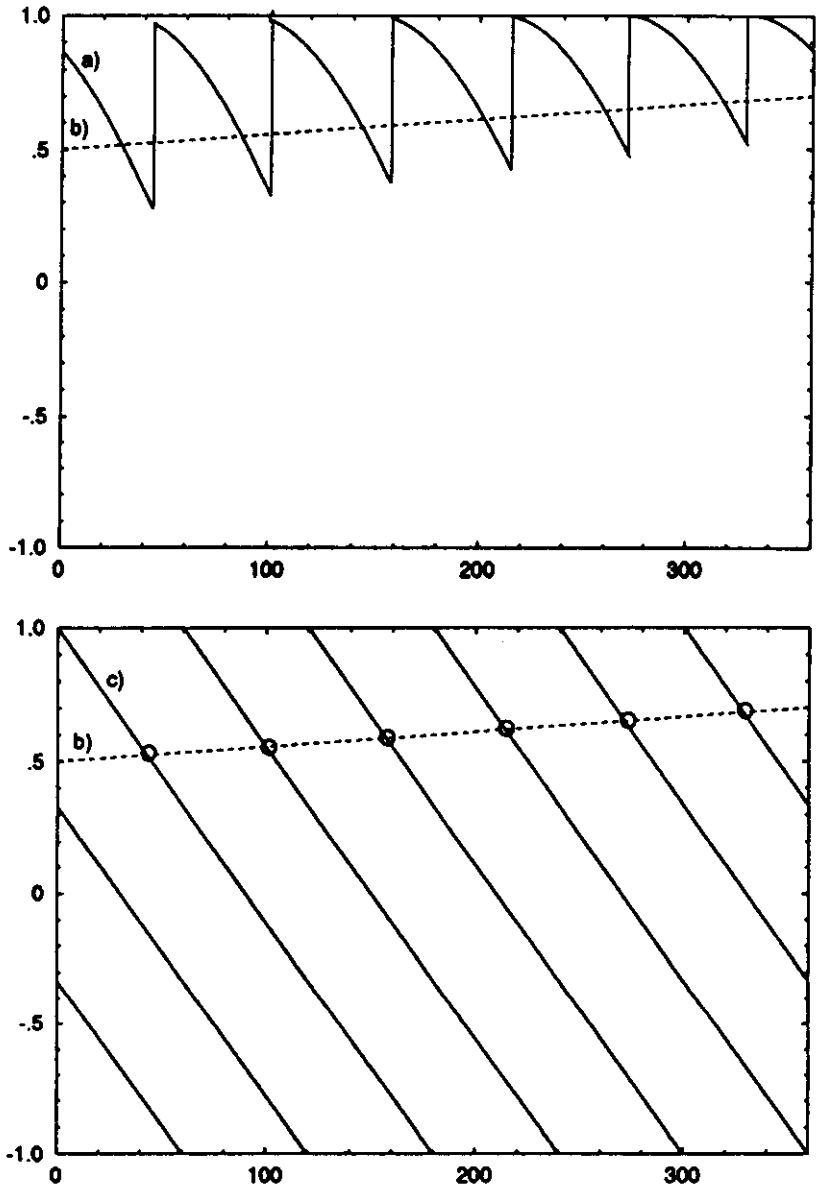


Figure V.5.
Waveforms illustrating the basic principle of individual phase control using a saw-tooth external signal.
a) output voltage; b) reference voltage; c) external saw-tooth signals.

In the figure the various sawtooth waves of an individual phase-control circuit are displayed together with an arbitrary varying reference signal. It can be seen in this figure that only a part of each sawtooth is involved in the actual timing process. Taking into account that firing pulses corresponding to different thyristors are generated in a sequential way, a common timing wave does always exist.

One interesting result of the sawtooth case is that for passing from one ramp to the following it is only necessary to increase or reduce the sawtooth signal voltage in a fix amount of voltage. Thus, the common timing wave required for generating all firing pulses can be derived from only one sawtooth signal.

The main idea of PLL methods is to generate this composed timing wave signal in such a way that only one comparator and pulse generator were required. A synchronized firing pulse distributor is then used in order to apply each pulse to the appropriate thyristor.

The circuit is composed by a sawtooth generator synchronized with the a-c supply voltage by means of a PLL circuit. Thus, the generator output is a 60 Hz sawtooth. For a 12-pulse power converter, the common timing wave has a fundamental frequency of 720 Hz. This waveform has to be synthesized from the 60 Hz sawtooth and the knowledge of past firing angles. Some different implementations are possible to attain this goal.

V.IV. PLL Firing Circuit Implementations

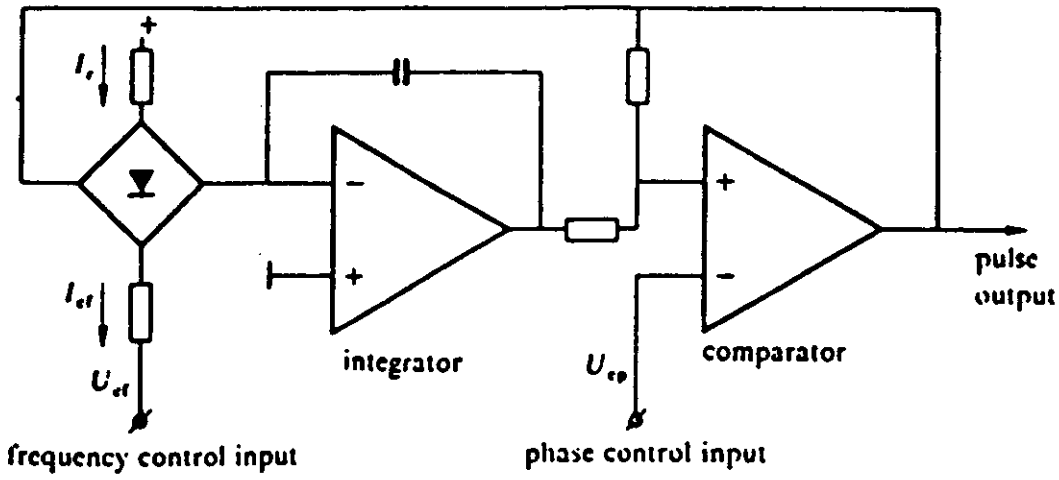
The PLL firing circuit method seems to be the most suitable for SSC magnet power supplies requirements. Three of the different PLL firing circuit implementations are briefly analyzed here.

V.IV.1. Double Oscillator Firing Circuit

The PLL method analyzed in reference [12] has been used in some power supplies firing circuits at Fermilab.

A close examination of the resulting waveform (figure V.5) reveals some typical characteristics, eventually leading to a practical pulse-timing oscillator circuit. The basic circuit should comprise a ramp generator and a comparator. Each time the ramp reaches the reference level it should be reset over a fixed distance as to adopt the instantaneous value of the next sawtooth. The slope should be controlled in order to obtain an average repetition frequency of exactly six times the main's frequency.

A 60 Hz sawtooth is generated and synchronized with the a-c supply by using one PLL circuit. The common timing wave is generated by using a second oscillator, which uses the voltage reference signal or phase control input and provides the required 720 Hz sawtooth output. The operation principle of this second oscillator is shown in figure V.6.



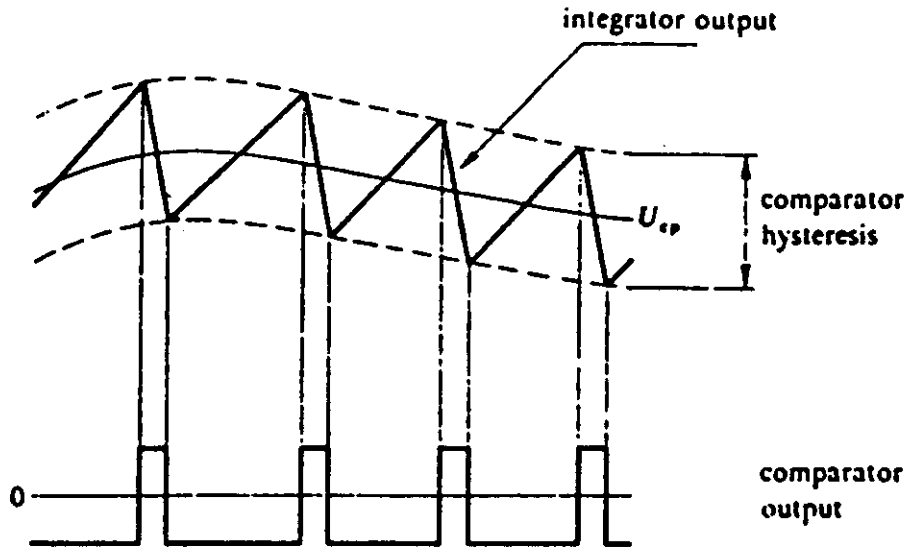


Figure V.6.
Practical circuit of common timing wave generation and associated waveforms.

In order to obtain an appropriate operation, this second oscillator has to have an appropriate slope and has to be synchronized with the a-c supply. For obtaining this, the 60 Hz sawtooth is related with the 720Hz common timing wave in such a way that both sawtooths where synchronized and having the same slope. The block diagram of the circuit is shown in figure V.7.

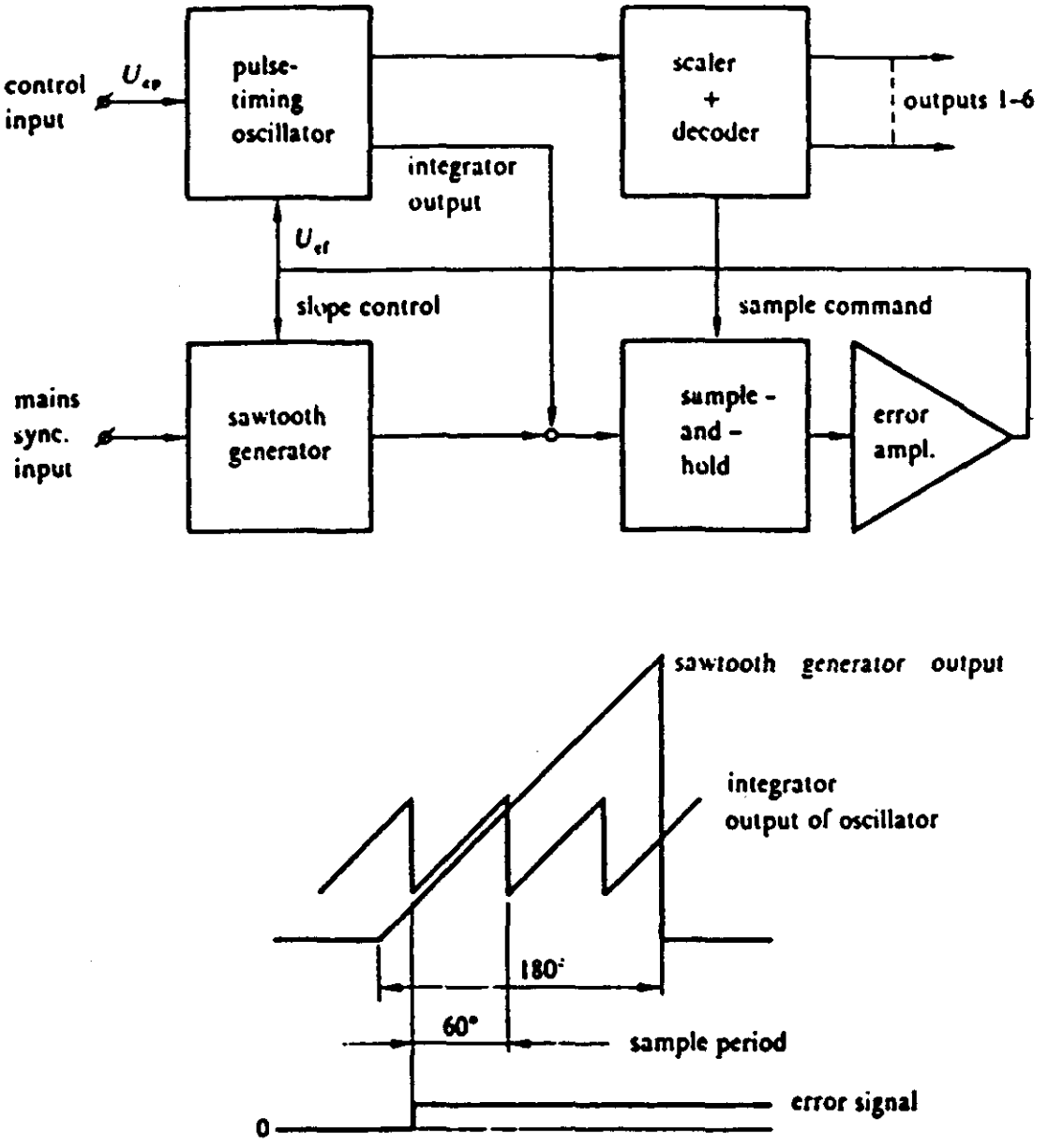


Figure V.7.
Block diagram of firing circuit employing a common timing wave generator with autonomous locking and associated waveforms.

Although this method has two closed loops, it can be considered as an open loop method because these loops are only used for generating the common timing wave and they do not use the output voltage of the bridge converter.

PLL methods have the properties of any open loop method of having maximum response speed without presenting stability problems. Moreover as the common timing wave is synthetically generated, PLL methods present highly immunity to transient perturbations, distortion and noise in the a-c supply.

The main drawbacks are due to the fact that feedforward compensation for a-c amplitude perturbations is not automatically obtained and that the equivalent transfer function is non linear.

V.IV.2. Standard PLL Firing Circuit

A general purpose thyristor firing circuit can be developed by using only one oscillator and PLL loop. The operation principle can be readily understood from the simplified block diagram of figure V.8.

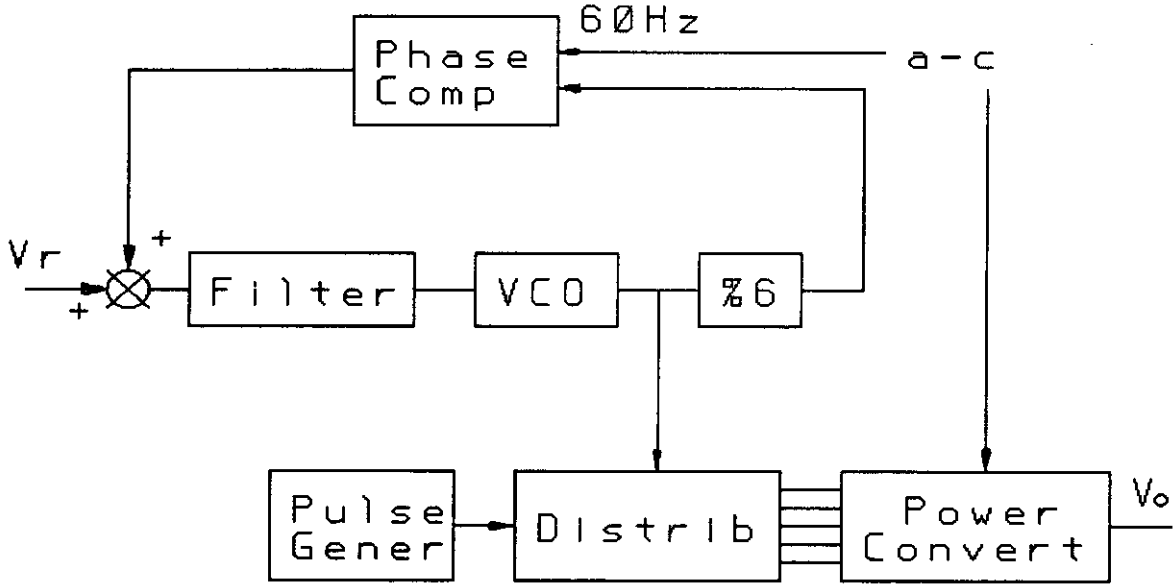


Figure V.8.

The PLL circuit compares the main voltage phase with the phase of the output signal (divider by 6). The voltage reference is added at the phase comparator output. When the system is locked, the d-c voltage at the filter output has a small value. The d-c voltage at the phase comparator output has a negative value of similar amplitude than the voltage reference. Therefore, the output signal will be delayed with respect to the main voltage and the delay angle will be proportional to the voltage reference.

The main drawback of this scheme is that it is not an open loop firing circuit. In fact, the PLL is not used for generating an external signal as in figure V.3 but for the direct generation of the firing pulses. A direct consequence of this close loop operation is the slow circuit response to changes in the voltage reference.

The bandwidth frequency response of the circuit can be improved by increasing the operation frequency of the phase comparator and the circuit complexity. This can be done by increasing the number of main voltage phases to be used by the PLL circuit. A block diagram of a circuit that uses three main voltage phases is shown in figure V.9 [13].

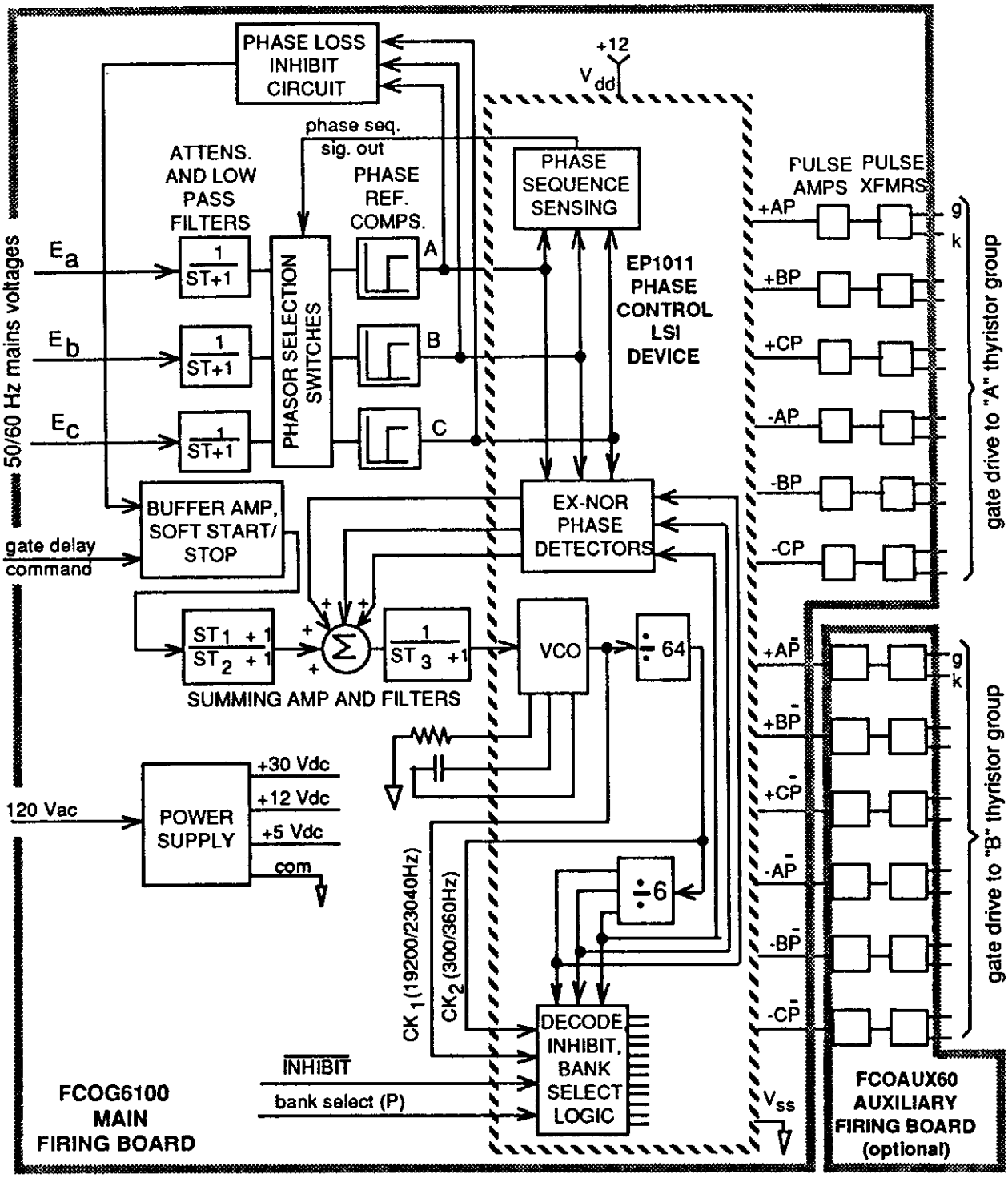


Fig. V.9. Firing circuit block diagram

In a firing circuit recently developed by Enerpro the operation frequency of the phase comparator has been increased up to 720 Hz by using 6 phases of the main voltage [14]. By using this structure, the PLL bandwidth has been increased up to 200 Hz [14].

IV.3. Digital Firing Circuits

It is interesting to show that it is possible to develop an open loop PLL firing circuit with only one PLL loop used to generate a digital 60 Hz sawtooth synchronized with the main a-c supply. The common timing wave signal can be directly derived from this sawtooth [15].

The operation principle of the method can be easily understood from the analysis of figure V.10. The 60 Hz 360° reference ramp and the individual ramp for each thyristor have been represented in this figure. The main idea of a digital generation of the common timing wave is to notice that the less significative bits of all individual ramps including the reference ramp are identical. Only the 4 most significative bits corresponding to the division by 12 are different.

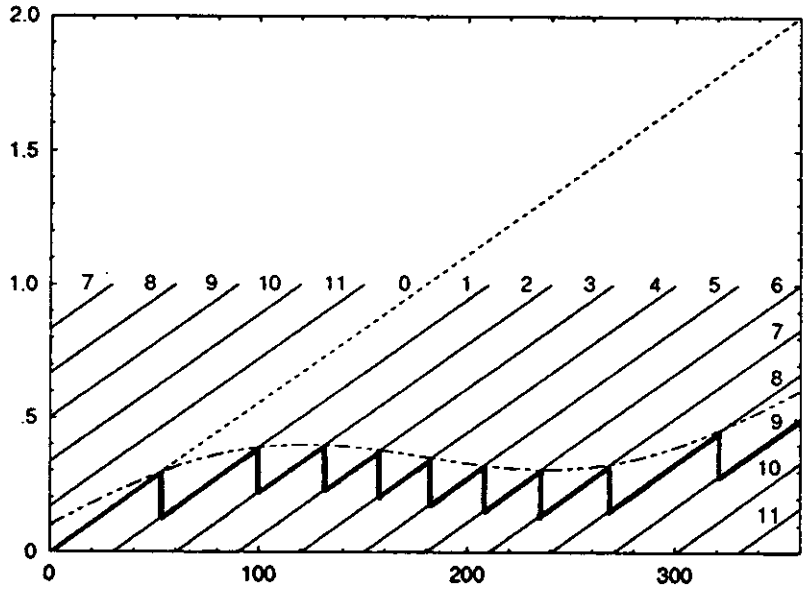


Fig. V.10. -- reference ramp
· - voltage reference
_ sawtooth signals
_ common timing wave

One possible implementation of a digital firing circuit based in this idea, is represented in block diagram en figure V.11 [15].

The VCO output provides a clock signal and a digital counter is used for generating a digital 60 Hz 360° reference ramp. The output of the counter is divided by 12 and locked with the a-c supply by the PLL loop. The number N_s stored in the divider by 12 has to be comprised between 0 and 11 and it is possible to pass from the reference ramp to any other ramp by reducing N_s by the number corresponding to the ramp to be generated (figure V.10). A counter to 12 synchronized with the firing pulses determines the number of the ramp to be generated and a difference circuit provides the most significative bits of this ramp. A digital comparator is then

used for generating the firing pulses. The N bits less significative of the reference voltage are compared with the contents of the N bits counter and the 3 bits more significative of the voltage reference are compared with the output of the difference circuit. When the comparator result is zero, a firing pulse is generated.

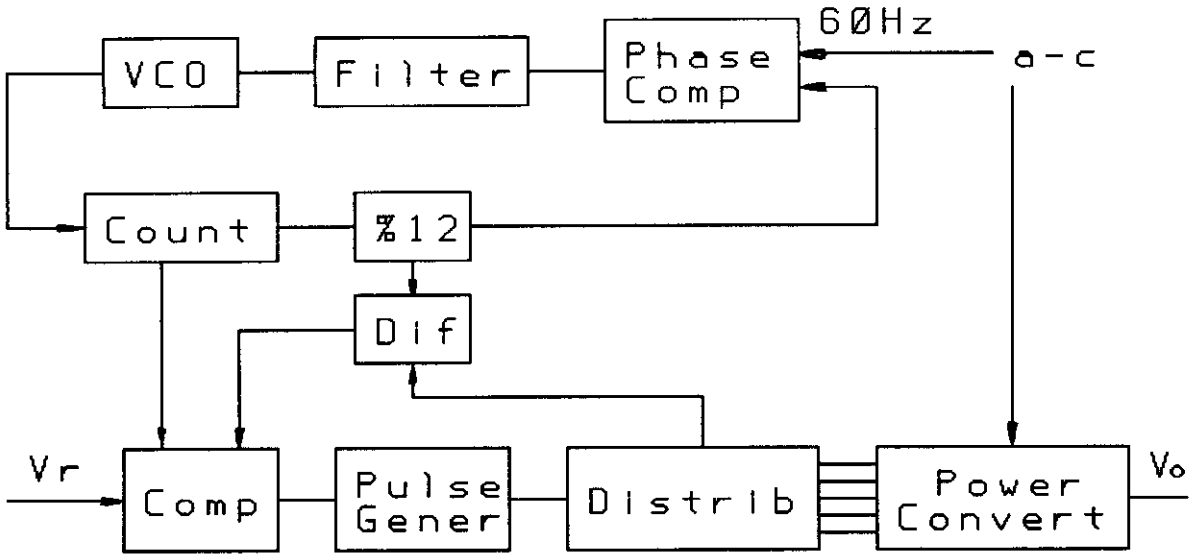


Fig. V.11. Digital firing circuit

The clock frequency determine the angle resolution of the firing circuit and can be modified by changing the divider number N of the PLL loop. In order to give an idea of the number of bits required for obtaining a given angle resolution, the case of a 12 bits digital voltage reference will be considered. In this case, N is equal to 9, the clock frequency will be of $60*12*2^9$ that is near to 370 KHz (368640 Hz). And the resolution in angle will be of about 0.1°.

V.V. Firing angle jitter and potential transformers

The ripple frequency, for a 12 pulse power converter, is 720 Hz. This frequency is the lower frequency component of the idealized voltage output waveforms associated with this circuit, which assume a constant reference and a perfectly symmetric operation. Under real operation a small amount of subharmonic frequencies is always present. The main contributors to these subharmonic components are voltage and phase unbalances which might exist between the 6-phase input voltages, impedance unbalances and jitter in the thyristor firing angles.

The load current accuracy requirement of 100 ppm has to be met in both, maximum and minimum current limits. The impact of small unbalances is more important when the load current has its minimum value. In this case, the thyristors firing angle will be higher than 80° and small phase unbalances or firing angle jitter will produce a high relative voltage error. For having a reduced amount of

subharmonic components it is wisdom that the total phase error including phase unbalance and firing angle jitter was held within 0.5°.

Another subject that merits some comments are the synchronization circuits. All open loop firing circuits generate external signals, which have to be synchronized with the main ac supply. To this end, resistive dividers or potential transformers are generally used. In the LEB application, the use of potential transformers is highly recommended because of the high voltage isolation required. The accuracy of this potential transformer depends on the adopted topology for the firing circuit. For Enerpro firing circuits, an instrument potential transformer with an accuracy as high as 0.1° [16] could be required. But, if a double oscillator or a digital firing circuit is adopted, the accuracy of the instrument potential transformer can be relaxed. In fact, the synchronization with only one of the main supply phases is needed and phase errors in the potential transformer can be eventually corrected by the voltage loop.

V.VI. Conclusions

Closed loop firing circuits are not generally recommended for SSC magnet power supplies due to their slow dynamic behavior and their inherent stability problems. The twelve pulse firing circuit recently developed by Enerpro, having a bandwidth of 200 Hz, could be used but the voltage loop has to be designed in order to compensate the firing circuit pole at 200 Hz.

When the voltage loop provides enough rejection to a-c voltage perturbations, PLL methods are preferred among other open loop methods due to their high immunity to noise in the a-c supply. The non linear static characteristic of the bridge converter can be solved by including a linearizing circuit in the reference signal path.

VI. DCCT SPECIFICATIONS

Zero Flux DC Current Transducer

Specifications for LEB current measurement

ELECTRICAL	
DC Current Range	Zero to 5000 Amps
Output Voltage @ F.S.	+10 volts DC
Output Impedance	< 5 mOhm
Output Current Limit	> 2 mA
Digital Output (Serial @ Parallel)	20 bits
Sampling frequency (external clock)	up to 2 kHz
Saturation Level	110% of F.S.
Small Signal Bandwidth	> 10 kHz
Slew Rate	> 10 Amp/ms
TRANSFER FUNCTION	
Initial error	< 50 ppm of F.S.
Error vs. temperature	< 0.1 ppm of F.S./K
Error vs. time	< 1 ppm of F.S./month
Linearity error	< 10 ppm max
Output Noise	
0 - 1 Hz (RMS)	< 1 ppm of F.S.
0 - 2 kHz (RMS)	< 2 ppm of F.S.
0 - 100 kHz (RMS)	< 5 ppm of F.S.
Electronics Operating Temperature Range	15 - 35 Deg. C.
Measuring Head Operating Temperature Range	10 - 50 Deg. C.
Power Supply	
Nominal Voltage and Frequency	120 VAC @ 60 Hz
Voltage Range	108 - 132 VAC
Frequency Range	58 - 62 Hz
Isolation Voltage (Measuring Head to Bus Bar)	10000 VDC for 1 min
Zero Flux and Error Current Indicators	Relay Contacts
Warm-up time	15 min. max

MECHANICAL

Electronics Module

Minimum Height, Standard 19" E.I.A., Rack Mount Assembly

Measuring Head

Integral 5000 Amp DC bus bar with connection flags hole patterns

Cable Length (Measuring Head to Electronics Module) 20 m

VII. REFERENCES

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APPENDIX A

VOLTAGE LOOP TUTSIM SIMULATIONS

The L.E.B. power supply voltage regulation loop (fig. I.4.) has been simulated using Tutsim and Spice. In Tutsim implementation, the transfer function of the different voltage loop blocks are simulated. In order to simplify the diagram and reduce the number of required integrator blocks a variable state model is used to simulate each transfer function. The procedure is explained by means of a second order transfer function.

$$\frac{Y(s)}{U(s)} = \frac{b_0 + b_1 s}{1 + a_1 s + a_2 s^2} \tag{1}$$

Equation 1 can be written as

$$[1 + a_1 s + a_2 s^2] Y = [b_0 + b_1 s] U \tag{2}$$

The state variable X_1 is defined by specifying the output Y as

$$Y = [b_0 + b_1 s] X_1 \tag{3}$$

The input U is then specified as

$$U = [1 + a_1 s + a_2 s^2] X_1 \tag{4}$$

Defining, as usual, $X_2 = \dot{X}_1$ the state equations are

$$\begin{aligned} \dot{X}_1 &= X_2 \\ \dot{X}_2 &= \frac{U}{a_2} - \frac{a_1}{a_2} X_2 - \frac{1}{a_2} X_1 \end{aligned} \tag{5}$$

The output equation is

$$Y = b_0 X_1 + b_1 X_2 \qquad (6)$$

The Tutsim implementation of the second order transfer function obtained by using equations (5) and (6), is represented in figure A.1.

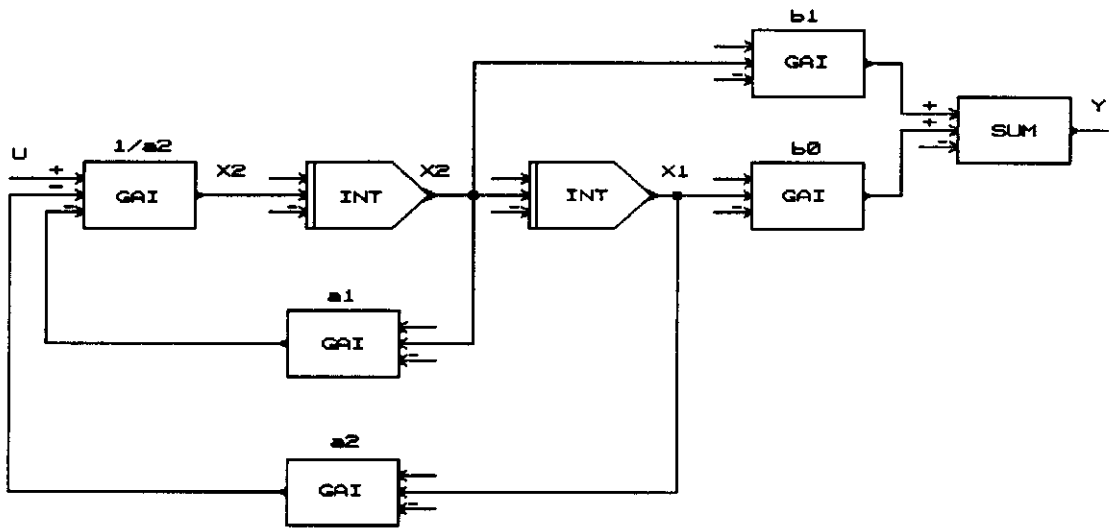

Figure A.1.
Tutsim implementation of a second order transfer function

The procedure developed here for a second order system can be directly applied to higher order transfer functions. For first and second order systems Tutsim has alternative solutions using special blocks as Iwz, Pid and Seo.

The Tutsim implementation of the L.E.B. power supply voltage regulation loop is shown in figure A.2. The electrical components of the output filter and load had been indicated in figure A.2. (61 to 70) but, Tutsim require block implementation for L, C, R and G components. For details about electric circuits implementation see Tutsim manual appendix C, Electric Circuits - Parts 1 and 2. The Tutsim model corresponding to figure A.2 is listed in page A-4.

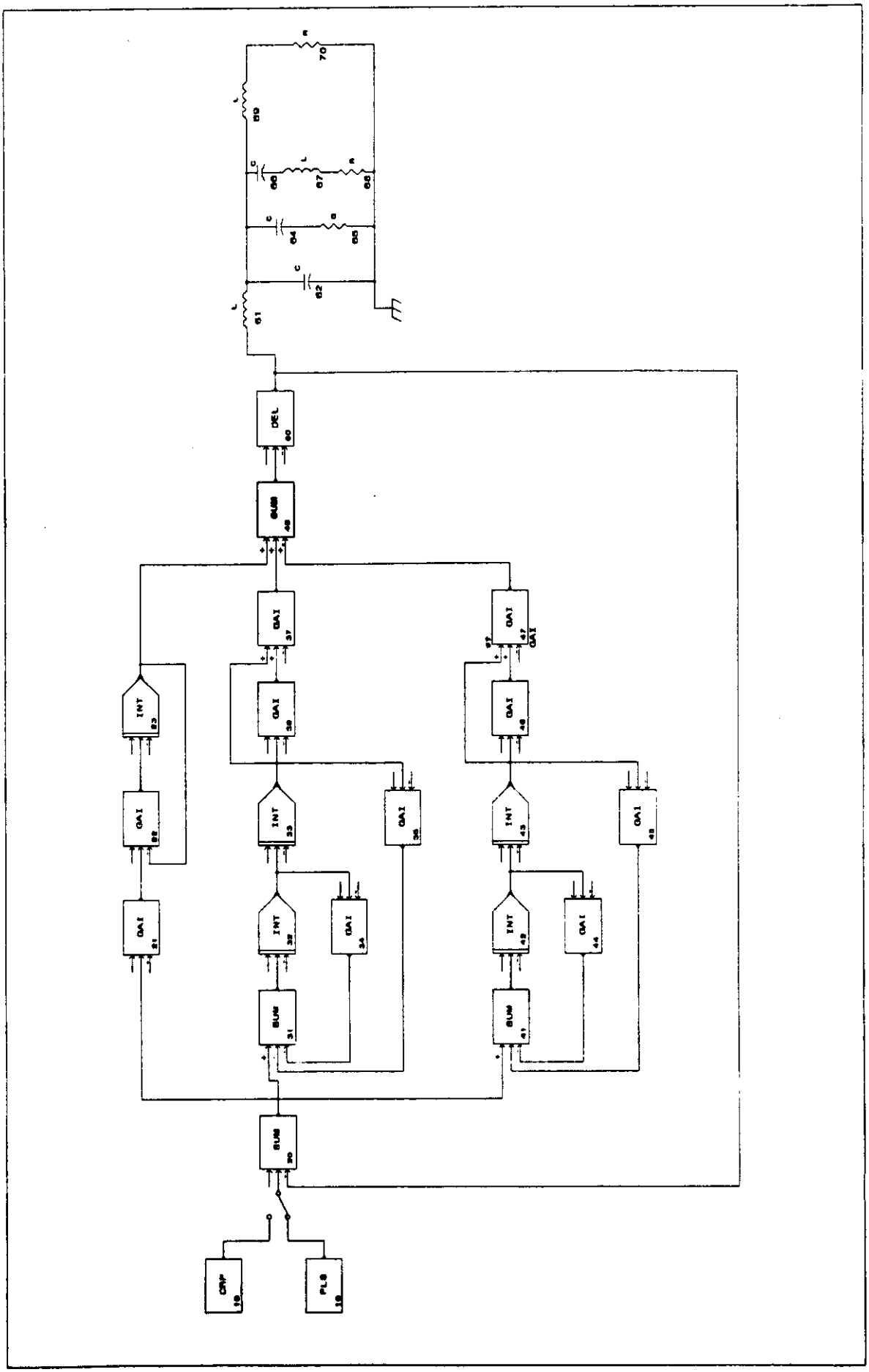

Figure A.2.
Tutsim implementation of the L.E.B. voltage loop

```
PROFESSIONAL VERSION OF TUTSIM

Model File: b:\tutsim\volta.sim
Date:      8 /    21 /  1991
Time:      9 :    48
Timing:  10.000E-06  ,DELTA  ;   0.0500000  ,RANGE
PlotBlocks and Scales:
Format:
     BlockNo,  Plot-MINimum,  Plot-MAXimum;  Comment
Horz:      0 ,   0.0000     ,   0.0500000  ; Time
  Y1:     10 ,   0.0000     ,   5.000E+03  ;
  Y2:     60 ,  -2.000E+03  ,   1.000E+03  ;
  Y3:     62 ,  -1.000E+03  ,   2.000E+03  ;
  Y4:        ,              ,               ;


   0.0000          10 PLS
   0.0010000
   1.000E+03
                   20 SUM      10     -60
 100.0000          21 GAI      20
   6.2500          22 GAI      21     -23
   0.0000          23 INT      22
                   31 SUM      20     -34     -35
   0.0000          32 INT      31
   0.0000          33 INT      32
   9.4250          34 GAI      32
 142.122E+03       35 GAI      33
 377.0000          36 GAI      33
  94.2500          37 GAI      36      32
                   41 SUM      20     -44     -45
   0.0000          42 INT      41
   0.0000          43 INT      42
  18.8500          44 GAI      42
 568.489E+03       45 GAI      43
 754.0000          46 GAI      43
 188.5000          47 GAI      46      42
                   49 SUM      23      37      47
 100.000E-06       60 DEL      49
 700.000E-06
   0.0000
   0.0019800       61 L        60     -62
   0.0000
   0.0013000       62 C        61     -65     -67
                              -69
   0.0000
   0.0040000       64 C        65
   0.0000
   0.7090000       65 G        62     -64
  49.000E-06       66 C        67
   0.0000
   0.0010000       67 L        62     -66     -68
   0.0000
   0.0050000       68 R        67
   0.1000000       69 L        62     -70
   0.0000
   0.1060000       70 R        69
```

Open loop analysis

The open loop transient behavior of the LEB voltage regulator can be performed by opening the feedback loop in figure A.2. This can be easily done by replacing the addition block (20) by a unitary gain. The usual sources employed (block 10) are impulse, step and sine wave or frequency modulated sine wave. A sine wave signal width frequency linearly swept from 20Hz to 200Hz has been used in figure A.3.

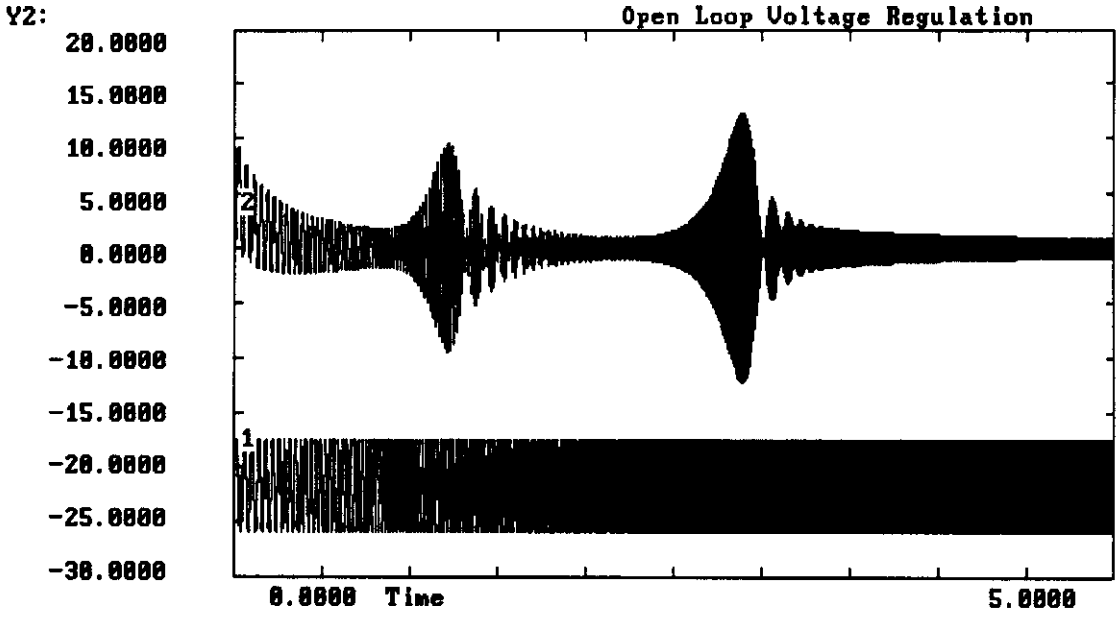

Figure A.3.
Tutsim Simulation of the Voltage Regulation in open loop
1 Swept sine wave input signal
2 Output voltage

Input and output voltage signals in the time domain are used by Fansim for estimating the spectral transfer function. The results obtained using input and output records of figure A.3. are represented in figures A.4 and A.5.

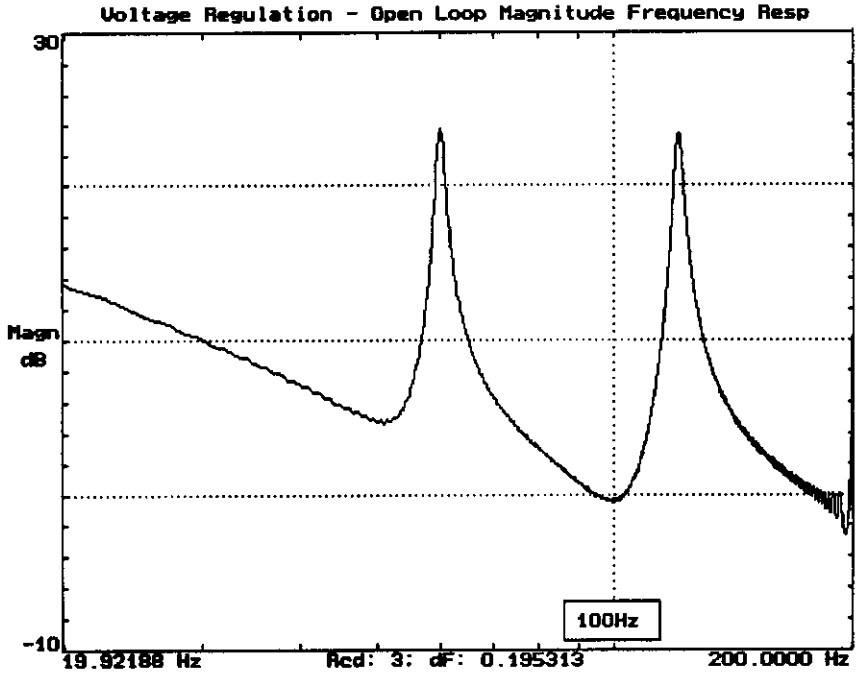

Figure A.4.

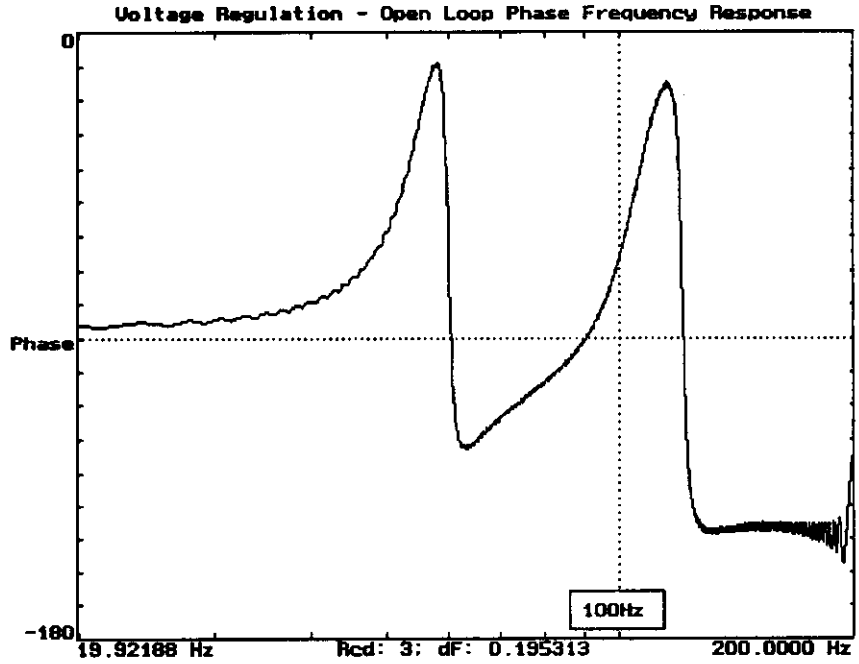

Figure A.5.

Similar results can be obtained by using a unitary impulse function instead of a swept sine wave signal. The open loop impulse response of the LEB voltage loop is shown in figure A.6.

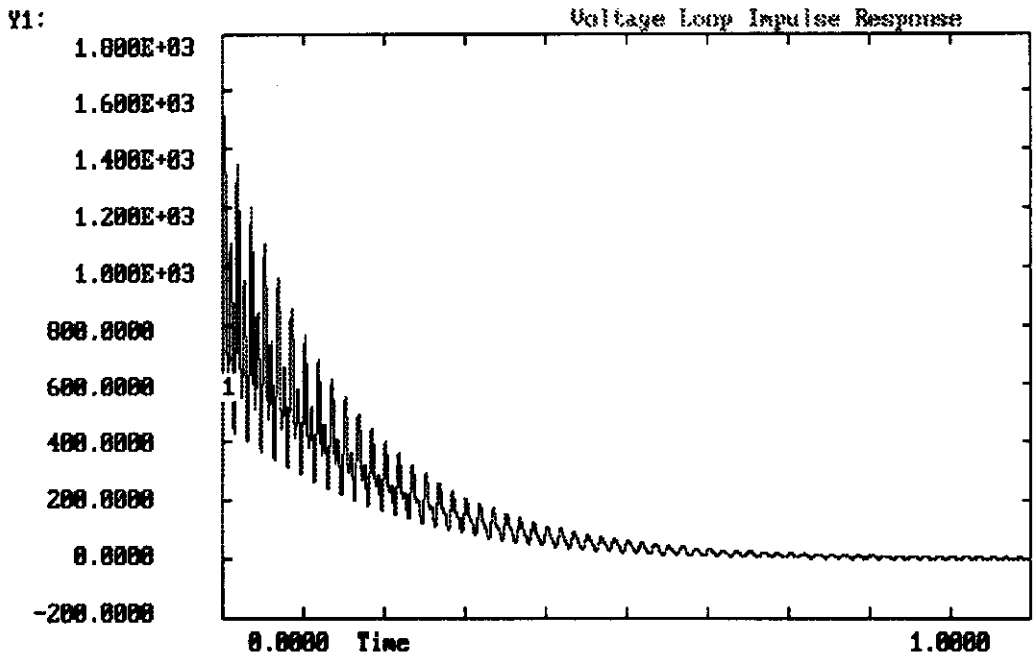

Figure A.6.

The frequency response of the voltage loop can be estimated by applying Fourier transform to the data of figure A.6. The resulting Bode phase diagram, obtained using Fansim, is shown in figure A.7.

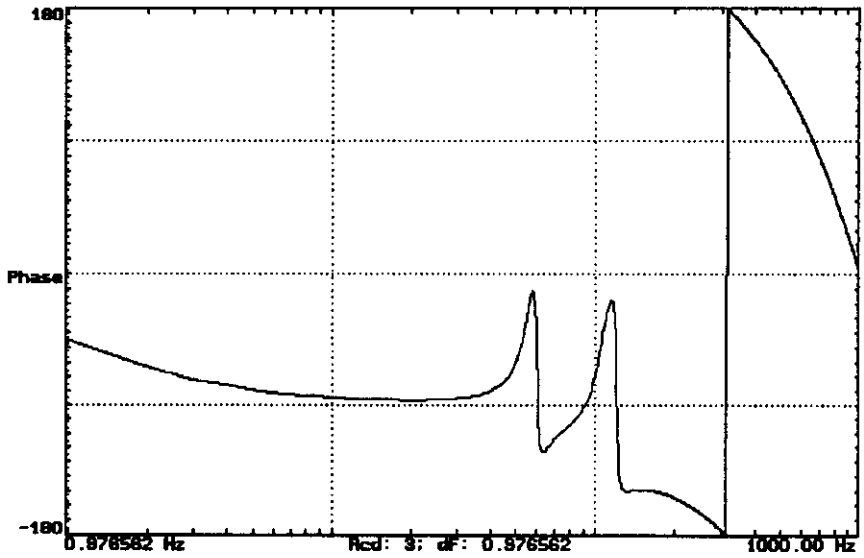

Figure A.7.

Closed Loop Analysis

The same procedure employed for open loop analysis has been applied to analyze the LEB voltage regulation system in closed loop operation. An unitary pulse input signal was applied to the voltage reference and the voltage waveforms at the power converter output and at the filter output have been registered. The results are shown in figure A.8.

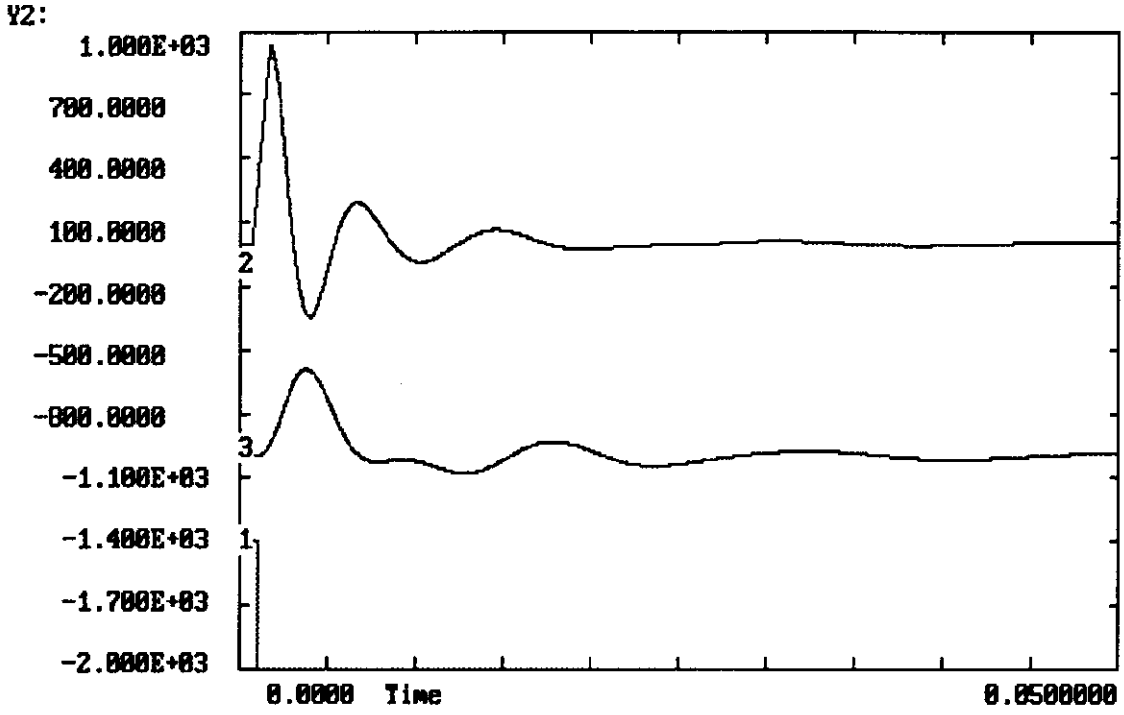

Figure A.8.
Tutsim Simulation of the Voltage Regulation in closed loop
1 pulse input signal
2 voltage waveform at the power converter output
3 voltage waveform at the filter output

The magnitude-frequency response to a reference signal of the LEB voltage regulator in closed loop operation is shown in figures A.9 and A.10. In figure A.9 the output is taken at the power converter while in figure A.10 the effect of the passive output filter is considered.

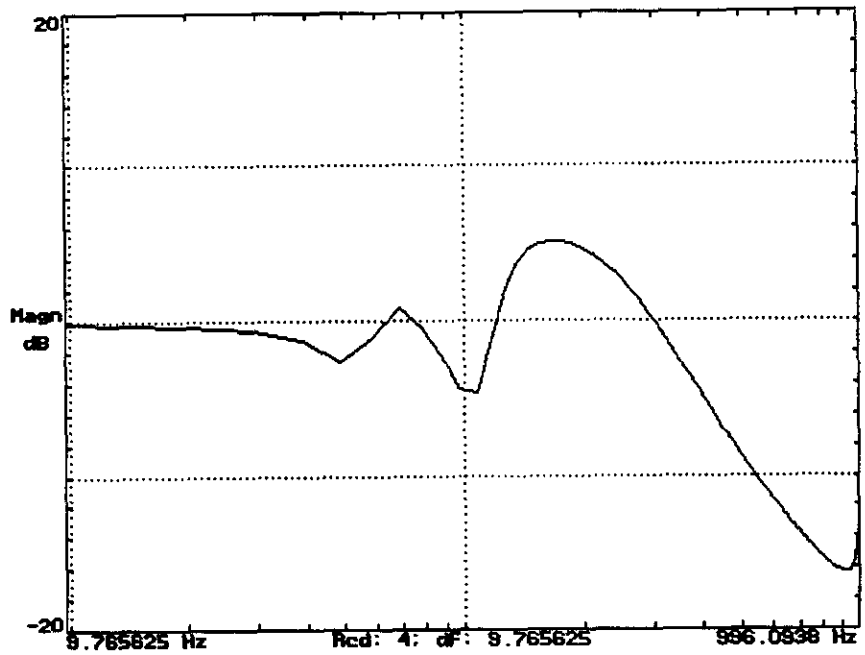

Figure A.9.
Voltage Loop Magnitude-Frequency response at the power converter output

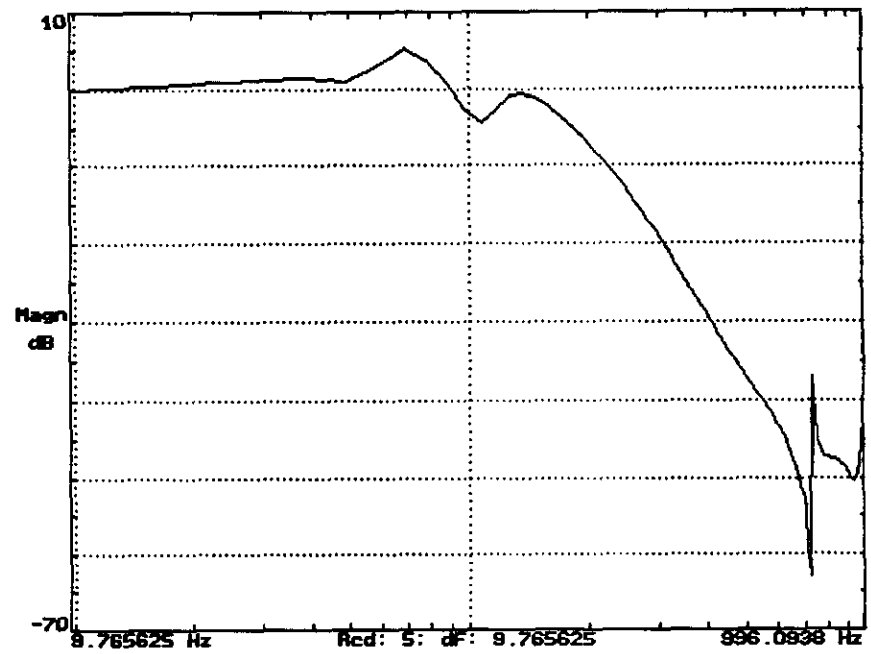

Figure A.10.
Voltage Loop Magnitude-Frequency response at the passive filter output

Ripple Rejection

Similar analysis has been made in order to determine ripple rejection characteristics of the voltage loop. Figure A.11. shows the time domain response to a voltage perturbation pulse.

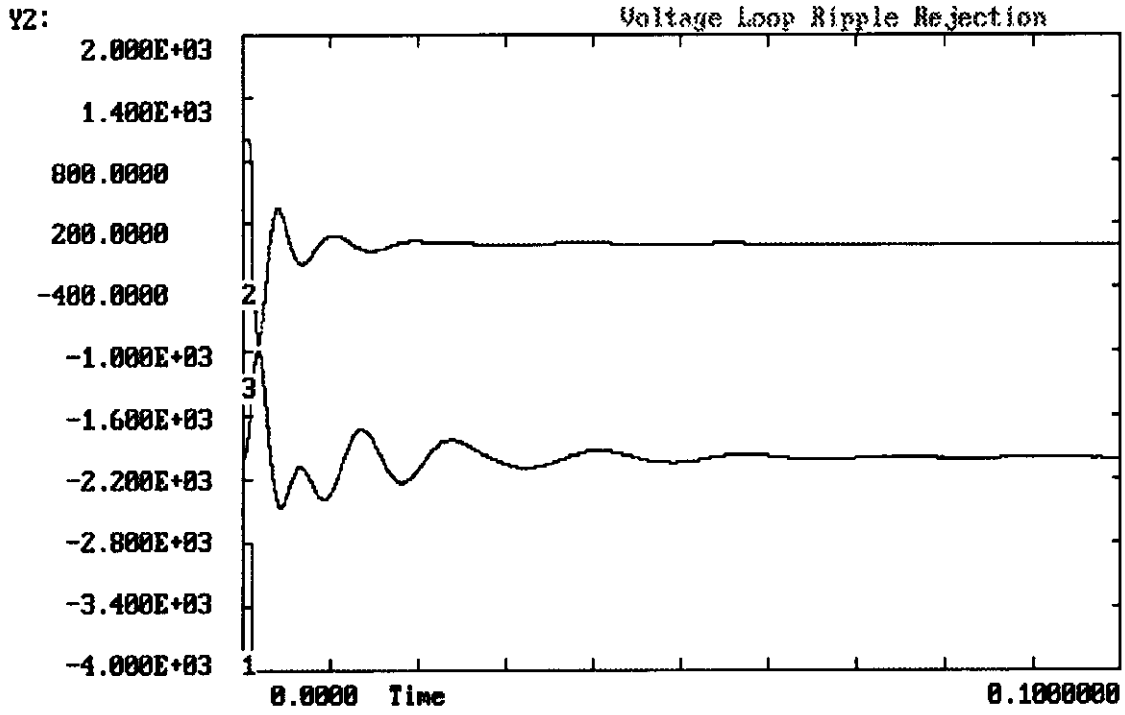

Figure A.11.
Ripple Rejection of the Voltage Regulation Loop
1 voltage perturbation pulse
2 voltage waveform at the power converter output
3 voltage waveform at the filter output

Figures A.12 and A.13 show ripple rejection characteristics at the filter output.

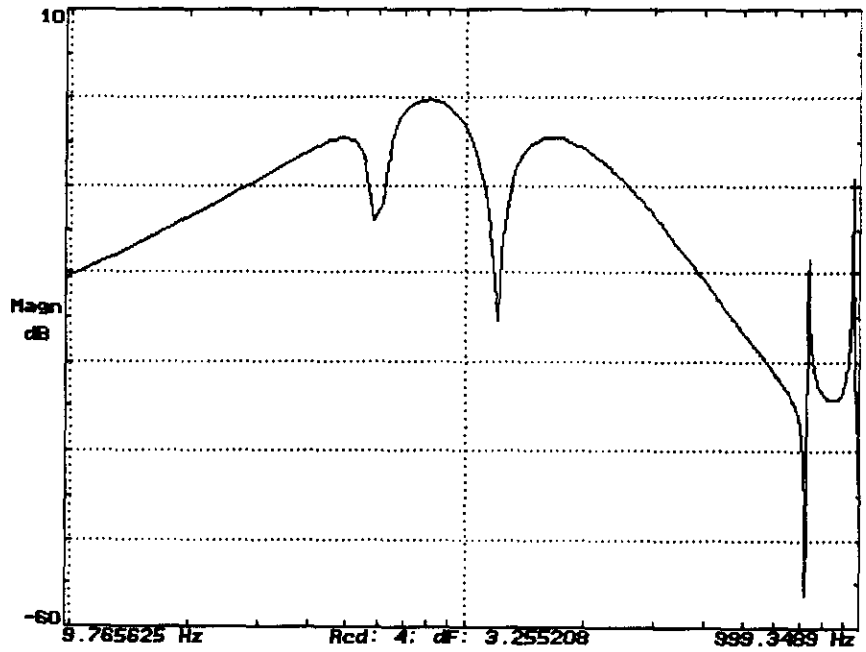

Figure A.12.
Response of the LEB Power Supply to a-c voltage perturbations

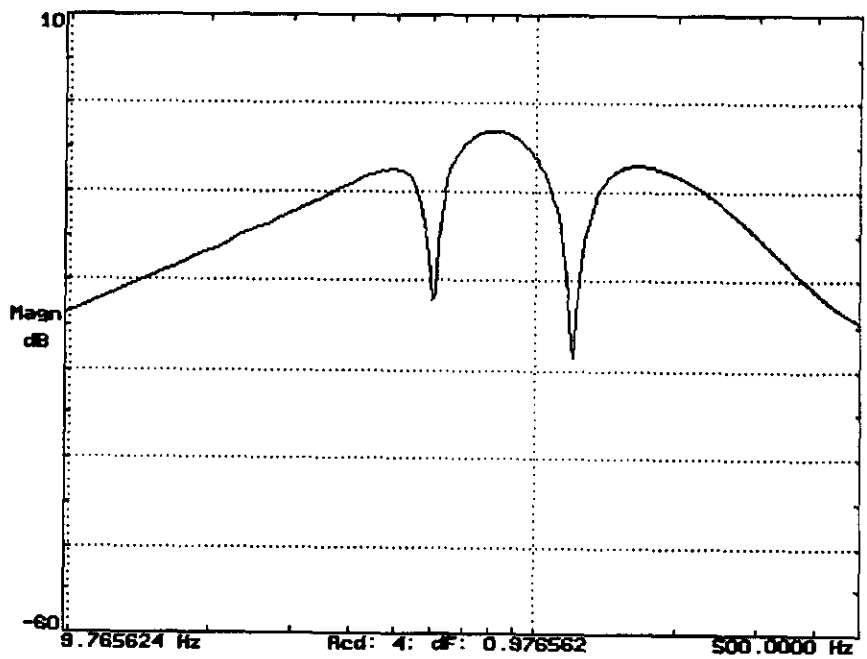

Figure A.13.
Response of the LEB Power Supply to a-c voltage perturbations

APPENDIX B

VOLTAGE LOOP SPICE SIMULATIONS

The voltage regulation loop of the LEB ring magnet power supply has been simulated using the program Spice. An schematic diagram of the voltage loop Spice simulation program is shown in figure B.1. The voltage compensator has been implemented using operational amplifiers (Subcircuit Opamp) in a parallel configuration in order to obtain the three terms of the corresponding transfer function. These three terms correspond to the subcircuits Compens, Bridg60 and Bridg120 respectively. The delay introduced by the power converter has been simulated by a single pole at 180Hz added to the subcircuit Addition.

The listing of the developed Spice program follows:

Spice Simulation Listing

```
Volta: Voltage Loop Simulation
*Compensator gain = 100
*Second Order Filters With Total Gain=0.25

.SUBCKT FILTER 3 8 5
L  3 5 .00196
C  5 8 1300UF
C1 5 6 4000UF
R1 6 8 1.41
C2 5 9 49UF
L2 9 10 .001
R2 10 8 .005
.ENDS FILTER

.SUBCKT OPAMP 1 2 3 4
RIN 1 2 100000
EOUT 3 4 2 1 100K
.ENDS OPAMP

.SUBCKT BRIDG60 1 8 5
*Double T Bridge Active Filter
*60 Hz 1% error in R3 and C3
*60 Hz gain = 0.5
RA 1 2 48.24K
R1 2 3 12.06K
R2 3 5 12.06K
R3 4 8 5.97K
C1 2 4 .220UF
C2 4 5 .220UF
C3 3 8 .445UF
X1 2 8 5 8 OPAMP
.ENDS BRIDG60
```

```
.SUBCKT BRIDG120 1 8 5
*Double T Bridge Active Filter
*120 Hz 1%error in R3 and C3
*120 Hz gain = 0.5
RA 1 2 24.12K
R1 2 3 6.03K
R2 3 5 6.03K
R3 4 8 2.985K
C1 2 4 .220UF
C2 4 5 .220UF
C3 3 8 .445UF
X1 2 8 5 8 OPAMP
.ENDS BRIDG120

.SUBCKT COMPENS 1 8 5
*GainDC=100 Pole at 1Hz
R1 1 2 10K
R2 2 5 1MEG
C1 2 5 .16UF
X1 2 8 5 8 OPAMP
.ENDS COMPENS

.SUBCKT ADDITION 1 2 3 8 6
*gain of 0.5 for both bridges
*gain of 1 for compens
*Pole at 180Hz, T=8.84 E-4
R1 1 5 10K
R2 2 5 20K
R3 3 5 20K
C4 5 6 .0884UF
R4 5 6 10K
X2 5 8 6 8 OPAMP
.ENDS ADDITION

*VIN 14 0 1 AC 1
VIN 10 0 AC 1
RIN10 10 0 10000
E1 11 0 10 13 1
XC   11 0 21 COMPENS
X60  11 0 22 BRIDG60
X120 11 0 23 BRIDG120
XAD 21 22 23 0 13 ADDITION
*E2 13 0 12 14 1
XF 13 0 1 FILTER
L1 1 2 .1
R1 2 0 .106
.AC DEC 100 10 1000
.END
```

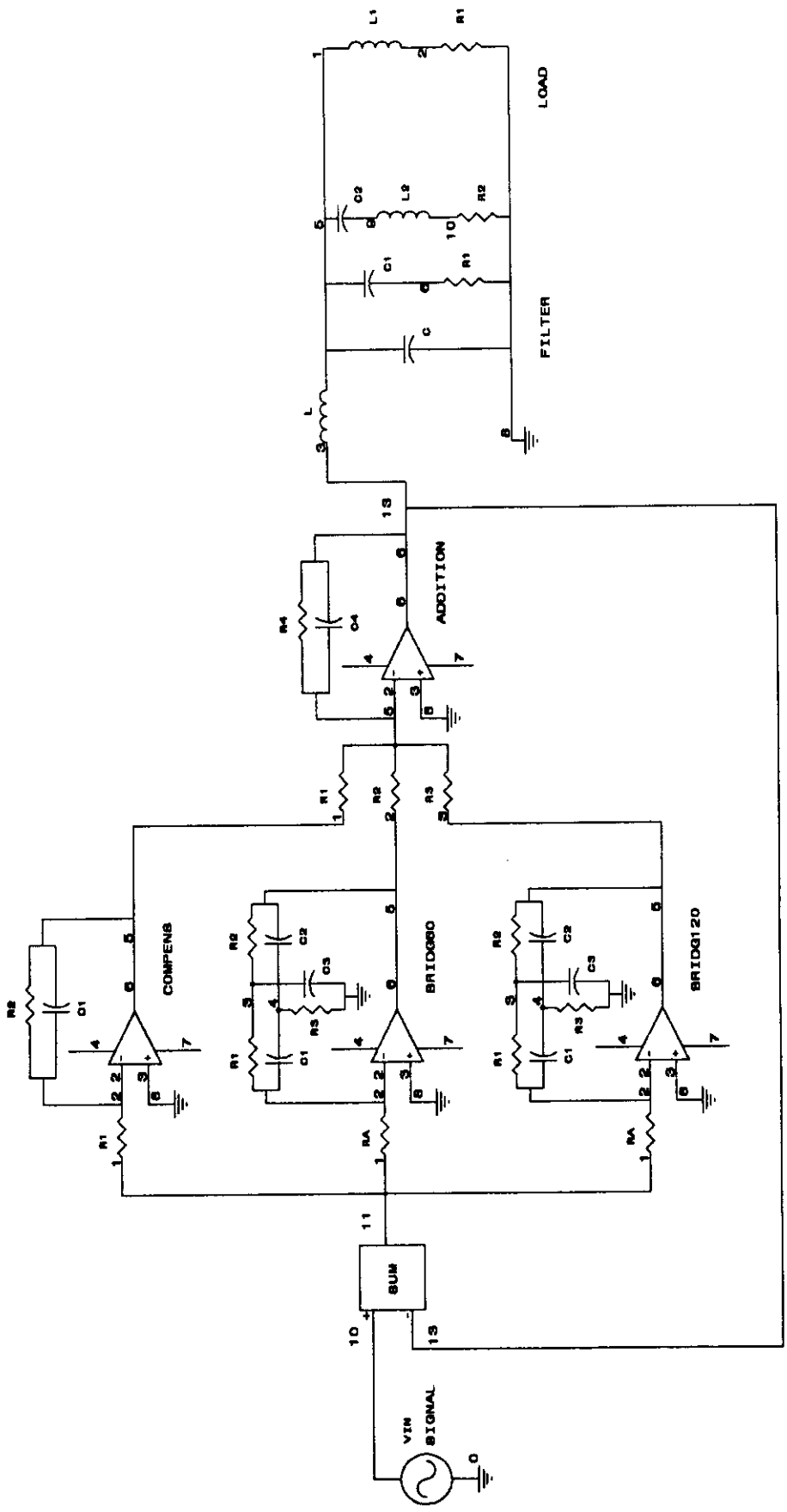

Figure B.1.
Schematic Diagram of the Voltage Loop Spice Simulation

Results and Discussion

The frequency response of the voltage loop obtained with the Spice simulations have been shown in figures I.6 and I.7. From figures I.6. a) and b) the stability margins can be determined. The phase margin is about 30° at a frequency of 140Hz. As at high frequencies the phase is tangent to -180° the gain margin goes to infinity. this is due to the fact that the converter delay has been simulated with a first order pole.

The results obtained in appendix A width Tutsim/Fansim simulations are basically the same at those obtained with Spice simulations. In fact phase margin and frequency (figures A.4 and A.5) are the same. Nevertheless, with Tutsim/Fansim simulations, the delay introduced by the power converter is well simulated and gain margin and frequency can be determined. From figure A.7. the gain margin obtained at a frequency of 300Hz has a value of about 10 dB. These two values are important; the frequency of 300Hz is the absolute maximum voltage loop bandwidth within stability conditions and 10 dB is the amount of gain loop increment that would just produce instability. Thus, maximum gain loop variations due to parameter changes and non-linear firing circuit behavior have to be carefully checked.

APPENDIX C

CURRENT LOOP, LINEAR RAMP MODE, COMPUTER SIMULATIONS

The current regulation loop of the LEB ring magnet power supply, under linear ramp operation mode, has been simulated using the program Spice. An schematic diagram of the current-loop linear ramp Spice simulation program is shown in figure C.1. The cascade current compensator has been implemented using operational amplifiers (Subcircuit Opamp) and the whole voltage loop was included inside the current loop. For details about the voltage loop, see Appendix B, Voltage Loop Spice Simulations.

The listing of the developed Spice program follows:

Spice Simulation Listing

```
LEBVOLR.CIR LINEAR RAMP CURRENT REGULATION
*Voltage rejection analysis
*Current loop simmulation, using a PI compensator
*Includes the voltage loop
.SUBCKT OPAMP 1 2 3 4
RIN 1 2 100000
EOUT 3 4 2 1 100000
.ENDS OPAMP

*---------------------------------------*
*VOLTAGE REGULATION LOOP
*Voltage Loop (volta.cir)
*Compensator gain = 100
*Second Order Filters with Total Gain=0.25

.SUBCKT FILTER 3 8 5
L  3 5 .00196
C  5 8 1300UF
C1 5 6 4000UF
R1 6 8 1.41
C2 5 9 49UF
L2 9 10 .001
R2 10 8 .005
.ENDS FILTER

.SUBCKT BRIDG60 1 8 5
*Double T Bridge Active Filter
*60 Hz 1%error in R3 and C3
RA 1 2 48.24K
R1 2 3 12.06K
R2 3 5 12.06K
```

```
R3 4 8 5.97K
C1 2 4 .220UF
C2 4 5 .220UF
C3 3 8 .445UF
X1 2 8 5 8 OPAMP
.ENDS BRIDG60

.SUBCKT BRIDG120 1 8 5
*Double T Bridge Active Filter
*120 Hz 1%error in R3 and C3
RA 1 2 24.12K
R1 2 3 6.03K
R2 3 5 6.03K
R3 4 8 2.985K
C1 2 4 .220UF
C2 4 5 .220UF
C3 3 8 .445UF
X1 2 8 5 8 OPAMP
.ENDS BRIDG120

.SUBCKT COMPENSV 1 8 5
*Compensator of the Voltage Loop
*Gain DC=100 Pole at 1Hz
R1 1 2 10K
R2 2 5 1MEG
C1 2 5 .16UF
X1 2 8 5 8 OPAMP
.ENDS COMPENSV

.SUBCKT ADDITION 1 2 3 8 6
*gain of 0.5 for both bridges
*gain of 1 for compens
*Pole at 180Hz, T=8.84 E-4
R1 1 5 10K
R2 2 5 20K
R3 3 5 20K
C4 5 6 .0884UF
R4 5 6 10K
X2 5 8 6 8 OPAMP
.ENDS ADDITION

.SUBCKT VOLTAGE 10 8 13
E1 11 8 10 13 1
XCV  11 8 21 COMPENSV
X60  11 8 22 BRIDG60
X120 11 8 23 BRIDG120
XAD 21 22 23 8 13 ADDITION
.ENDS VOLTAGE
*-----------------------------------*
```

```
.SUBCKT COMPENSI 1 9 6
*Compensator of the Current Loop
R1 1 2 10.8K
R2 3 4 100K
C  2 3 9.43UF
RB 2 4 11600K
X1 2 9 4 9 OPAMP
R3 4 5 10K
R4 5 6 10K
X2 5 9 6 9 OPAMP
.ENDS COMPENSI

* VIN 1 0 AC 1 PWL(0 375 .125 375 .475 3750 .625 3750 .975 375 1.2 375)
VIN 1 0 DC 1
RE1 1 0 1
E  2 0 1 11 1
RE3 2 0 1
XCI 2 0 3 COMPENSI
XV 3 0 4 VOLTAGE
XF 4 0 14 FILTER
VINR 13 0 AC .106
RE13 13 0 1
EF 5 0 14 13 1
L0 5 7 .1
R0 7 0 .106
ER 11 0 7 0 9.4339623
RE11 11 0 1
.OPTIONS LIMPTS=1000
.AC DEC 50 .001 1000
*.TRAN .03 1.2
.PROBE V(7) V(1) V(2) V(3) V(4) V(5) V(11) V(14) V(13)
.PROBE I(R0) I(RE1) I(RE3) I(RE11)
.END
```

Results

With a few modifications, the above Spice program has been used to simulate the LEB Linear Ramp current regulation system under open-loop and closed-loop operation (figures II 5, 6, 7, 10 and 11). It has been also used to determine the rejection characteristics of the current loop to voltage and current perturbations (figures II.8, 9, 12 and 13).

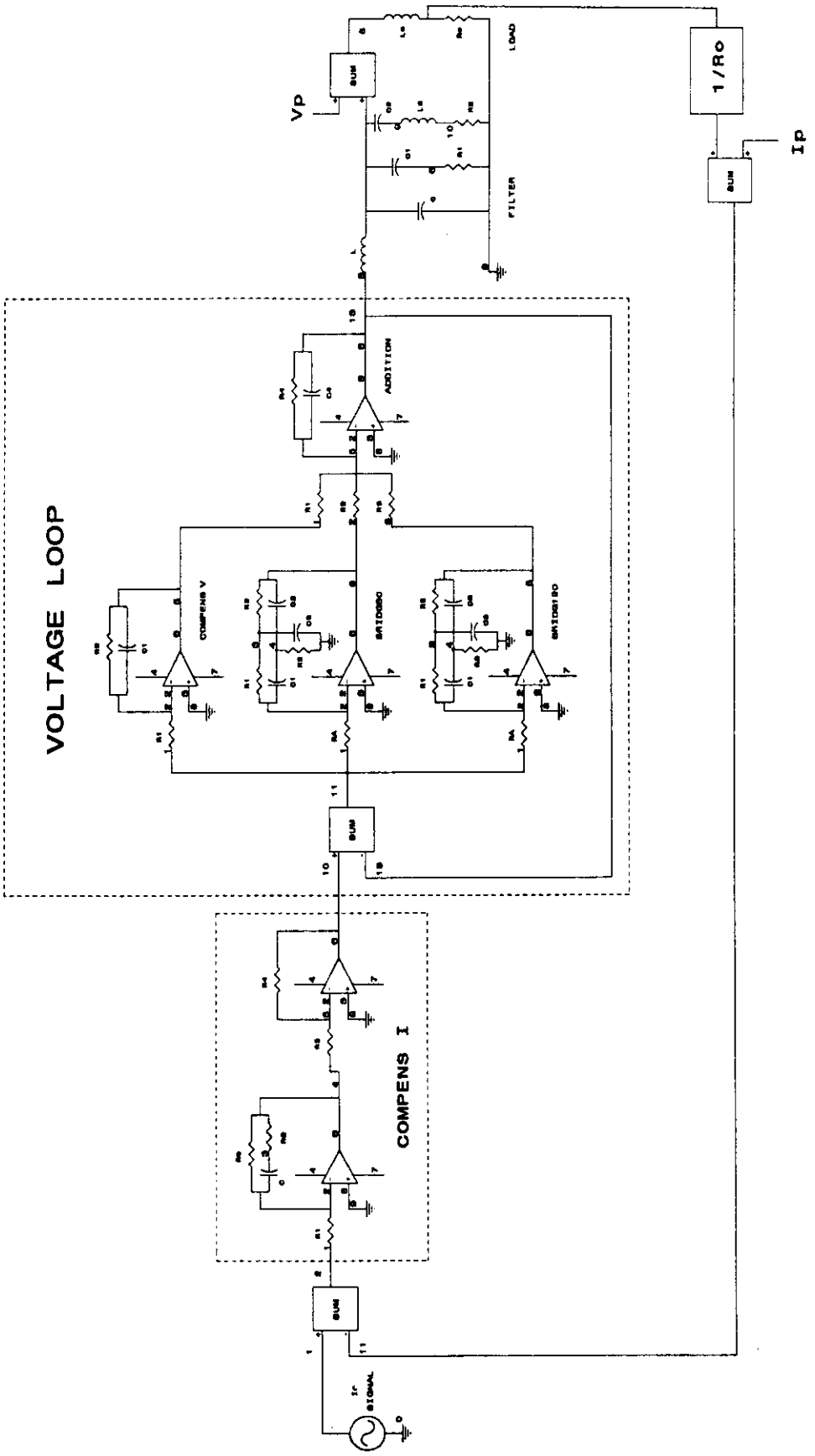

Figure C.1. Schematic Diagram of the Current Loop
Linear Ramp Operation Mode, Spice Simulation

APPENDIX D

CURRENT LOOP, SINE WAVE MODE, COMPUTER SIMULATIONS

I - TUTSIM SIMULATIONS

The L.E.B. 10 Hz Biased Sine Wave current regulation loop (fig. IV.3.) has been simulated using Tutsim and Spice. In Tutsim implementation, the transfer function of the different voltage loop blocks are simulated. The transfer function of both cascade compensators can be implemented following the procedure presented in appendix A or using the special Tutsim blocks as Iwz, Pid and Seo.

The Tutsim implementation is shown in figure D.1; where the cascade compensators were implemented using integrators and the multiplier and sample and hold using the corresponding blocks Mul and Spl. The only parameter of the sample-and-hold block is the sample interval corresponding to 10 Hz. Therefore, the two Spl (63 and 64) are simultaneous and in order to detect maximum and minimum current, an extra delay of half sample interval was introduced preceding the block Spl 64 (Del, 61). The electrical components of the output filter and load have been indicated in figure D.1. (42 to 54) but, Tutsim require block implementation for L, C, R and G components. For details about electric circuits implementation see Tutsim manual appendix C, Electric Circuits - Parts 1 and 2. The Tutsim model corresponding to figure D.1. follows.

Tutsim Simulation Listing

```
PROFESSIONAL VERSION OF TUTSIM

Model File: tutsim\leb10\dcloop.sim
Date:    11 /    19 /  1991
Time:    12 :    20
Timing:   0.0010000  ,DELTA  ;  11.0000     ,RANGE
PlotBlocks and Scales:
Format:
     BlockNo,  Plot-MINimum,  Plot-MAXimum;  Comment
Horz:     0 ,   1.0000     ,  11.0000     ; Time
  Y1:    30 ,   0.0000     ,   5.0000     ;
  Y2:   101 ,  -3.5000     ,   1.5000     ; d-c current deviation
  Y3:    18 ,  -1.0000     ,   4.0000     ; Output Current [KAmp]
  Y4:       ,              ,              ;


  10.0000          1 FRQ
   1.0000
   0.0010000       2 DEL      1
   0.0450000
   0.0000
                   3 MUL      2      62
   1.0000          4 GAI      3      58        ;Output Voltage [KVolt]
   1.0200          5 GAI      4      -6
```

```
   0.2815000        6 INT       5
   0.7000000        7 GAI       5
   1.4000           8 GAI       7       6
   0.0019800       11 L         8     -12
   0.3484000
   0.0013000       12 C        11     -14     -18
   0.2177000
   0.0040000       13 C        14
   0.2502000
   0.7090000       14 G        12     -13
   0.1000000       18 L        12     -22     -23  ;Output Current [KAmp]
                              -19
   0.3748000
   0.1320000       19 R        18
   0.2400000       20 R        21
   0.1600000       21 L        22      23     -20
   1.4965
   0.0041250       22 C        18     -21
   0.2207000
   0.0120000       23 R        18     -21
   1.0000          30 PLS
   5.0000
   1.0000
   1.7500          31 CON
                   32 SUM      30      31
   0.0010000       33 DEL      18
   0.0500000
   1.7500
   0.1000000       34 SPL      33              ;Maximum Value
   1.0000          35 GAI      32     -34
 312.500E-06       36 GAI      35     -37
 172.855E-06       37 INT      36
   1.2600          38 GAI      36
   1.300E+03       39 GAI      38      37
   1.0000          40 PLS
   5.0000
   1.0000
   0.3750000       41 CON
                   42 SUM      40      41
   0.1000000       44 SPL      18
   1.0000          45 GAI      42     -44
 312.500E-06       46 GAI      45     -47
  36.036E-06       47 INT      46
   1.2600          48 GAI      46
   1.300E+03       49 GAI      48      47
   1.0000          51 GAI      39      49
   0.7936500       55 GAI      51     -56
   0.2715000       56 INT      55
   0.9800000       57 GAI      55
   1.0400          58 GAI      56      57
   1.0000          61 GAI      39     -49
   1.0000          62 GAI      61
   0.5000000      101 GAI      34     -31      44  ;d-c current deviation
                              -41
   0.5000000      102 GAI      34     -31     -44  ;a-c current deviation
                               41
```

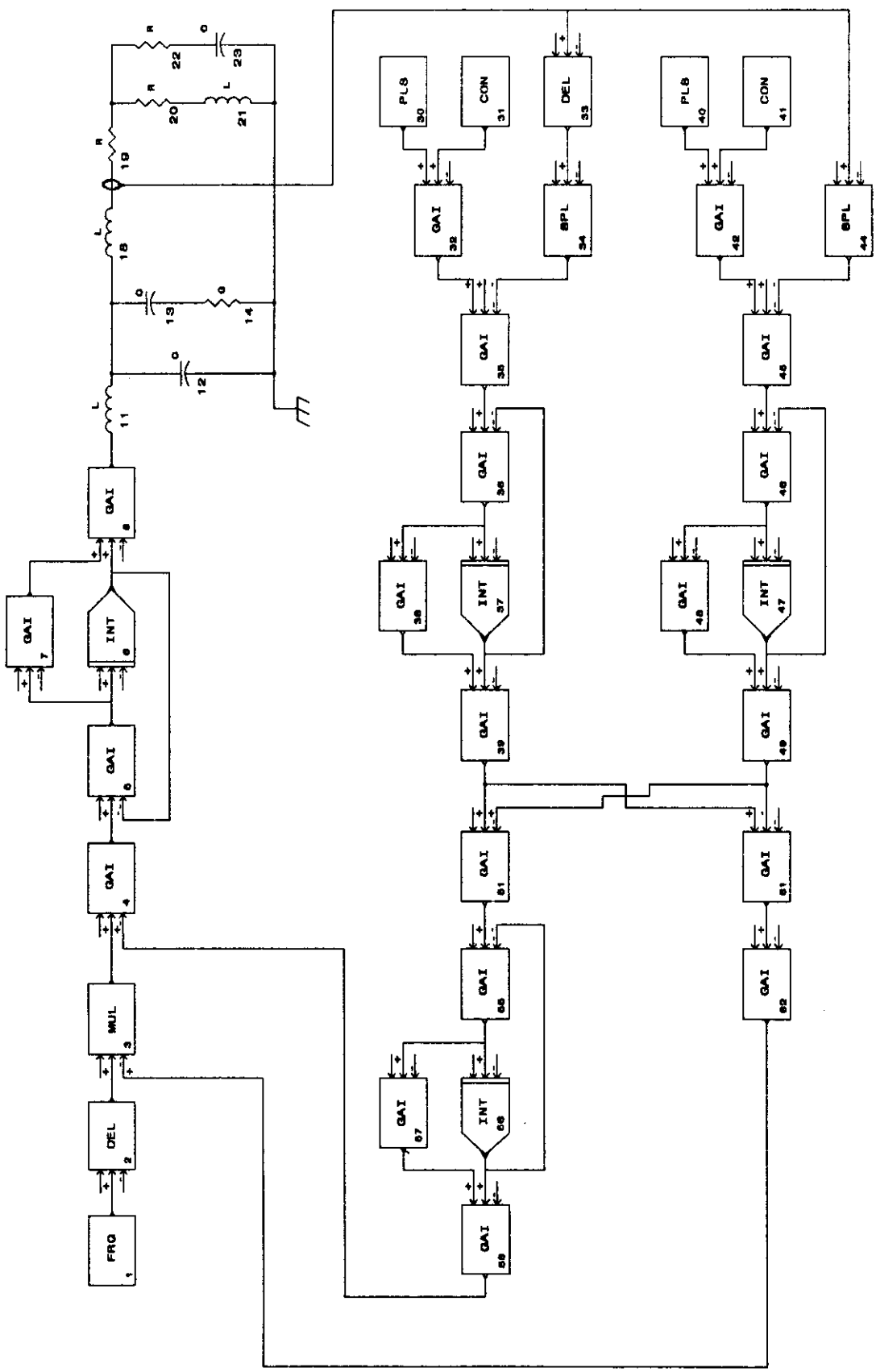

Figure D.1.
L.E.B. 10 Hz Biased Sine Wave Current Loop - Tutsim Implementation

Open loop analysis

The transfer function determination of d-c and a-c load behavior under open loop operation is important in order to validate the lower order mathematical expressions theoretically deduced for both current loops (expressions 26 and 38).

The open loop transient behavior of the LEB current regulator can be performed by opening both feedback loops in figure D.1. The usual sources employed are impulse, step and sine wave or frequency modulated sine wave. A sine wave signal width frequency linearly swept from 0.02Hz to 1Hz in 50 sec. has been considered.

a) d-c Current Loop

The sine-wave frequency-modulated signal has been added to the mean value input signal. The resulting time-domain analysis is shown in figure D.2 and the corresponding Bode diagrams estimated with Fansim are shown in figure D-3.

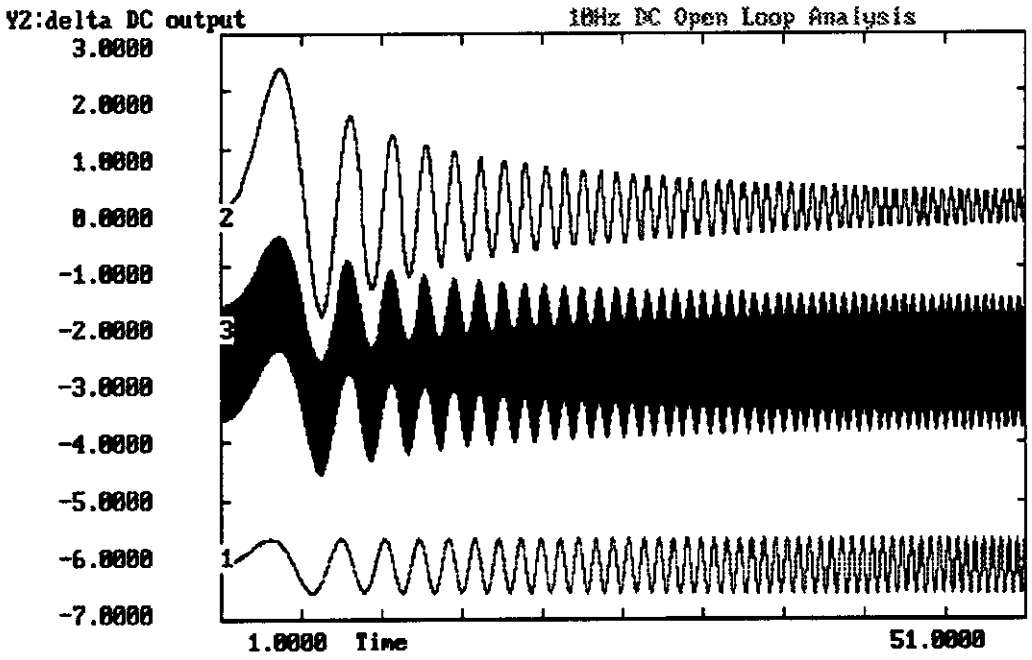

Figure D.2. Open-loop time-domain analysis of the d-c mean-value current regulation
1. Sine-wave frequency-modulated signal
2. Deviation of the current-output mean value
3. Output current

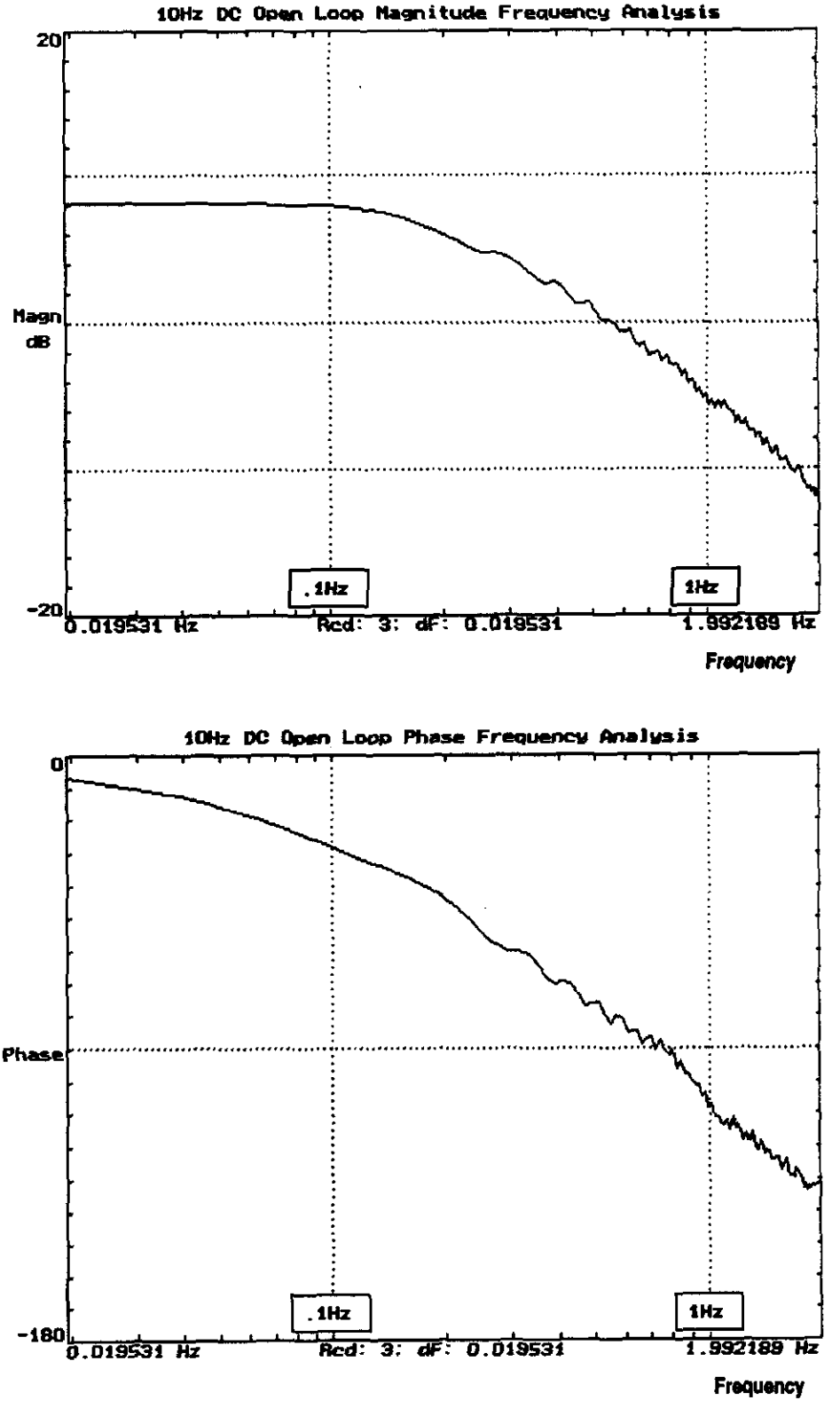

Figure D.3. Open-loop Bode diagrams of the d-c mean-value current loop

From the Bode diagrams of figure D.3, load admittance parameters can be directly estimated. Other possibility is to use the iterative least-squares curve fitting capabilities of Fansim program. The obtained coefficients reasonable agree with the load admittance lower order approximation of equation 26.

b) a-c Current Loop

The same sine-wave frequency-modulated signal has been also used to modulate the 10 Hz a-c current amplitude. The resulting time-domain analysis is shown in figure D.4 and the corresponding Bode diagrams estimated with Fansim are shown in figure D-5.

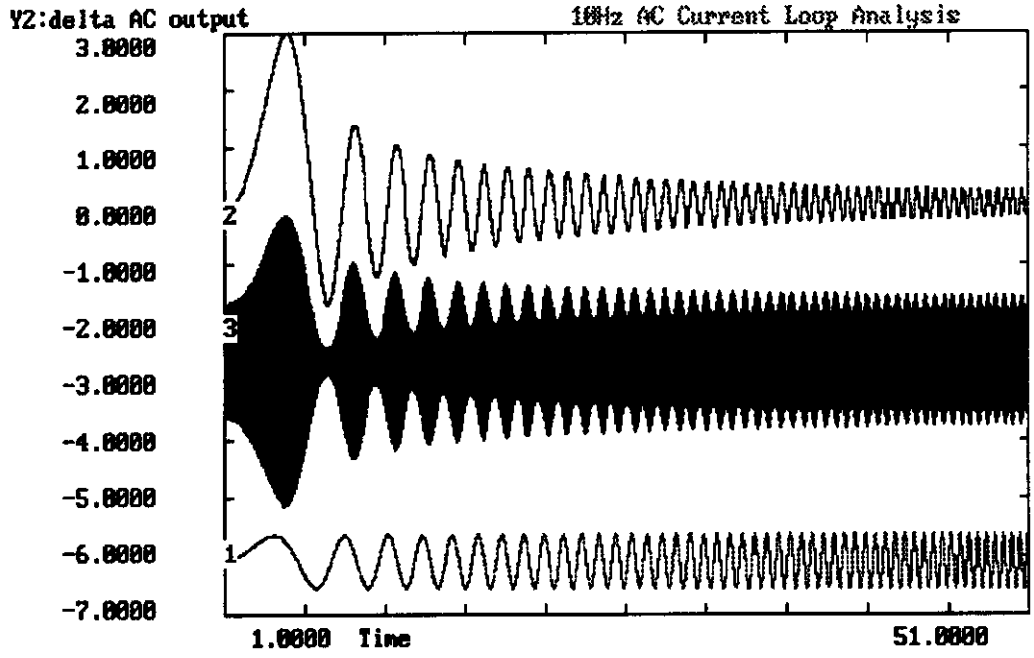

Figure D.4. Open-loop time-domain analysis
of the a-c amplitude current regulation
1. Sine-wave frequency-modulated signal
2. Deviation of the a-c current amplitude
3. Output current

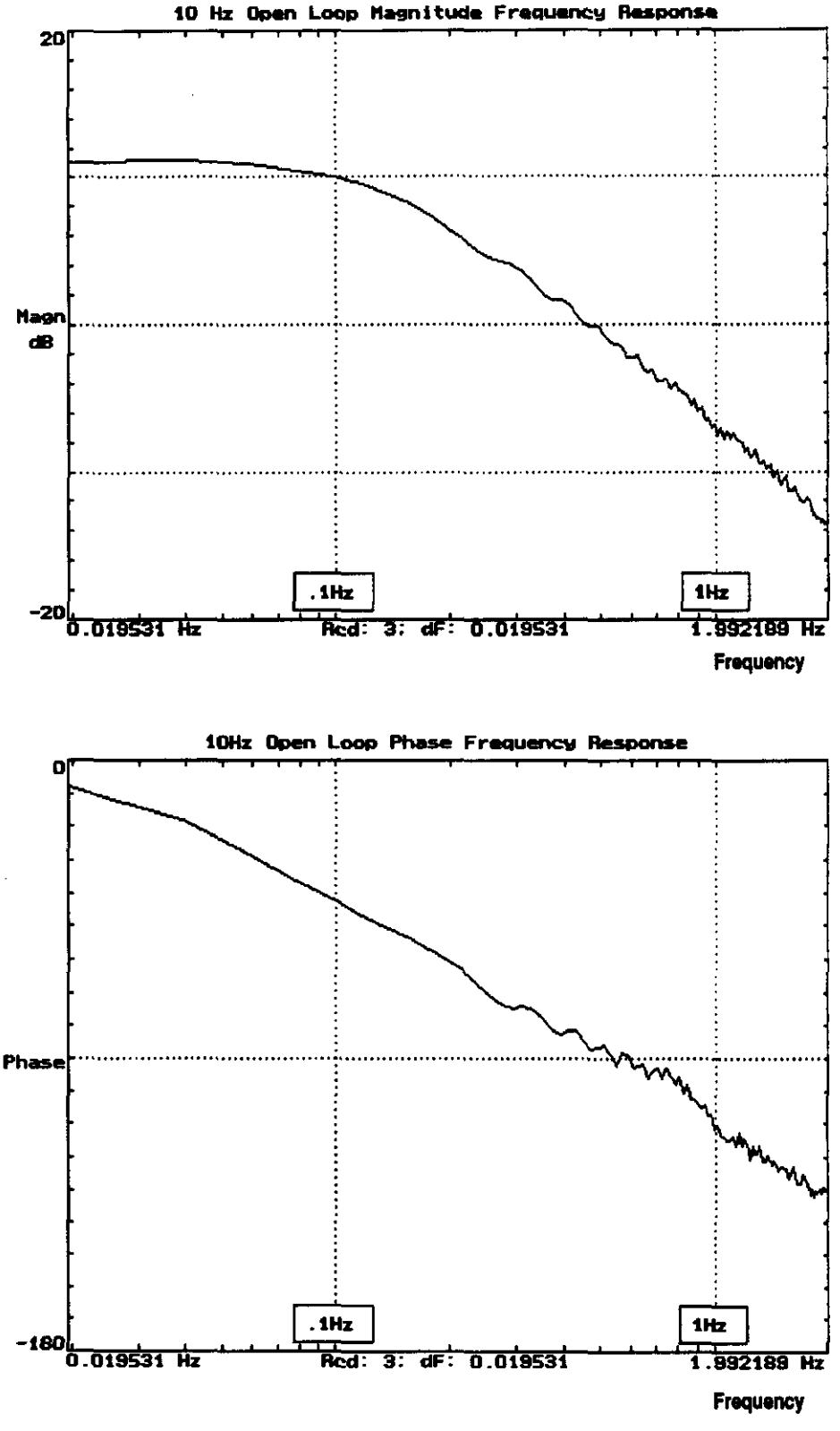

Figure D.5. Open-loop Bode diagrams of the a-c amplitude current loop

The transfer function between multiplier input and detector output, including the nonlinear operations of amplitude modulation and peak detection, can be estimated from the Bode diagrams of figure D.5. Using the Fansim iterative least-squares curve fitting routine, the following estimated transfer function has been obtained.

$$T(s) = \frac{3.8}{1 + s\,1.25}$$

This expression reasonable matches the theoretical result obtained applying convolution theorems in the s-plane domain (equation 28). The difference in gain of a factor 2 is due to the fact that in Tutsim\Fansim simulations the output current peak has been detected while in the deduction of equation 38 a synchronous detector has been considered.

Closed loop analysis

The closed loop operation of the 10 Hz biased current regulation system has been simulated using the diagram implementation shown in figure D.1. The transient behavior of the d-c loop is analyzed by adding a same rectangular pulse to both continuous current references. The d-c current output is calculated by adding maximum and minimum current measurements and dividing by two. The time response of the d-c current loop is shown in figure D.6.

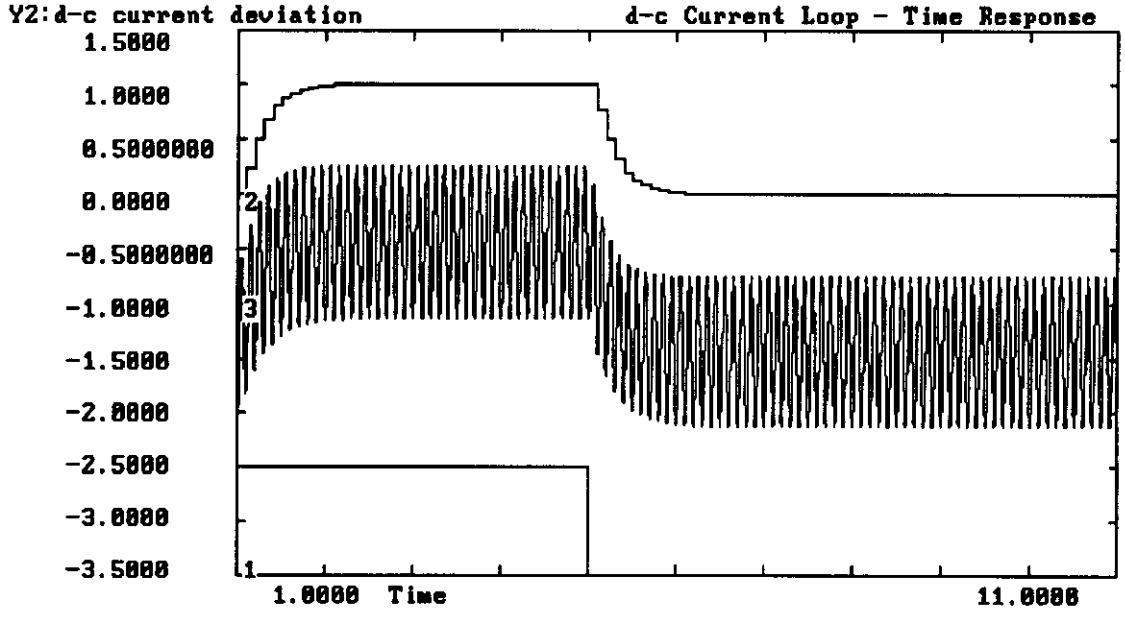

Figure D.6. Time response of the d-c current regulation loop
1. Rectangular pulse added to current references
2. Deviation of the d-c current output
3. Output current

The frequency response of the d-c current loop can be estimated by processing with Fansim the time-domain data of figure D.6. The obtained magnitude and phase Bode diagrams have been shown in figure IV.10.

The a-c magnitude current loop is analyzed in a similar way adding rectangular pulses with opposite polarities to both continuous current references. The time-domain simulation results is shown in figure D.7.

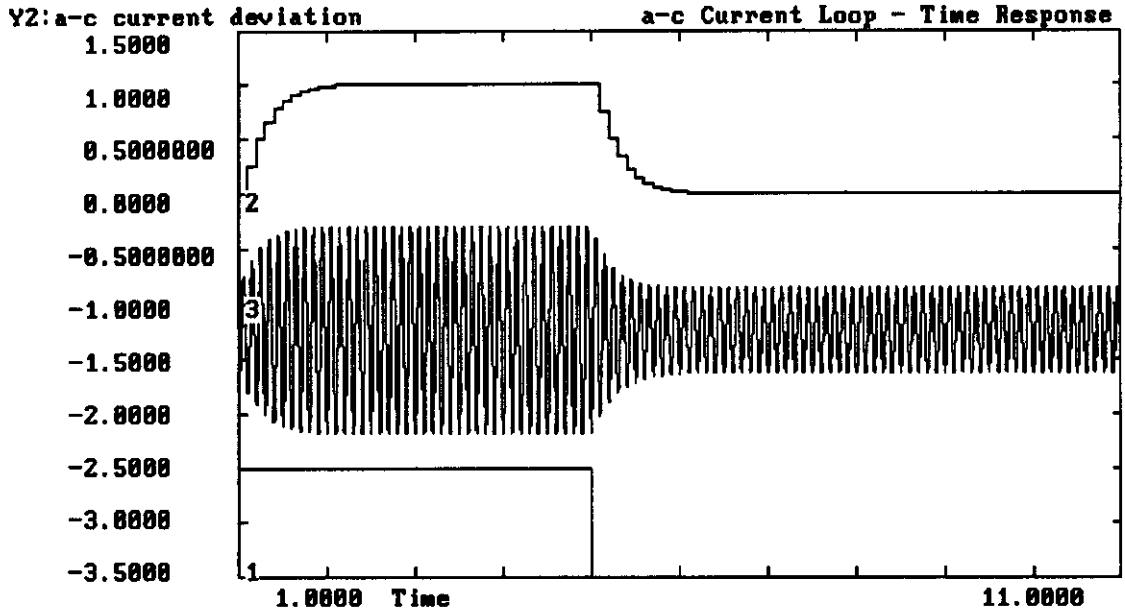

Figure D.7. Time response of the a-c current regulation loop
1. Rectangular pulse added and subtracted to current references
2. Deviation of the a-c current output
3. Output current

The corresponding frequency response of the a-c current loop as estimated by Fansim has been shown in figure IV.12.

II - SPICE SIMULATIONS

The current regulation loop of the LEB ring magnet power supply, under sine wave operation mode, has been also simulated using the program Spice. An schematic diagram of the current-loop sine wave Spice simulation program is shown in figure D.8.

Both cascade current compensators have been implemented using operational amplifiers and the sample-and-hold circuit using switches followed by a capacitor. The switches S1 and S2 are driven by the sample pulses Pls 21 and Pls 22 synchronized with the time corresponding to maximum and minimum output current respectively. The switches S3 and S4 driven by Pls 22 have been added in order to measure simultaneously the errors in maximum and minimum current and reducing the interdependence between d-c and a-c current loops.

The listing of the developed Spice program follows:

Spice Simulation Listing

```
10 Hz Current Closed Loop Simmulation
*With compensator and filter

* Second Order Filter
.SUBCKT FILTER 3 8 5 18
LA 3 5 .0005
LB 8 18 .0005
K1 LA LB .98
C  5 8 1300UF
C1 5 6 4000UF
R1 6 8 1.41
C2 5 9 49UF
L2 9 10 .093
R2 10 8 .005
.ENDS FILTER

.SUBCKT OPAMP 1 2 3 4
RIN 1 2 100MEG
EOUT 3 4 2 1 100K
.ENDS OPAMP

.SUBCKT COMPG 1 8 6
*Gain(1300), Zero at 1.26 Pole at 3200
R1 1 2 246K
RC 3 4 126K
C1 2 3 10UF IC=.01V
R2 2 4 320MEG
X1 2 8 4 8 OPAMP
R3 4 5 10K
R4 5 6 10K
X2 5 8 6 8 OPAMP
.ENDS COMPG
```

```
.SUBCKT COMPDC 1 8 4
*Gain(1.04), Zero at .977, Pole at 1.26
R1 1 2 26.9K
RC 3 4 98K
C1 2 3 10UF IC=.01V
R2 2 4 28K
X1 2 8 4 8 OPAMP
.ENDS COMPDC

.SUBCKT COMPA 1 8 6
*Gain(1.4), Zero at .7, Pole at .98
R1 1 2 20K
RC 3 4 70K
C1 2 3 10UF IC=.01V
R2 2 4 28K
X1 2 8 4 8 OPAMP
R3 4 5 10K
R4 5 6 10K
X2 5 8 6 8 OPAMP
.ENDS COMPA

VIN 20 0 0 SIN(0 1 10 0)
VP1 21 0 0 PULSE(-.5 1 27.0MS .01MS .01MS .01MS 100MS)
VP2 22 0 0 PULSE(-.5 1 77.0MS .01MS .01MS .01MS 100MS)
VP3 23 0 0 PULSE(-.5 1 2.0MS .01MS .01MS .01MS 100MS)
VMAX 8 0 DC 3750
VMIN 9 0 DC 375
*V14 14 0 DC 20
B1 16 0 V=v(14)*v(20)
*Both loops connected
E4 18 28 16 15 1
XF 18 28 51 0 FILTER
XCA 51 0 1 COMPA
L1 1 2 .1
R1 2 3 .132
RL 3 4 .240
L  4 0 .160
C  3 44 4125UF
R2 44 0 .012
E1 5 0 2 3 7.576
RLL 5 0 100K
S1 5 6 21 0 SMOD
CA 6 0 1UF IC=.01V
RA 6 0 10000MEG
S2 5 7 22 0 SMOD
CB 7 0 1UF IC=-.01V
RB 7 0 10000MEG
E2 30 0 8 6 1
E3 32 0 9 7 1
S3 30 31 23 0 SMOD
CC 31 0 1UF IC=-.01V
RC 31 0 10000MEG
S4 32 33 23 0 SMOD
CD 33 0 1UF IC=-.01V
```

```
RD 33 0 10000MEG
ESM1 60 0 31 0 1
ESM2 61 0 33 0 1
XCG1 60 0 10 COMPG
XCG2 61 0 11 COMPG
EMAX 14 0 10 11 1
EMI1 17 0 0 11 1
EMI2 13 0 10 17 1
XC2  13 0 15 COMPDC
R15  15 0 100K
*E14 14 0 12 0 .24
*R30 30 0 1K
.TRAN .05 5 0 .003 UIC
.END

.MODEL SMOD SW
```

Results

The above Spice program has been used to analyze the transient behavior of the LEB 10 Hz Sine Wave current regulation system. The stationary state and the transient behavior of output voltage and magnet current have been shown in figures IV.14, 15 and 16.

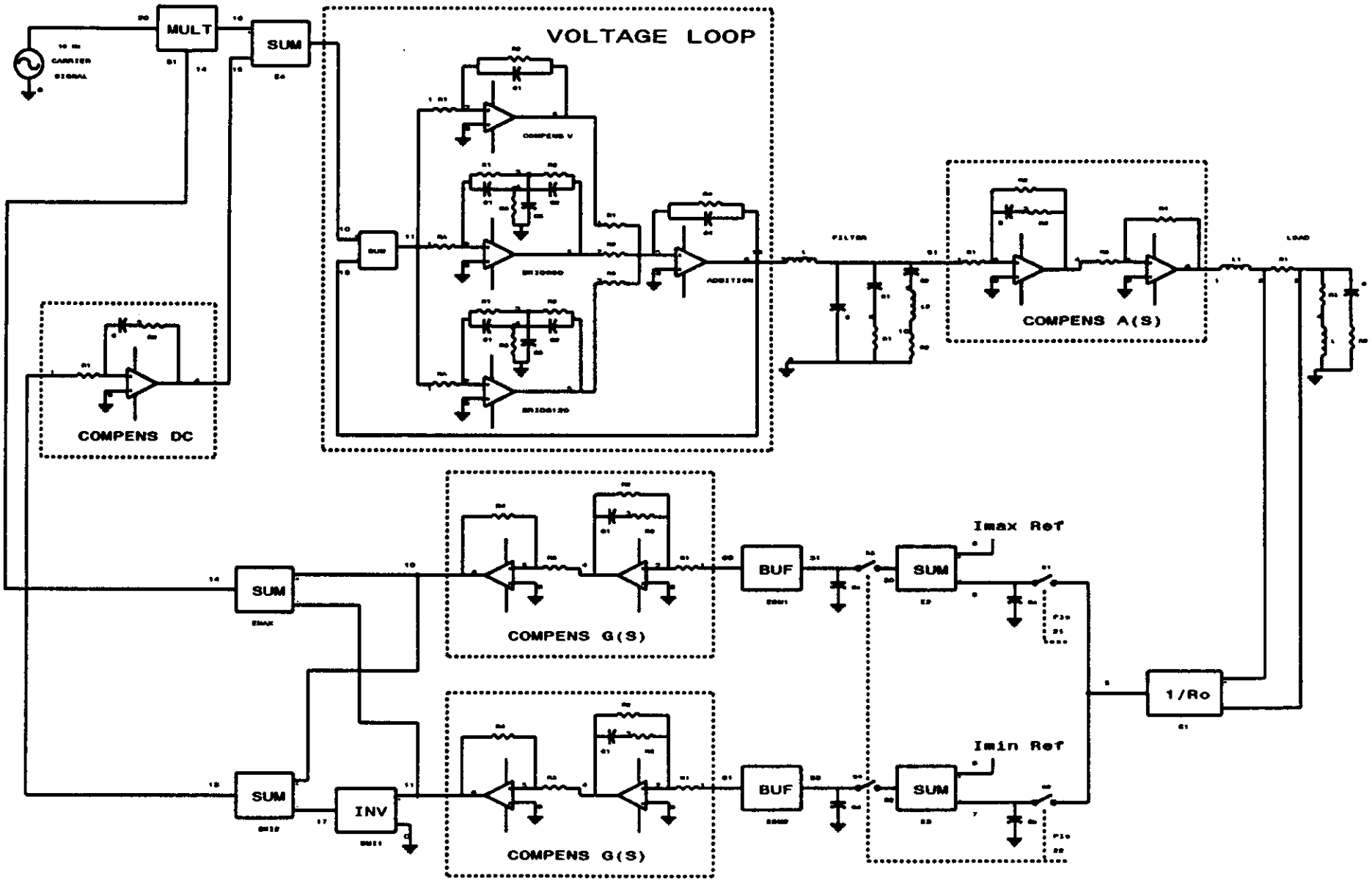

Figure D.8. Schematic Diagram of the Current Loop
10 Hz Sine Wave Operation Mode, Spice Simulation

LEB RING MAGNET POWER SUPPLY SYSTEM

VOLTAGE AND CURRENT REGULATION DESIGN

Eugenio J. Tacconi

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