Published by IOP Publishing for Sissa Medialab

Received: *November 1, 2024*
Revised: *January 14, 2025*
Accepted: *March 5, 2025*
Published: *March 27, 2025*

Topical Workshop on Electronics for Particle Physics
University of Glasgow, Scotland, U.K.
30 September–4 October 2024

A novel feedback circuit for analogue time walk compensation

J. Hammerich,* **S. Powell, E. Vilella, B. Wade and C. Zhang**

Department of Physics, University of Liverpool,
Oliver Lodge Building, Oxford Street, Liverpool L69 7ZE, U.K.

E-mail: jhammerich@hep.ph.liv.ac.uk

Abstract: Ever more precise time information is required to separate independent events at planned and proposed particle physics experiments. Typically, a combination of internal gain, very fast amplifiers and complex sampling circuitry are used to achieve this high time resolution, which usually come at the price of additional power consumption, layout area and complexity. In this contribution a novel circuit to improve the time resolution of a Depleted Monolithic Active Pixel Sensor (DMAPS) is presented. Its amplifier feedback is designed such that within its dynamic range the time walk of the trailing edge of the amplifier is compensated, making it the better estimate of the time of arrival (ToA). At moderate layout cost, this circuit allows reduce the power consumption of the analogue front end and enables a simple time walk correction which can be implemented on the ASIC.

Keywords: Analogue electronic circuits; Electronic detector readout concepts (solid-state); Particle tracking detectors (Solid-state detectors); Timing detectors

*Corresponding author.

https://doi.org/10.1088/1748-0221/20/03/C03052

2025 JINST 20 C03052

Contents

1 Introduction

As particle physics experiments aim for higher event and particle rates, detectors need to be able to resolve the tracks of these particles not only in space but also in time. For example, in collider experiments like ATLAS or CMS at the LHC each hit in every tracking detector needs to be assigned to the correct bunch crossing to prevent collisions of consecutive bunch crossings from overlapping. At the High-Luminosity LHC (HL-LHC) the number of collisions per bunch crossing will be so large that a much more precise time information is required to resolve the individual interactions which is referred to as 4D tracking [1, 2]. Improving the time resolution of a silicon sensor comes usually at the price of higher power consumption of the analogue frontend but generally also requires more sophisticated circuitry to sample the timestamp of a hit. These drawbacks are more severe for monolithic pixel sensors compared to hybrid pixels as they cannot use the full pixel area for logic, which would also add parasitic capacitance, or share logic among neighbouring pixels. As the readout is integrated into the same die of silicon which acts as sensitive element, monolithic pixels cannot transition easily to smaller process nodes. In recent years many approaches have been developed to improve the timing performance of monolithic pixel sensors. Some projects make use of bipolar transistors with very high maximum frequencies [3] or add an additional gain layer to the substrate [4] to improve analogue performance. Other developments focus on sampling circuits to achieve a precise enough time binning [5–8]. One of the fundamental limitations of the time resolution of analogue frontends is time walk. Larger signal charge induces a larger pulse in the amplifier causing the comparator to cross its threshold earlier than smaller charges and smaller pulses. In the following a novel approach for analogue time walk compensation in an analogue frontend of a DMAPS sensor is presented.

2 Concept

The working principle of the compensating feedback circuit is inspired by the analogue frontend of the switched-reset pixel in RD50-MPW2 [9], a DMAPS prototype developed in the LFoundry 150 nm process, shown in figure 1. The sensitive element is a reversed biased diode formed by a deep n-well in a p-substrate. An amplifier to which the signal is AC-coupled is placed in shallow wells within the deep n-well. A constant feedback current source (I_FB_Const) ensures that the amplifier is restored to its nominal working point after a pulse has been generated. The amplifier output is then digitised by a comparator. This topology is common for many large fill-factor DMAPS [10, 11]. In the switched-reset pixel an additional feedback source (I_FB_SWITCHED) is added which is triggered

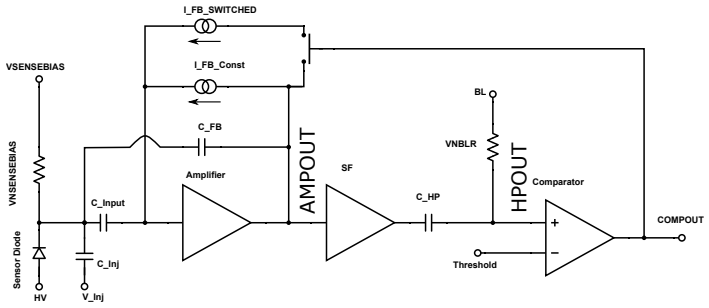

Figure 1. Schematic sketch of the switched-reset pixel of RD50-MPW2 (adapted from [9]). Charge is collected by a reverse biased diode and then AC-coupled into a charge sensitive amplifier. The amplifier output is fed into a comparator, which discriminates the signal, by a high-pass filter (HP). The HP reduces the impact of low frequency noise and allows the setting of the baseline (BL), the DC working point of the comparator independently of the amplifier. Besides a constant feedback current source (I_FB_Const) an additional feedback source (I_FB_SWITCHED) is added to the circuit. This switched feedback source is triggered by the comparator output to quickly restore the amplifier to its nominal working point after a hit has been registered, reducing the analogue dead time. Reproduced with permission from [9].

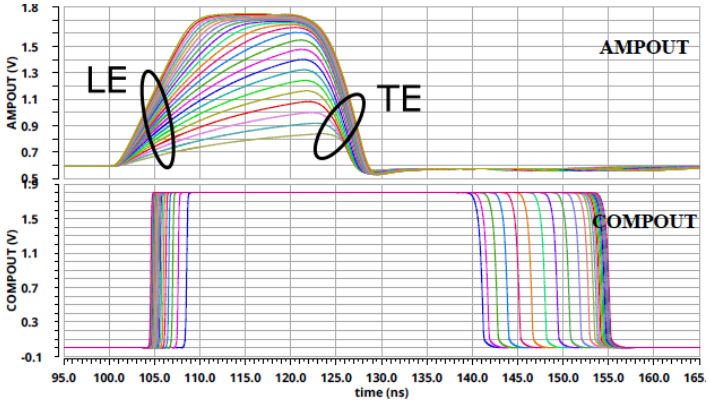

Figure 2. Analogue transient simulations of the amplifier (AMPOUT) and comparator (COMPOUT) response of the switched-reset pixel of RD50-MPW2 (annotated from [9]) for an input range of 3k electrons to 25k electrons. Leading Edge (LE) and Trailing Edge (TE) of the amplifier pulse are annotated. Due its intrinsic delays, the comparator switching occurs later than the threshold crossing of the input waveform. The comparator for RD50-MPW2 was optimised for the LE which causes a larger delay for the TE. Reproduced with permission from [9].

by the comparator output. The aim of this feedback is to significantly speed up the restoration of the amplifier to its working point after a hit has been successfully registered by the comparator as shown in figure 2. A side effect of the switched-reset is highlighted in figure 2: the difference in transient response of the amplifier in the Leading Edge (LE) is much more pronounced than in the Trailing Edge (TE) such that the time information of the TE should be less affected by time walk than that of the LE. However, the rest of the analogue frontend is not optimised to reflect this effect in the comparator response. Thus the compensating feedback pixel [12] was designed with the aim of implementing a feedback circuit so that timing of the TE of the amplifier response is time walk compensated. The schematic of the compensating feedback pixel, which has been implemented in a successor of RD50-MPW2 called UKRI-MPW0 [13] also produced in the LFoundry 150 nm process, is presented in figure 3. Here, the switched feedback source is replaced by a new current source which

2025 JINST 20 C03052

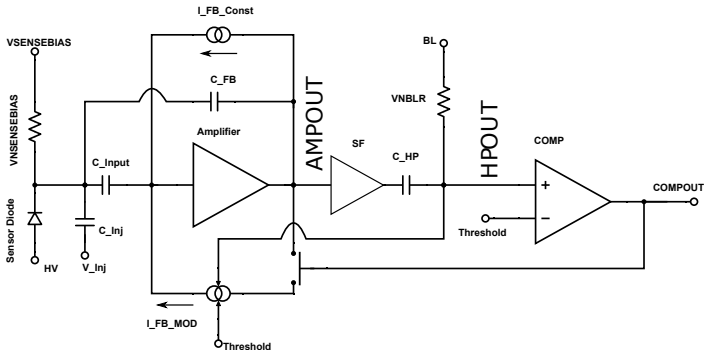

Figure 3. Schematic sketch of the compensating feedback pixel implemented in UKRI-MPW0. The additional switched feedback current source of figure 1 is replaced by a new current source which is controlled by the high-pass output and threshold. It is still gated by the comparator output.

is controlled by the high-pass filter output of the amplifier and still gated by the comparator. Since the feedback current is now a function of the pulse height at a given time, smaller signals receive a weaker current while larger signals receive a stronger feedback. This ensures a more uniform response of the TE by compensating the difference in amplitude.

3 Simulation and measurement results

To gauge the performance of the circuit, the delays $d_{\mathrm{LE/TE}}$ of the respective comparator edges are measured with respect to a charge injection signal which are annotated in the left plot in figure 4. As only the change of the delay as function of the input charge Q is of interest the figure of merit

$$\Delta t = d_{\mathrm{LE/TE}}(Q) - \min(d_{\mathrm{LE/TE}}) \tag{3.1}$$

is defined. $\min(d_{\mathrm{LE/TE}})$, the smallest delay of a given data set for each edge, is subtracted to remove offsets in time. The range of the simulated input charges has been chosen according to the expectation of achieving full depletion of a 280 µm thick sensor which has about 50 µm depletion at $1 \times 10^{16} n_{\mathrm{eq}}/\mathrm{cm}^2$ radiation [14].

The compensating feedback pixel in UKRI-MPW0 was implemented as copy of the RD50-MPW2 switched-reset pixel with the switched feedback source being replaced by the new circuit. The parasitic layout extraction of the pixel was used to optimise bias setting with respect to the original switched-reset pixel. The results of transient simulations for a range of signal charges are plotted on the right in figure 4. It can be seen that the TE is almost identical for the medium range of the simulated input charges such that full compensation is achieved in these cases. However, figure 4 also shows the limitations of the circuit. For very small signals in the order of 4 ke or less, the Time-over-Threshold (ToT) of the comparator is too short for the feedback to properly work and no compensation is achieved. Large signals cause the amplifier to saturate such that the compensation mechanism cannot work as intended any more. Δt for both edges for a larger charge range is also plotted in figure 5 and the previously identified regions of performance are annotated. The LE exhibits the expected large time walk for small charges which decreases significantly for large charges. The optimum of the TE is achieved around 7 ke in which the time walk is almost completely compensated. It should be noted that even though the compensation circuit is not fully working for charges around

2025 JINST 20 C03052

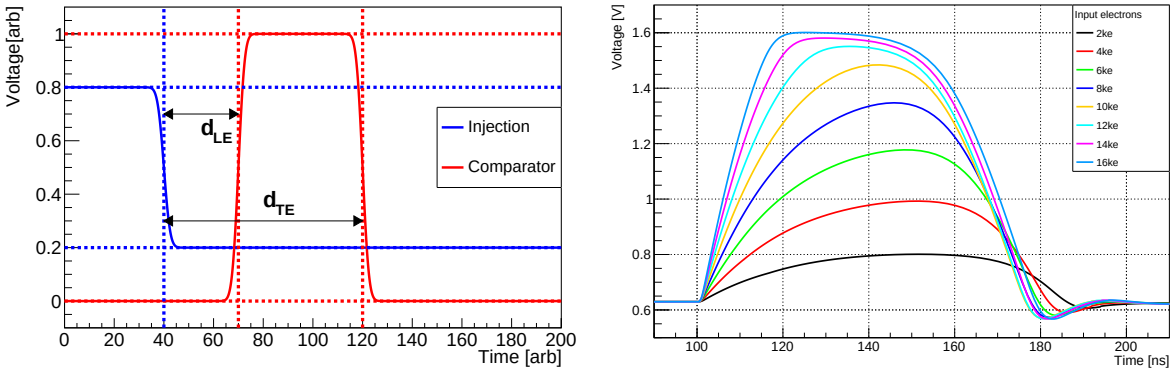

Figure 4. *Left*: sketch showing how the delays $d_{\mathrm{LE/TE}}$ are measured. The reference times (dashed vertical lines) for the injection and comparator edges are defined by the 50% point between the higher and lower levels (dashed horizontal lines) of the respective signal. *Right*: simulated transient amplifier response of the compensating feedback pixel to different amounts of input charge.

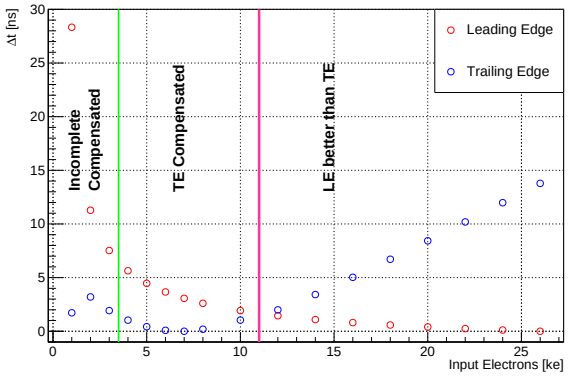

Figure 5. Δt extracted from post-layout transient simulation as function of input charge for both edges.

3 ke or below, the time walk for the TE in this region is significantly less than for the LE. Up to 16 ke the time walk for the TE is below 5 ns. For charges around 11 ke both edges perform equally well such that this point is defined as cross-over point. For lower charges the TE performs better while for larger signals the LE is the better estimator of the ToA of a charged particle.

The ideal performance of the system is achieved when both edges are sampled and the ToT at the cross-over point is known. The ToA can then be defined as:

$$\mathrm{ToA} = \begin{cases} \mathrm{t_{TE}} - \mathrm{offset_{TE}} & \mathrm{ToT} < \mathrm{ToT_{cross\text{-}over}} \\ \mathrm{t_{LE}} - \mathrm{offset_{LE}} & \mathrm{ToT} \geq \mathrm{ToT_{cross\text{-}over}} \end{cases} \tag{3.2}$$

Using this definition the time walk in figure 5 would be limited to around 4 ns or less. As the slopes of Δt as function of charge of both edges are small at the cross-over point, $\mathrm{ToT_{cross\text{-}over}}$ does not have to be determined very precisely as the induced error is small.

The timing performance of the pixel circuit on the fabricated sensor was evaluated and results are presented in figure 6. Here, test pulses of different voltages are injected into the pixel and the timing of both edges are recorded relative to the trigger of the injection pulse. The delays are derived from this data and the associated errors are derived by the standard deviation of the data points for each injection voltage. In the right plot in figure 6 the bias setting for the compensating feedback is scanned. While

2025 JINST 20 C03052

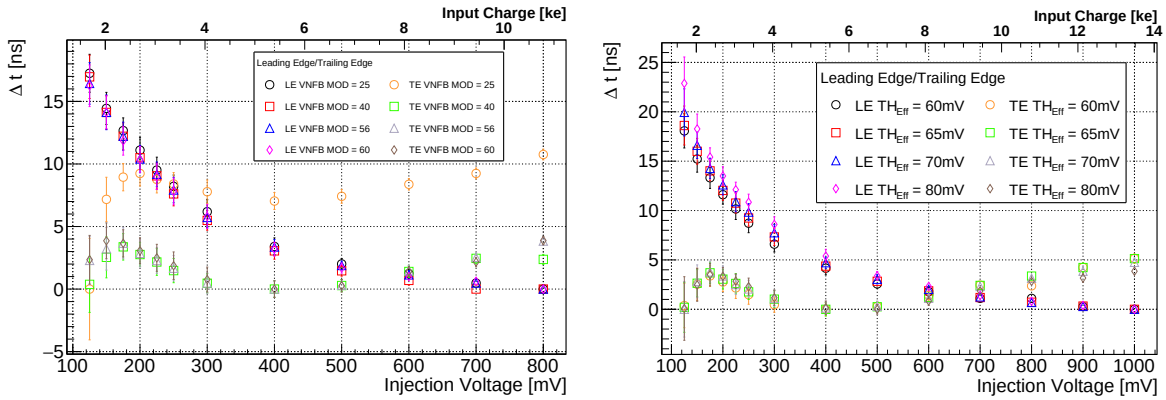

Figure 6. *Left*: Δt as function of input charge and bias setting for the compensating feedback VNFB MOD. *Right*: Δt as function of input charge and effective threshold TH_{Eff} = Threshold-Baseline.

the measurement points for all bias settings follow the shape in figure 5, a very high setting of 40 or higher is required to achieve full compensation. This is a lot higher than the optimised working point in the simulation of 6, indicating that some parasitics have been underestimated by the extraction. The higher bias setting also explains why the region of optimal compensation and the cross-over point are at slightly lower charges compared to figure 5, although the conversion of injection voltage to charges relies on the nominal design injection capacitance which carries a significant uncertainty. However, figure 6 replicates the shape of figure 5 almost perfectly and also peaks at a Δt of around 4 ns. In the right plot of figure 6 the effective threshold TH_{Eff} = Threshold-Baseline is varied to test the robustness of the circuit against dispersion in the amplifier gain or comparator threshold. As expected, the LE shows a deterioration for small charges at increasing thresholds. Remarkably, the TE exhibits no noticeable influence of the threshold. This indicates that the dynamic range of the circuit is large enough such that it can compensate even at shorter ToTs while keeping the cross-over point constant. Error bars on the data points in figure 6 are given by the standard deviation of the data set for each configuration and give an estimate of the jitter of each edge. Above 3 ke input charge, the jitter for both edges is less than 1 ns and less than 0.5 ns for charge larger than 7 ke in both figures. As the comparator was not optimised for the TE it performs worse than the LE. Between 3 ke and 6 ke the TE exhibits almost identical jitter which is less than 10% larger than the jitter of the LE.

4 Conclusion

A novel concept for analogue time walk compensation in the analogue frontend of a silicon detector has been designed, simulated and measured. Results measured with the fabricated chip demonstrate that the circuit is able to keep the time walk below 5 ns over a large range of signal charge. Using a simple discrimination to select either the time of the Leading Edge or the time walk compensated Trailing Edge could be implemented on the chip reducing the required bandwidth for the hit data. This scheme would be well suited to collider environments like the LHC where hits need to be assigned to the correct bunch crossing.

Classical time walk correction based on ToT are typically limited by the matching of the timestamp binning to the dynamic range of the amplifier. For a more comprehensive comparison between the two methods, more complex simulations are required which take the binning and jitter for a reference input spectrum into account.

2025 JINST 20 C03052

The new feedback source is only 25% larger than the switched feedback source it replaced (66 μm^2 vs 52.5 μm^2). In simulation the optimised nominal working point consumes 20% less power than the original switched-reset pixel at its nominal conditions (20 µW vs 25 µW for a sensor capacitance of about 200 fF [15]). Due to the emphasis on the Trailing Edge, the Leading Edge does not need to be as steep such that the amplifier bias current can be reduced.

Due to time constraints of the submission, the circuit was not fully simulated in terms of stability and corner performance. Oscillations and ringing have been observed in the circuit in some pixels under certain biasing conditions and concepts to address these issues and to improve the circuit are under investigation. Further measurements are required to determine the dispersion in performance of the pixels and their optimal working points. As the circuit reduces the dependence of the comparator delay to the input charge, the impact of noise from the diode should be reduced in this scheme. While the optimal working conditions in the fabricated chip differ from the settings in simulation the performance is replicated and a proof-of-concept was demonstrated.

Acknowledgments

For this circuit a UK patent has been filed under the reference 2404472.9. Patent pending. This work has received funding from UK Research and Innovation (UKRI) under the grant reference MR/S016449/1.

References

[1] H.F.W. Sadrozinski, A. Seiden and N. Cartiglia, *4D tracking with ultra-fast silicon detectors*, *Rept. Prog. Phys.* **81** (2018) 026101 [arXiv:1704.08666].

[2] N. Cartiglia et al., *4D tracking: present status and perspectives*, *Nucl. Instrum. Meth. A* **1040** (2022) 167228 [arXiv:2204.06536].

[3] M. Milanesio et al., *Time resolution of a SiGe BiCMOS monolithic silicon pixel detector without internal gain layer with a femtosecond laser*, 2024 *JINST* **19** P04029 [arXiv:2401.01229].

[4] M. Milanesio et al., *Gain measurements of the first proof-of-concept PicoAD prototype with a ^{55}Fe X-ray radioactive source*, *Nucl. Instrum. Meth. A* **1046** (2023) 167807.

[5] R. Blanco et al., *HVCMOS Monolithic Sensors for the High Luminosity Upgrade of ATLAS Experiment*, 2017 *JINST* **12** C04001.

[6] Y. Degerli et al., *MiniCACTUS: A 65 ps Time Resolution Depleted Monolithic CMOS Sensor*, arXiv:2309.08439.

[7] J. Braach et al., *Test-beam performance results of the FASTPIX sub-nanosecond CMOS pixel sensor demonstrator*, *Nucl. Instrum. Meth. A* **1056** (2023) 168641 [arXiv:2306.05938].

[8] S. Cadeddu et al., *Recent developments in the IGNITE project on front-end design in CMOS 28-nm technology*, 2024 *JINST* **19** C01040.

[9] C. Zhang, *Development of Depleted Monolithic Active Pixel Sensors for High Energy Physics Experiments*, Ph.D. Thesis, University of Liverpool (2021), DOI:10.17638/03149533.

[10] A. Schöning et al., *MuPix and ATLASPix — Architectures and Results*, *PoS* **Vertex2019** (2020) 024 [arXiv:2002.07253].

[11] P. Rymazewski et al., *Development of depleted monolithic pixel sensors in 150 nm CMOS technology for the ATLAS Inner Tracker upgrade*, *PoS* **TWEPP-17** (2018) 045 [arXiv:1711.01233].

2025 JINST 20 C03052

[12] J. Hammerich, *Evaluation of an HV-CMOS Pixel Sensor Prototype for the LHCb Mighty Tracker and Development of a Novel Circuit for Improved Time Resolution*, Ph.D. Thesis, University of Liverpool (2024), DOI:10.17638/03184751.

[13] C. Zhang et al., *Design and evaluation of UKRI-MPW0: An HV-CMOS prototype for high radiation tolerance*, *Nucl. Instrum. Meth. A* **1040** (2022) 167214.

[14] B. Wade et al., *Edge-TCT evaluation of high voltage-CMOS test structures with unprecedented breakdown voltage for high radiation tolerance*, 2022 *JINST* **17** C12017.

[15] C. Zhang et al., *Design and evaluation of UKRI-MPW0: a monolithic HV-CMOS pixel sensor with backside biasing*, 2024 *JINST* **19** P11011.

2025 JINST 20 C03052