Noise Behavior of a 180 nm CMOS SOI Technology for Detector Front-End Electronics

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***Abstract*— This paper is motivated by the growing interest of the detector and readout electronics community towards silicon-on-insulator CMOS processes. Advanced SOI MOSFETs feature peculiar electrical characteristics impacting their performance with respect to bulk CMOS devices. Here we mainly focus on the study of these effects on the noise parameters of the transistors, using experimental data relevant to 180 nm fully depleted SOI devices as a reference. The comparison in terms of white and 1/f noise components with bulk MOSFETs with the same minimum feature size gives a basis of estimate for the signal-to-noise ratio achievable in detector front-end integrated circuits designed in an SOI technology.**

***Index Terms* — Silicon-On-Insulator, MOSFET, Noise, Front-End Electronics.**

I. Introduction

CMOS SOI (Silicon-On-Insulator) technologies have become very attractive for the design of advanced sensors and readout electronics for the future generation of high energy physics experiments and for other scientific applications. They provide a technique for the integration of readout electronics isolated by the buried oxide layer (BOX) from a high resistivity substrate where fully-depleted detector elements can be located [1]. From the standpoint of microelectronic integration, SOI processes with an ultra-thin, fully-depleted (FD) silicon film may be able to overcome critical issues associated with standard CMOS scaling [2]. Association of SOI with vertical integration techniques can lead to 3-D multilayer structures including sensors and mixed-signal readout electronics with high functional density [3, 4]. This is a very promising scenario; however, it requires to verify if SOI devices can achieve the very good properties demonstrated by deep submicron bulk CMOS detector readout electronics. This is especially interesting for FD-SOI transistors, where peculiar physics mechanisms take place [5]. In this paper, we focus on studying how these mechanisms may affect the noise behavior of the devices and how this may impact the performance of a detector front-end system.

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II. Investigated Devices and Experimental Setup

This analysis is based on the experimental results of noise measurements carried out on FD-SOI devices belonging to the 180 nm process described in [4]. This technology was developed by MIT Lincoln Laboratory and can be integrated into a 3-D fabrication process. The BOX thickness is 400 nm and the thickness of the active silicon film above the BOX is 40 nm. The maximum allowed supply voltage V_{DD} is 1.5 V. Besides the source, gate and drain pads, the devices have a body contact pad which was grounded during the measurements. The tests were carried out on three process monitor chips from different wafers, with 60 NMOS and PMOS with an open layout and with various gate areas. A comparison with the behavior of bulk CMOS counterparts is achieved by using noise data relevant to 180 nm MOSFETs manufactured by TSMC and STMicroelectronics [6]. As for the FD-SOI process, the gate oxide thickness is 4 nm for these devices.

The gate-referred noise voltage spectrum was measured using instrumentation purposely developed at the Electronic Instrumentation Laboratory, University of Pavia. The noise of the device under test is amplified by a wideband interface circuit and detected by a Network/Spectrum Analyzer HP4195A [7]. Measurements of static and signal parameters were carried out with an Agilent E5270B Precision Measurement Mainframe with E5281B SMU modules.

III. Experimental Results

A. Kink Effect and Lorentzian Noise

It is well-known that SOI NMOSFETs exhibit floating body effects, which may result in typical kinks in the drain current I_D versus drain–to-source voltage V_{DS} characteristics. The kink effect is due to impact ionization arising from channel current carriers accelerated in the high-field drain

depletion region, where they create electron-hole pairs. The generated holes may accumulate in the device body, increasing its potential and decreasing the threshold voltage. As a result, I_D shows a steep increase when V_{DS} exceeds a value needed for a significant impact ionization to occur. As shown by Fig. 1, the FD-SOI NMOS transistors studied in this paper clearly exhibit a kink effect in the I_D-V_{DS} characteristics, which points out that they do not operate in an ideal full depletion mode. Moreover, the presence of a single body contact does not appear to be effective in suppressing these effects. This can be explained by the high resistance of the thin body region. As expected, kink effect is less evident in PMOSFETs, since holes are less effective than electrons in giving impact ionization. The discussion of the kink effect dependence on transistor parameters and bias voltages is available in the literature [8].

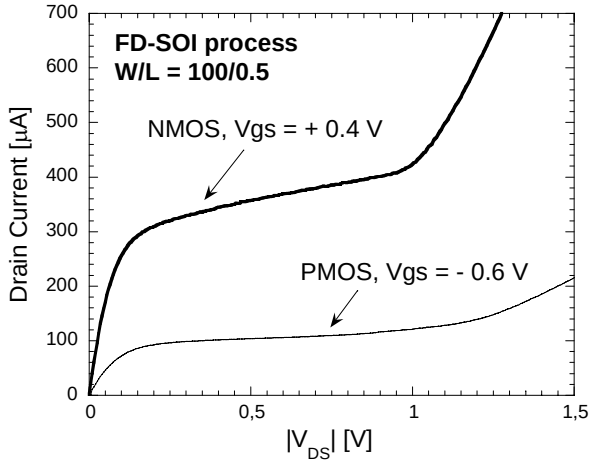

Fig. 1. Drain current as a function of the drain-to-source voltage for FD-SOI MOSFETs with W/L = 100/0.5.

Kink effect is also associated with Lorentzian-like low frequency contributions affecting the series noise voltage spectrum when V_{DS} is increased towards the maximum allowed voltage V_{DD} [9, 10]. As shown by Fig. 2, we detected these excess noise terms in FD-SOI NMOS devices, which confirms that actually the body is not ideally depleted.

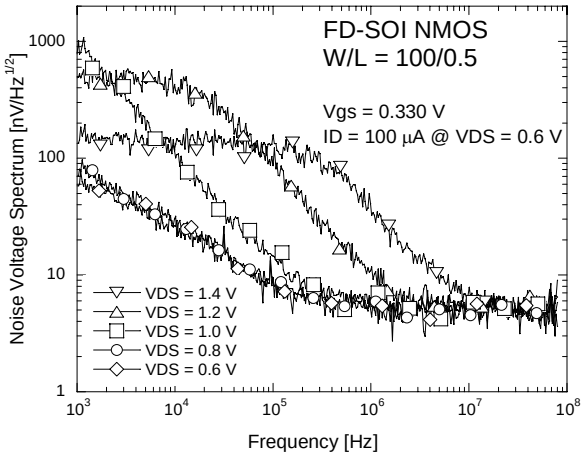

Fig. 2. Noise voltage spectra of an FD-SOI NMOSFET with W/L = 100/0.5 and V_{DS} from 0.6 V to 1.4 V. At V_{DS} = 0.6 V, I_D = 100 μA.

For $V_{DS} \geq$ + 1.2 V, in the examined frequency range the noise voltage spectra feature the typical Lorentzian behavior, with a plateau up to a characteristic frequency followed by a $1/f^2$ roll-off. The Lorentzian cutoff frequency shifts towards higher values when V_{DS} is increased. According to the model proposed in [10], this may be explained by the increase in the impact ionization current, which in turn decreases the small-signal resistance of the body-source junction. The Lorentzian characteristic frequency therefore increases, since it is inversely proportional to the product of this resistance and the body–to-ground capacitance.

From Fig. 2, when the device is biased below the kink onset voltage ($V_{DS} \leq$ 0.8 V), the noise voltage spectrum has a very little dependence on V_{DS}. For best performance, this dictates to operate the devices at $V_{DS} \leq V_{DD}/2$. This rule is usually applied in analog front-end design as far as the preamplifier input device is concerned. However, other devices such as loads may also be critical for a low noise performance, and care must be taken to operate them at a low enough V_{DS} to avoid excess noise associated with kink effect.

In PMOSFETs, the impact of kink effect is smaller also as far as the noise voltage spectrum is concerned. As shown by Fig. 3, an increase of low-frequency noise is noticed only when $|V_{DS}|$ is close to the maximum allowed voltage V_{DD}.

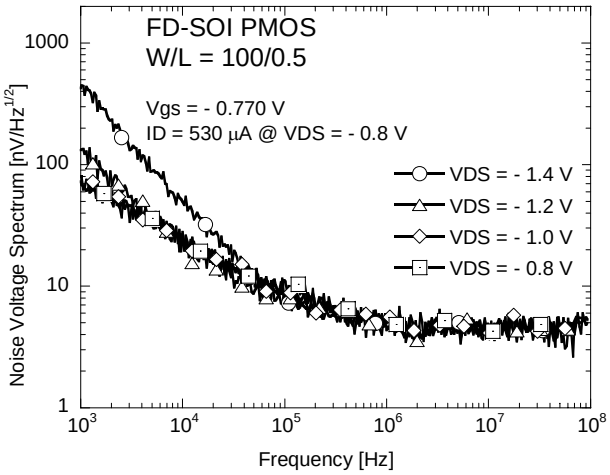

Fig. 3. Noise voltage spectra of an FD-SOI PMOSFET with W/L = 100/0.5 and V_{DS} from - 0.8 V to - 1.4 V. At V_{DS} = - 0.8 V, I_D = 530 μA.

B. 1/f Noise

At V_{DS} small enough to avoid the kink effect, the low-frequency noise of the investigated FD-SOI devices is of a 1/f nature. As in bulk CMOS transistors, 1/f noise is to a large extent independent of the drain current, as shown by Fig. 4.

In the investigated process, at V_{DS} below the kink onset voltage, NMOS and PMOS devices with identical gate width W and length L have a very similar noise behavior, as shown by Fig. 5. This is an interesting feature, since in deep submicron bulk CMOS processes PMOSFETs exhibit a sizably smaller low-frequency noise. This is apparent from the data in Table I, reporting 1/f noise parameters for the FD-

SOI process (including PMOS and NMOS with minimum gate length) and for two bulk CMOS technologies with the same minimum feature size [6]. In bulk CMOS, the fact that PMOSFETs feature a smaller low-frequency noise than equally sized NMOSFETs was generally related to buried channel conduction [11, 12]. In SOI CMOS, the active silicon film is so thin that the conduction takes place close to the surface and to oxide traps also in P-type devices. This might be the reason why the magnitude of their 1/f noise is close to N-type counterparts. An alternative explanation could be found in an interaction of the charge carriers with the thick buried oxide. However, this seems unlikely, since the appearance of the kink effect also in PMOSFETs points out that the channel interface to the BOX is only weakly depleted. It is then reasonable to assume that most of the drain current flows in a region closer to the front gate oxide, and that the quality of this thin oxide layer determines the 1/f noise properties of the devices.

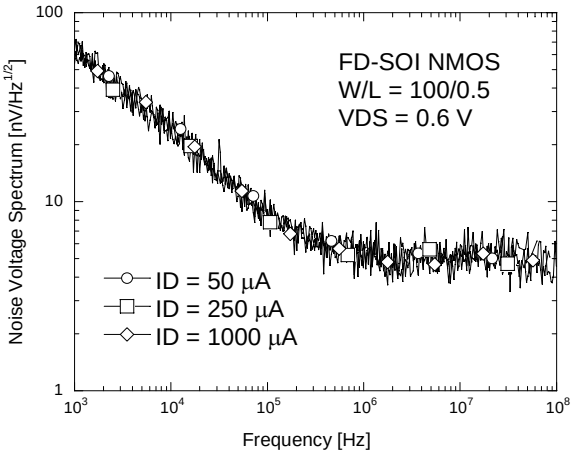

Fig. 4. Noise voltage spectra of an FD-SOI NMOSFET with W/L = 100/0.5 at I_D from 50 μA to 1 mA.

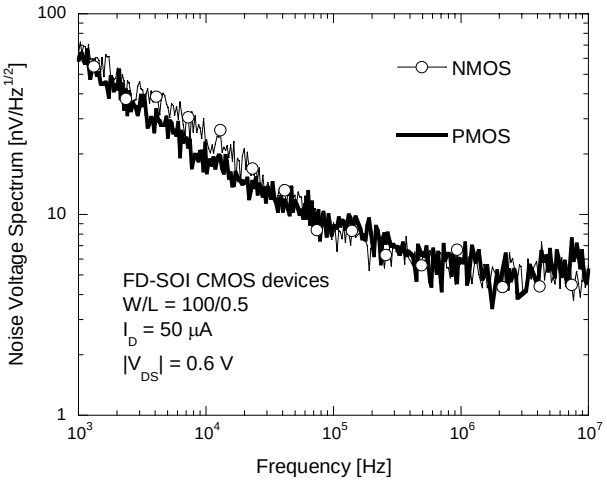

Fig. 5. Noise voltage spectra of FD-SOI NMOSFET and PMOSFET with W/L = 100/0.5 at I_D = 50 μA.

The 1/f contribution to the noise voltage spectrum can be expressed as:

$$S_{1/f}^2(f) = \frac{K_f}{C_{OX}WL}\frac{1}{f^{\alpha_f}} \quad (1)$$

where K_f is an intrinsic process parameter for 1/f noise, C_{OX} is the gate capacitance per unit area and the exponent α_f determines the slope of the 1/f noise term.

According to Table I, K_f and α_f values for SOI NMOSFETs are very close to those featured by bulk NMOS devices. For SOI PMOSFETs, K_f is instead larger than for bulk counterparts, confirming the worse 1/f noise properties of the examined process for this device polarity.

TABLE I
1/f NOISE PARAMETERS FOR 180 nm CMOS SOI AND BULK TECHNOLOGIES

180 nm CMOS foundry	Polarity	α_f	K_f $\left(10^{-25}\,\mathrm{J\,Hz^{\alpha_f-1}}\right)$
FD-SOI	NMOS	0.9	10
	PMOS	1	15
TSMC, bulk	NMOS	0.9	10
	PMOS	1	5
STMicroelectronics, bulk	NMOS	0.9	15
	PMOS	1.1	8

As a general comment, 1/f noise can be expected to be strongly process-dependent in SOI processes as it is in bulk CMOS. This means that it is safe to characterize it with extensive device measurements for a correct assessment of a candidate technology for the implementation of low-noise electronics.

C. White Noise

In Fig. 4, it is apparent that not only 1/f noise but also white noise in the high frequency part of the spectrum is insensitive to drain current variations. This behavior can be attributed to a noisy parasitic body resistor adding a constant contribution to channel thermal noise in the white part of the spectrum [13, 14]. According to this model, the white noise voltage spectrum can be expressed as follows:

$$S_W^2 = 4k_BT\frac{\Gamma}{g_m} + 4k_BTR_{body}\frac{g_{mb}^2}{g_m^2} \quad (2)$$

In (2), the first term is given by channel thermal noise; k_B is the Boltzmann's constant, T is the absolute temperature and g_m is the transconductance. The value of the coefficient Γ depends on the degree of channel inversion and on the effect of the bulk on the transconductance; in submicron devices it may be increased by short channel effects such as mobility reduction and hot carriers [12]. The second term in (2) is given by the thermal noise in the parasitic body resistor R_{body}, which generates drain current fluctuations through the body transconductance g_{mb}. Since the ratio g_{mb}/g_m is independent of the drain current [15], this contribution is not expected to change at different I_D and dominates white noise in the I_D range investigated in Fig. 4. This excess noise term increases when the gate length is shrinked, as shown by

Fig. 6, because R_{body} also increases. The value of the parasitic body resistor can be calculated by $R_{body} = R_B \cdot (W/L)$, where R_B is the resistivity per unit silicon film thickness of the body [8].

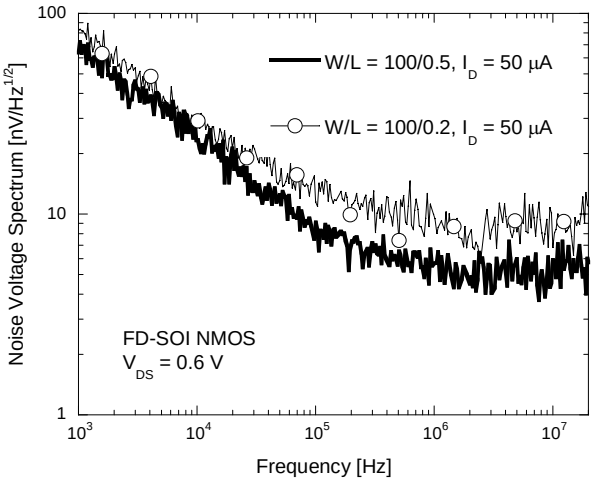

Fig. 6. Noise voltage spectra of FD-SOI NMOSFETs with W/L = 100/0.5 and with W/L = 100/0.2 at I_D = 50 μA.

At smaller drain currents, g_m decreases and channel thermal noise gives a larger contribution to the total white noise voltage spectrum. This means that the limitation from the additional noise term due to the body resistor becomes less evident. Fig. 7 and 8 show the noise voltage spectra of an FD-SOI NMOS measured at I_D = 50 μA and I_D = 10 μA respectively, together with the channel thermal noise values calculated according to the first term in (2) and to g_m values measured at the same drain currents. The plots also report the value of Γ in (2), which was calculated from the relationship [12]:

$$\Gamma = \frac{1}{1+\dfrac{I_D L}{I_Z^* W}}\left[\frac{1}{2}+\frac{2}{3}\frac{I_D L}{I_Z^* W}\right]\cdot n \qquad (3)$$

In (3), I_Z^* is the characteristic normalized drain current which sets the boundary between weak and strong inversion, and the coefficient n is proportional to the inverse of the subthreshold slope of I_D as a function of the gate-to-source voltage V_{GS}. The values extracted from measurements on NMOS devices in this process are I_Z^* = 0.35 μA, n = 1.2.

From Fig. 7, at I_D = 50 μA it is apparent that the calculated channel thermal noise is well below the measured white noise level, which is therefore determined by the noise in the body resistor. At I_D = 10 μA, this excess white noise contribution has a smaller weight on the total measured white noise, which is close to the calculated channel thermal noise, as shown by Fig. 8. This is the expected behavior at a drain current density $I_D/W \cong 0.15$ μA/μm, which is a typical operating condition for front-end devices in low power readout systems.

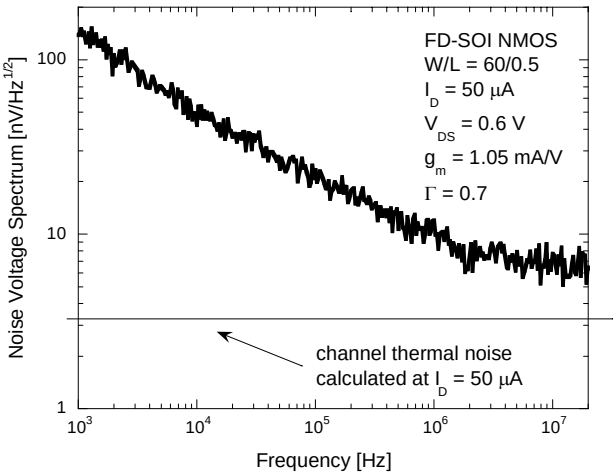

Fig. 7. Noise voltage spectrum of an FD-SOI NMOSFET with W/L = 60/0.5 at I_D = 50 μA and channel thermal noise value calculated at the same drain current.

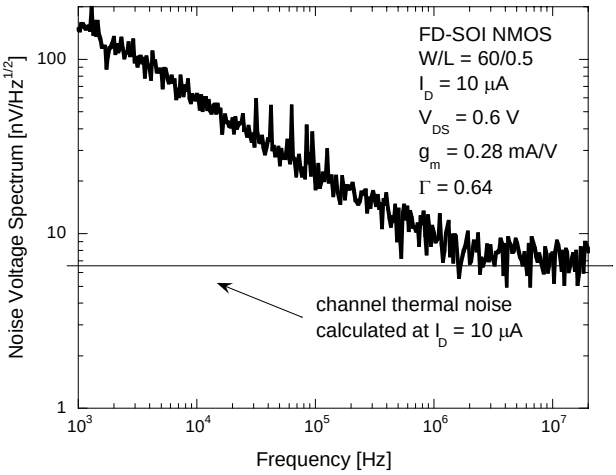

Fig. 8. Noise voltage spectrum of an FD-SOI NMOSFET with W/L = 60/0.5 at I_D = 10 μA and channel thermal noise value calculated at the same drain current.

D. Effect of backgate voltage

In applications where the device substrate below the BOX is used as a high resistivity sensor, a depletion voltage will be applied to the substrate itself. In thin body SOI MOSFETs, this is expected to affect the threshold voltage by the backgate action of the buried oxide [5]. This effect is observed also in the FD-SOI devices examined in this paper, as shown by Fig. 9. The plot shows how a positive backgate voltage V_{bg} decreases the threshold voltage, which is instead increased by applying a negative V_{bg}.

Fig. 10 shows the effects of the backgate voltage on the noise voltage spectrum of an FD-SOI NMOSFET. The noise is affected only at positive V_{bg}, when the backgate comes into play in depleting the active silicon film. The noise degradation may be due to the increased interaction of charge carriers with the thick backgate oxide, since thicker oxides are associated with higher low-frequency noise contributions [16].

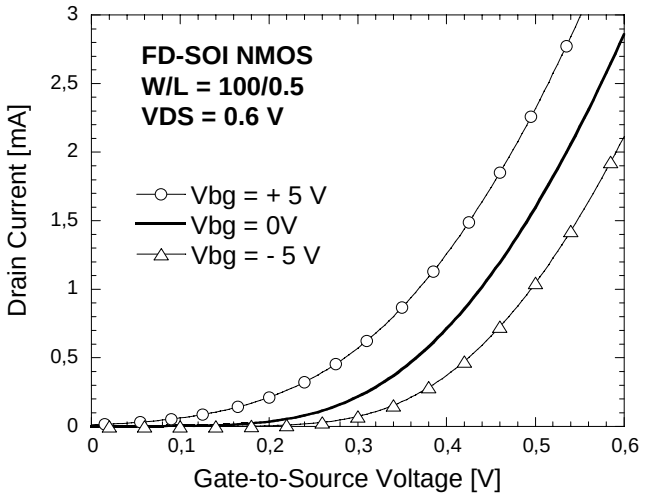

Fig. 9. Drain current I_D as a function of the gate-to-source voltage V_{GS} for an FD-SOI NMOSFET with W/L = 100/0.5 at different backgate voltages V_{bg}.

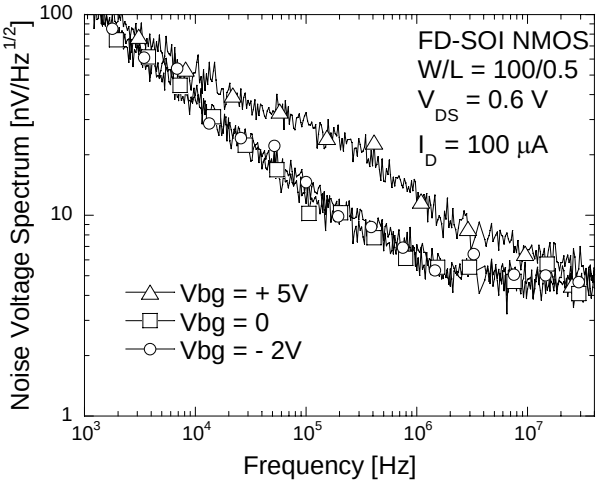

Fig. 10. Noise voltage spectra of an FD-SOI NMOSFET with W/L = 100/0.5 at I_D = 100 μA at three different values of the backgate voltage V_{bg}.

IV. Discussion

The noise performance of a detector readout system can be assessed in terms of the Equivalent Noise Charge (ENC). In the case of CMOS front-end systems, ENC is mostly determined by the noise voltage spectrum of the preamplifier input device, and can be described as follows [17]:

$$ENC^2 = S_W^2 \frac{A_1}{t_P} C_T^2 + (2\pi)^{\alpha_f} A_2(\alpha_f) \frac{K_f}{C_{OX} WL} t_P^{\alpha_f - 1} C_T^2 \quad (4)$$

In (4), C_T is the total capacitance at the preamplifier input, including the detector capacitance, the preamplifier input and feedback capacitances and the strays. t_P is the signal peaking time, A_1 and A_2 are coefficients depending on the signal shaping.

For the FD-SOI devices examined in this paper, the 1/f noise slope α_f is close to 1 for both N- and PMOS. If α_f = 1 in (3), the 1/f noise contribution to ENC is independent of the peaking time. This second term in (4) is expected to dominate at long t_P's. Here, front-end systems based on FD-SOI and bulk CMOS processes should feature similar performance, since in a same technology node 1/f noise parameters are comparable for bulk and SOI transistors, as discussed in Section III-B. This would be accurately true if the 1/f noise properties of the system are mostly determined by NMOSFETs. Unlike bulk technologies, at least in the case of the examined FD-SOI process, the use of PMOSFETs would not bring along any advantage with respect to NMOSFETs. Noise parameters are very similar for both device polarities, and P-channel SOI devices appear to feature higher low-frequency noise than bulk counterparts. Moreover, in SOI devices low-frequency noise may be affected by the backgate voltage. This is especially relevant in applications where their substrate is used as a sensor region for particle detection.

The first term in (4) is due to white noise and is dominant at short peaking times. Excess noise arising from parasitic resistors was analyzed in Section III-C, where it was pointed out as a degradation factor in the high frequency region of the noise voltage spectrum of SOI devices. This may affect the performance of a charge measuring system at short t_P's. However, at low current density the effect of this contribution should be less evident.

An effective evaluation of the noise performance when the gate width W is scaled to match the detector capacitance is provided by the normalized spectral density $C_i S_e^2(f)$ [6]:

$$C_i S_e^2(f) = C_i \left[S_W^2 + S_{1/f}^2(f) \right] = S_W^2 C_i + \frac{K_f}{f^{\alpha_f}} \quad (5)$$

$S_e^2(f)$ is the total gate-referred noise voltage spectrum, $C_i = C_{OX} WL$.

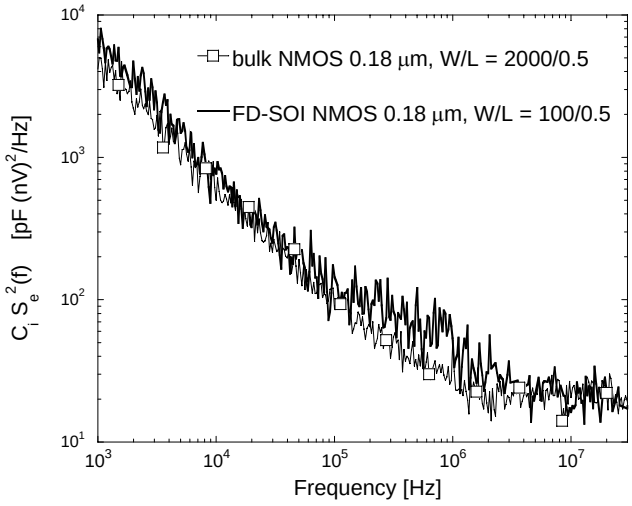

Fig. 11. Frequency dependence of the $C_i S_e^2(f)$ product for two NMOSFETs in the 0.18 μm CMOS generation. The device with W/L = 2000/0.5 is a bulk transistor manufactured by TSMC and was biased at I_D = 250 μA. The device with W/L = 100/0.5 is an FD-SOI transistor biased at I_D = 10 μA with V_{bg} = 0.

Fig. 11 compares the product $C_iS_e^2(f)$ for an FD-SOI and for a bulk NMOSFET in the 180 nm CMOS node. In the low-frequency region, the behavior of this product is determined by the 1/f noise parameter K_f, which is very similar for the two devices, as discussed above. At higher frequencies, the contribution from white noise is dominant. The two devices have the same gate length L and are biased at similar current densities I_D/W in the weak inversion region. In these conditions, they feature very close values of channel thermal noise [6]. In Fig. 11, this actually results in a very similar behavior in the white noise region, which points out that excess noise due to the body parasitic resistor does not degrade the performance of the FD-SOI device at this current density.

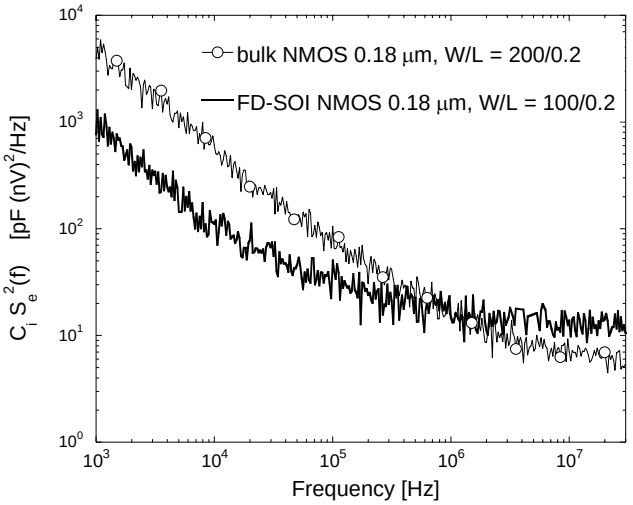

Fig. 12. Frequency dependence of the $C_iS_e^2(f)$ product for two NMOSFETs in the 0.18 μm CMOS generation. The device with W/L = 200/0.2 is a bulk transistor manufactured by TSMC and was biased at I_D = 50 μA. The device with W/L = 100/0.2 is an FD-SOI transistor biased at I_D = 25 μA with V_{bg} = 0.

Fig. 12 shows the product $C_iS_e^2(f)$ for an FD-SOI and a bulk device with a length equal to the minimum value allowed by the process. An interesting feature is outlined by this plot: in the case of bulk technologies, the 1/f noise parameter K_f sizably increases when L approaches the minimum gate length in a given process [17]. In Table I, K_f values for bulk technologies are an average which actually does not include data for minimum L transistors. This behavior is not detected in the FD-SOI devices we studied in this work, which is the reason why in Fig. 12 at low frequency the SOI transistor features a smaller value of the product $C_iS_e^2(f)$ as compared to the bulk device. At higher frequencies, the excess noise in the body resistor impairs the performance of the FD-SOI device, which is biased at a higher current density with respect to the NMOSFETs in Fig. 11.

As a general remark, the noise analysis presented here does not highlight any severe limitation in the use of a readout electronics based on SOI CMOS devices in an operating region complying with low power dissipation constraints.

V. Conclusion

This paper presented a discussion of the experimental results of noise studies carried out on devices from a 180 nm FD-SOI CMOS process. The data are relevant to one technology; however, they show effects which can be considered as typical for SOI transistors. Therefore they can give a hint of the problems to be tackled when designing a low noise SOI CMOS system. For a complete picture, other issues remain to be addressed, pertaining to the effects on noise which may be given by choosing various options in the device structure (e.g., body ties). Another concern is the noise behavior after irradiation. The thick buried oxide layer is expected to be radiation soft, which may impact low frequency noise as well as other parameters. The analysis of radiation effects in these devices deserves a dedicated study for a complete evaluation of noise degradation mechanisms, which will be carried out in a future paper.

Acknowledgment

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