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Prototyping of hybrids and modules for the forward silicon strip tracking detector for the ATLAS Phase-II upgrade

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Abstract: For the High-Luminosity upgrade of the Large Hadron Collider an increased instantaneous luminosity of up to $7.5 \cdot 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$, leading to a total integrated luminosity of up to $3000\,\mathrm{fb}^{-1}$, is foreseen. The current silicon and transition radiation tracking detectors of the ATLAS experiment will be unable to cope with the increased track densities and radiation levels, and will need to be replaced. The new tracking detector will consist entirely of silicon pixel and strip detectors. In this paper, results on the development and tests of prototype components for the new silicon strip detector in the forward regions (end-caps) of the ATLAS detector are presented. Flex-printed readout boards with fast readout chips, referred to as hybrids, and silicon detector modules are investigated. The modules consist of a hybrid glued onto a silicon strip sensor. The channels on both are connected via wire-bonds for readout and powering. Measurements of important performance parameters and a comparison of two possible readout schemes are presented. In addition, the assembly procedure is described and recommendations for further prototyping are derived.

Keywords: Si microstrip and pad detectors; Particle tracking detectors (Solid-state detectors); Solid state detectors

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1 Introduction

For the High-Luminosity phase of the LHC (HL-LHC), a roughly tenfold increase in the integrated and instantaneous luminosities is envisaged. The current inner detector of the ATLAS experiment will be unable to cope with these conditions, both in terms of radiation levels and occupancy, and will need to be replaced. The new inner tracking detector will be an all-silicon system consisting of four layers of pixel and five layers of strip detectors in the barrel region. In the end-cap region, six or more layers of pixel sensors and seven of strip detectors are currently foreseen [1]. However, the final layout is still under discussion.

In the strip detector system, a modular yet highly integrated approach is followed. Modules are built by glueing the front-end readout board, known as the hybrid, directly onto the silicon sensor and by wire-bonding the ASIC channels on the hybrid to the sensor pads. The module itself is glued onto a carbon-based support structure, including cooling pipes and a multi-layer tape, known as the bus tape, for electrical connectivity. This local support structure is called the stave for the barrel region and the petal for the forward region. Modules are populated on both sides of a stave/petal.

A sketch of a petal is given in figure 1. It shows one side of a petal as it is foreseen for the detector upgrade. The carbon-fibre core with cooling pipes inside and the cooling pipe connectors on the side of the petal are visible in the figure. Silicon-detector modules are glued for routing on top of a bus tape which is glued on the core. In addition, the petal-readout board is sketched. It will be placed to the side of the petal. The petal has a wedge-shape and 32 of them will be assembled to form one disc of the end-cap. Due to this the modules vary in size and for larger radii two modules are glued next to each other on the surface of the core. The sensors are n-in-p-type strip sensors with strip lengths between 18 mm and 48 mm, allowing several rows of strips on one sensor. Depending on the radius, there are one or two hybrids glued on one sensor. The ASICs are foreseen to be produced in a 130 nm CMOS process (ABC130 [2]) with 256 channels and four rows of wire-bond pads. This leads to a lower total number of ASICs and hybrids compared to the ones used in the prototyping described in the following. The chip is an analogue binary chip and allows to process signals from the silicon strip sensors in a binary read-out architecture.

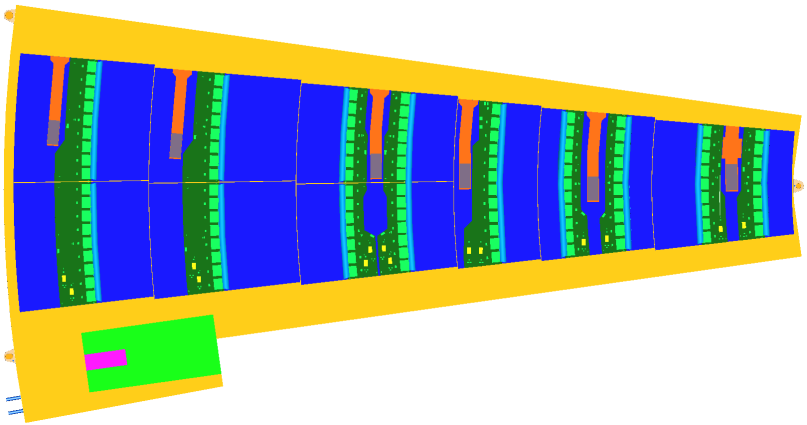

Figure 1. Sketch of a petal consisting of a carbon-fibre core with cooling pipes inside. One side is visible with silicon-detector modules glued on top. Cooling pipe connectors and the readout board of a petal are visible at the side of the petal. The layout is for ASICs produced in a 130 nm CMOS process.

In this paper the results of an R&D project and the prototyping efforts for modules for the forward part of the new silicon strip tracker are described. They are based on the investigation of a reduced-size version of the petal, referred to as the petalet.

In the petalet project, the most challenging geometrical part of the petal is addressed, namely the transition region from one to two sensors in the foreseen ring structures. The petalet consists of three sensors in total on each of its two sides, two upper sensors and one lower sensor. This allowed an investigation of most parts necessary for modules of a complete petal. A schematic sketch of one side of a two-sided petalet is shown in figure 2. It sketches the carbon-fibre core with cooling pipes, a lower module with one hybrid on top and two upper sensors for one or two upper modules. Lines on the upper sensors indicate the wire-bond area for placing the hybrid. The ASICs in the prototyping phase differ from them for petals. Therefore the number of hybrids and channels for modules differ between the petalet and a petal. The ASICs used for the petalet are produced in a 250 nm CMOS process (ABCN250 [3, 4]) with 128 channels and double-row of wire-bonds, resulting in half the channel numbers compared to modules foreseen in petals. Both the silicon

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sensors [5] and the hybrids were produced, tested and then assembled to so-called lower and upper modules for all sensor types required for the petalet. Despite their difference in ASIC types, the project allowed to build fully functional modules which can be used for prototyping of a larger structure. Moreover, it established the assembly and testing procedures for prototyping of modules for petals. The main purpose of the petalet project was a detailed investigation of two different design concepts. In one version, known as the *split readout scheme*, power and data connections are situated on opposite sides of a module. In contrast, in the *common readout scheme*, the power and data connections are on the same side. Based on the results of the R&D project a proposal for the design of full-size petals is derived.

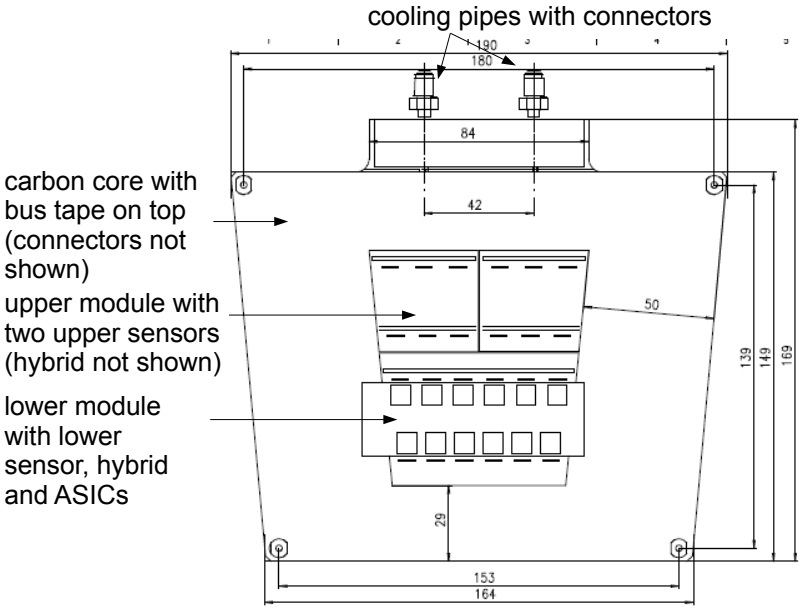

Figure 2. Sketch of a petalet consisting of a carbon-fibre core with cooling pipes inside. One side is visible with two upper sensors and a lower module glued on top. For the upper module the hybrid is not shown but lines indicate the placement and wire-bond area. For the lower module the hybrid is drawn on top.

2 Development and investigation of hybrids

The flex hybrid read-out boards appropriate for the ABCN250 were developed for the petalet programme. They are multi-layer flex PCBs with ASICs glued on top for readout of data and communication. After assembly and testing, these are glued on top of the silicon sensors and wirebonded to these to give the detector modules. For a given readout scheme either two or three different hybrid types were prototyped in the petalet project. Their layout, assembly, and electrical and mechanical test results are described in the following.

2.1 Hybrid layouts

The hybrids consist of a four-layer flex PCB and have ASICs glued on top. The layout principle is similar for all hybrids [6]. For the lower module, one hybrid spans fully across the silicon sensor. This is referred to as a lower module with a so-called lower hybrid. For the upper module, one

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or two hybrids depending on the readout scheme span across two sensors. Both the lower and the one/two upper hybrids carry two rows of six ASICs each, resulting in 768 channels per row. The main differences are in the geometry and the routing of readout and power to the bus tape. Circuits are designed with conservative design rules to optimise the yield in production. The thicknesses of layers are similar for all hybrids of the forward region and there are only small differences in the track width and gap thicknesses as listed in the respective sections. A schematic of the layers is provided in figure 3 (left). Three different kinds of vias are employed, as shown in the right part of figure 3. For the split readout scheme, power is routed on layer 2, differential signals on layer 3 and ground on layer 4, while for the common readout scheme, layer 2 routes signal, layer 3 power and layer 4 ground. In both layouts the hybrids are covered with a photosensitive dry film coverlayer with a thickness of 25 μm and the pads are covered with electroless nickel immersion gold.

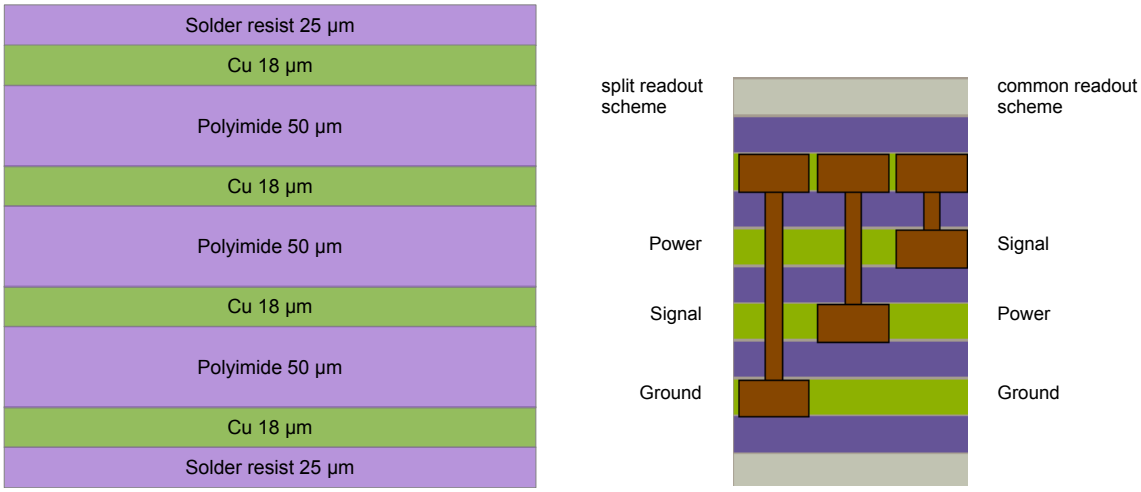

Figure 3. Sketch of thicknesses of the four-layer flex PCB of the hybrids (left) and the three different kinds of vias and routing of layers for both readout schemes (right).

The ABCN250 chips are used in the first stage of prototyping of both the barrel and the end-cap components of the strip-tracker upgrade. As described earlier, the large-scale production of final detector modules will be performed using ASICs produced in 130 nm CMOS technology, such that the results presented here will have to be reviewed in this context. The power consumption for 130 nm technology chips is roughly a factor of six smaller compared to 250 nm technology, while the noise is expected to be kept at the same level and the double number of channels reduces the amount of material. The main functional blocks of the binary readout chip are: front-end, input register, pipeline, derandomising buffer, data compression logic blocks, command decoder, readout logic, threshold and calibration control, and power regulation.

2.1.1 Hybrids in split readout scheme layout

In the split readout scheme, the data, clock and control lines are routed to one side of the hybrid, whereas low voltage power lines and high voltage bias lines are routed to the other side. Figure 4 illustrates the position of the two modules on a petalet and sketches the readout scheme. For the lower module, one hybrid spans fully across the silicon sensor. For the upper module, one hybrid,

the upper hybrid spans across two sensors. The latter feature is characteristic for the split readout scheme. As mentioned earlier, ASICs which will be used for the petal have the number of channels doubled and by this one hybrid could serve for all three sensors. For routing data and power to the petalet readout board the system needs a mirrored routing on the front- and back-side of the petalet. The inherent separation of the high-speed data and clock lines from the low- and high-voltage power lines by using bus tapes improves both signal and power integrity, even with relatively narrow bus tapes. In order to maintain signal and power integrity several measures are implemented in the hybrid design. For example, fast signals with sharp transitions are routed as thin lines with stable power/ground reference planes. Additionally, inter and intra pair spacing design rules have been applied, and special X2Y EMI filters [7] and coupling capacitors are utilised.

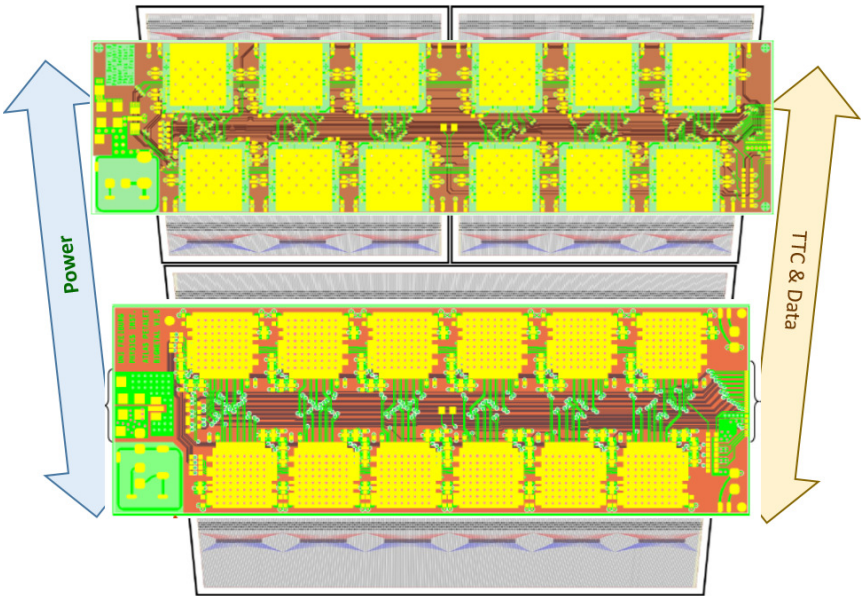

Figure 4. Sketch of the split readout scheme layout. Two modules, each consisting of one hybrid mounted on one (lower module) or two (upper module) sensors, respectively, are placed and read out on one bus tape on each side of a petalet. The power is routed on the left-hand side whereas data, clock, trigger and control (TTC) signals are routed on the right-hand side of the hybrids.

The split readout scheme hybrids have been designed according to the "IPC-2223A Class A (flex-to-install)" [8] flexible circuit industry standards and specifications. The applied width and gap are 100 μm/100 μm. The drill/pad parameters for vias are in the respective layers: L1/L2: 100 μm/300 μm, L1/L3: 125 μm/350 μm, L1/L4: 250 μm/500 μm. The assembly and reflow soldering of passive components on hybrids were performed in-house utilising a fully-automatic pick-and-place machine and an industry standard reflow oven. In total about 70 hybrids were assembled and evaluated as described in sections 2.2.1 and 2.3.2.

2.1.2 Hybrids in common readout scheme layout

The aim of the common readout scheme layout is to simplify the module construction by having one hybrid per sensor. This means that in comparison with the split readout scheme, two smaller hybrids are needed to cover the two upper sensors. These two hybrids (referred to as upper right,

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UR, and upper left, UL) can be only accessible from the right- or left-hand side of the bus tape, respectively. Thus, the routing has to be designed such that power and data lines are provided on both sides. To maintain good cooling properties, no routing is allowed on the tapes under the sensor area. Because of this, as can be seen in figure 5, a single piece of bus tape on either side of the module connects three hybrids, two on the front and one on the back-side of the petalet (and vice versa), by folding the bus tape by 180 degrees over the top edge of the carbon core, taking advantage of its flexibility. Combining fast data and power lines close by, requires careful design to avoid coupling of the DC/DC noise in data and high-voltage lines. Industry standards were applied and the minimum track width/separation is set to 100 μm/100 μm. Ground and power vias were designed with drill diameter/pad diameter/clearance diameter of 150 μm/400 μm/700 μm, while the diameters for signal vias are 100 μm/300 μm/600 μm.

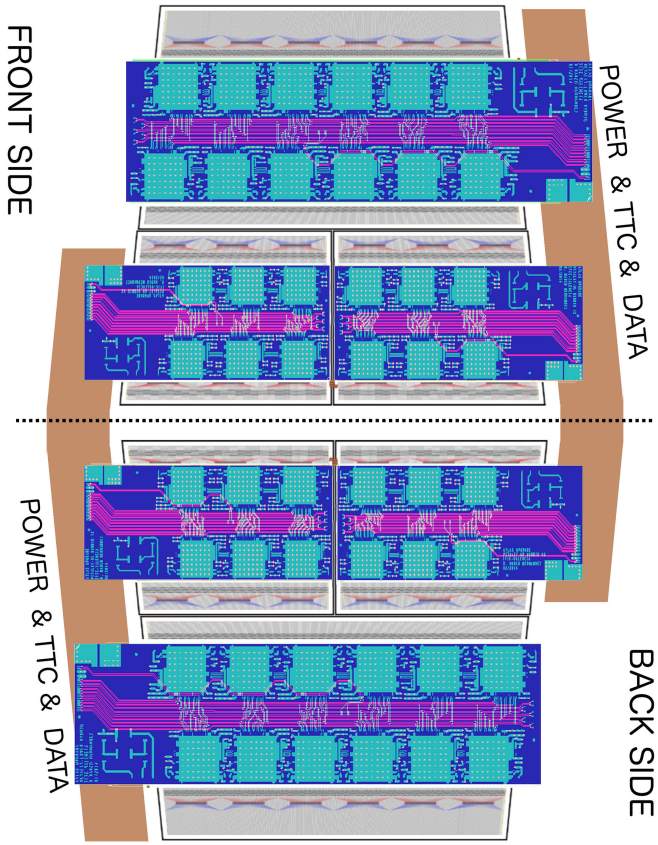

Figure 5. Sketch of the common readout scheme layout. Six hybrids are used to read out six sensors. A single piece of bus tape covers both the front- and back-side of the petalet, providing power and data lines for both sides.

The three different kinds of hybrids (a lower hybrid, an upper-left and an upper-right) populated with ASICs and passive components are shown in figure 6. Details on the assembly are given in section 2.2.2. The upper-left and the lower hybrids receive power and data lines from the left-hand side of the bus tape, while the upper-right hybrid is connected to the right-hand side. The lower hybrid has twelve ASICs, while each of the upper ones has six.

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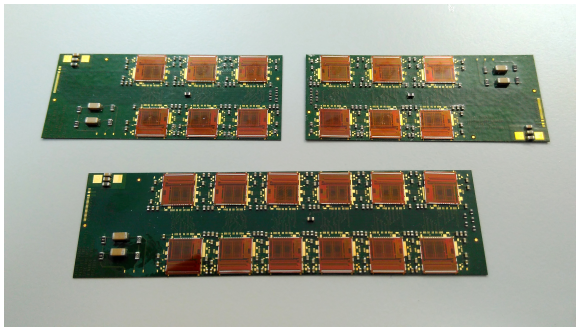

Figure 6. Photograph of the three different flavours of hybrids, a lower hybrid, an upper-left hybrid and an upper-right hybrid, for the common readout scheme. The upper-left and the lower hybrids receive power and data lines from the left-hand side, while the upper-right hybrid is connected to the right-hand side.

2.2 Hybrid assembly

For both concepts, the first assembly step is the population of the PCBs with passive components (resistors, capacitors and temperature sensors referred to as NTCs). A visual inspection is performed to check that no solder paste has been spilled over the bonding pads to assure that the pads on the PCB can be wire-bonded to. The ASICs are then glued onto the PCB. The results presented in this paper are obtained using the silver epoxy conductive glue TRA-DUCT 2902 from Henkel Inc [9]. In parallel, efforts have been made to qualify an alternative UV-curable glue to benefit from significantly shorter curing times and lower costs. Results can be found in ref. [10]. The thickness and the pattern of the glue determine the thermal conductivity. Moreover, the amount of glue has to be controlled in order to prevent it from spilling over the bonding pads placed around the footprint of the ASIC, which would result in shorted lines and make it impossible to wire-bond the connections between the ASICs and the hybrid at a later stage of the production process. The positioning of the readout chips is also important, because a slight variation will affect the bonding angle of the wire-bonds which connect the chip pads to the sensors strip pads.

For glueing the ASICs onto the hybrids, two assembly methods have been investigated: a method deploying custom-designed tooling, which has been used for both readout scheme layouts, and a method for individual glueing of the ASICs using a flip-chip machine. The latter was only tested in the common readout scheme layout. The assembly steps for both methods were performed in clean rooms and are described in the following sections.

2.2.1 Custom-design tooling method

This method was used for the assembly of hybrids of both readout schemes. Several dedicated tools for the assembly of lower and upper hybrids were manufactured. The assembly proceeds as follows: the ASICs are first placed in a chip-tray tool, providing a good relative positioning among all the chips (see figure 7, upper left). Then, they are picked up using a custom-made pick-up tool connected to a vacuum line and equipped with positioning pins that fit into positioning holes in the chip tray. Afterwards, the pick-up tool with the chips is placed upside-down in a holder. Figure 7 (upper right) shows the pick-up tool and the ASICs at this stage of the process. A steel stencil of a thickness of 130 μm is placed on the holder, covering the back-side of the ASICs.

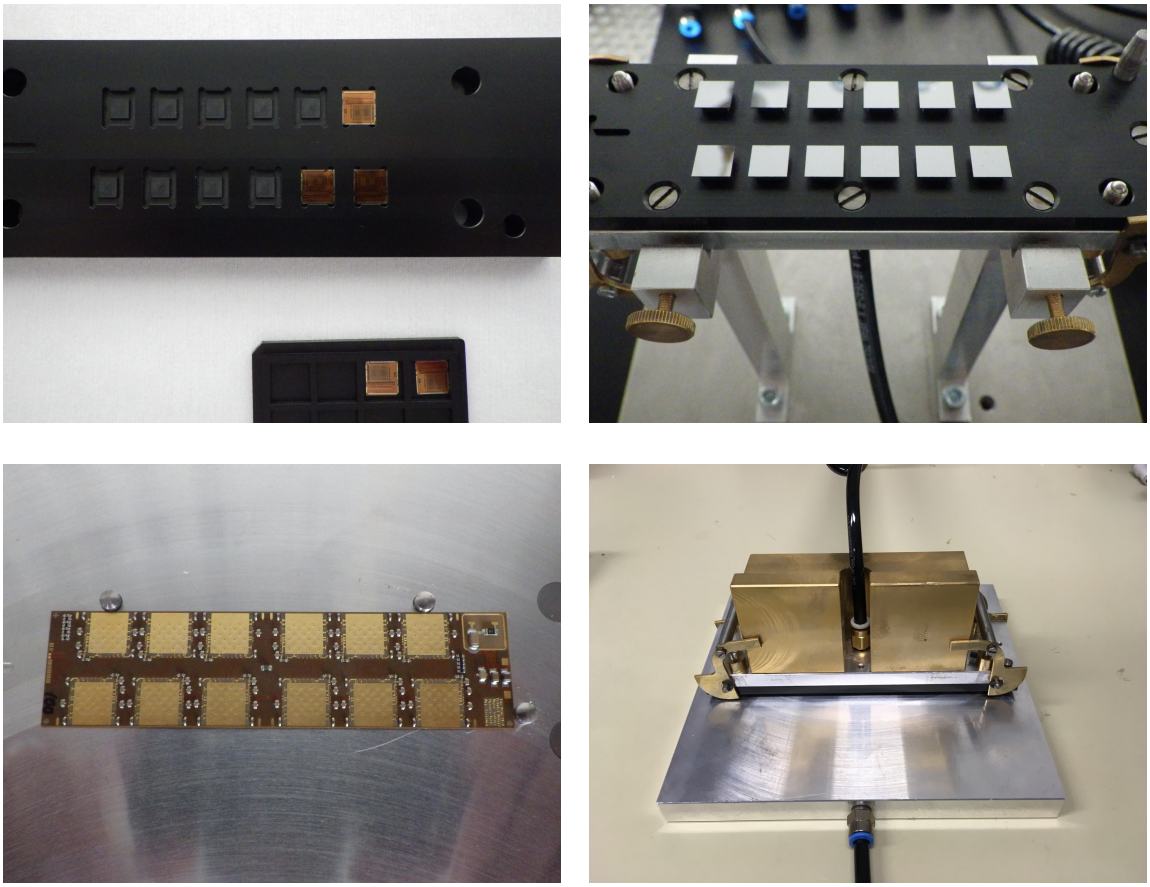

Figure 7. Chips in a partially filled chip tray (upper left), pick-up tool in a holder after picking up ASICs (upper right), upper hybrid before population with ASICs on a vacuum jig (lower left) and pick-up tool placing the ASICs onto a hybrid lying on a vaccum jig. The pictures are taken for hybrids of the split readout scheme.

This stencil determines the glue pattern and the amount of glue. Silver epoxy glue is applied using a plastic spatula. In parallel, the hybrid is placed onto a vacuum jig with positioning holes to align the pick-up tool (see figure 7, lower left). The stencil is then removed from the ASICs. The pick-up tool still holds the ASICs that now have the glue pattern deposited on their back-sides. The pick-up tool is then placed onto the hybrid jig. By this the back-side of the ASICs is pressed onto the top of the hybrid. The distance between the top of the hybrid and the back-side of the chips is controlled using adjustable high-precision screws in the pick-up tool. These act as spacers and control the thickness of the glue layer between the hybrid and the ASIC. The precision screws are adjusted once before the assembly of the first hybrid. A brass weight is then placed on top of the pick-up tool and the glue is cured for 24 hours at room temperature. Figure 7 (lower right) shows a picture of the curing step. The vacuum of the pick-up tool is not released until the curing is completed in order to keep the desired thickness of glue.

X-ray images are taken in order to verify that the glue pattern is spread correctly. An X-ray image of a chip glued to the hybrid (upper-left of common readout scheme layout) is shown in figure 8. The glue pattern can be seen as five separate dark dots. This pattern corresponds to what is expected for stable assembly.

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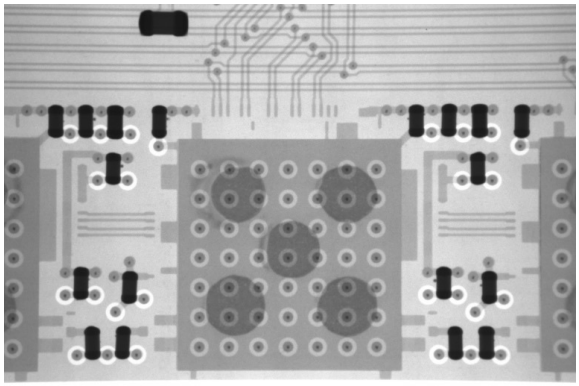

Figure 8. X-ray picture of an ASIC glued onto an upper-left hybrid in the common readout scheme.

In addition, height measurements are performed to monitor the thickness of the glue. Figure 9 shows the measured thicknesses for a number of hybrids built for the split readout scheme. These are measured to be on average 80 μm with a spread of up to 40 μm, which is within the design specifications for the hybrids. The different glue heights for the different chips of a given hybrid type can be explained by the non-planarity of the pickup-tool or the vacuum jig.

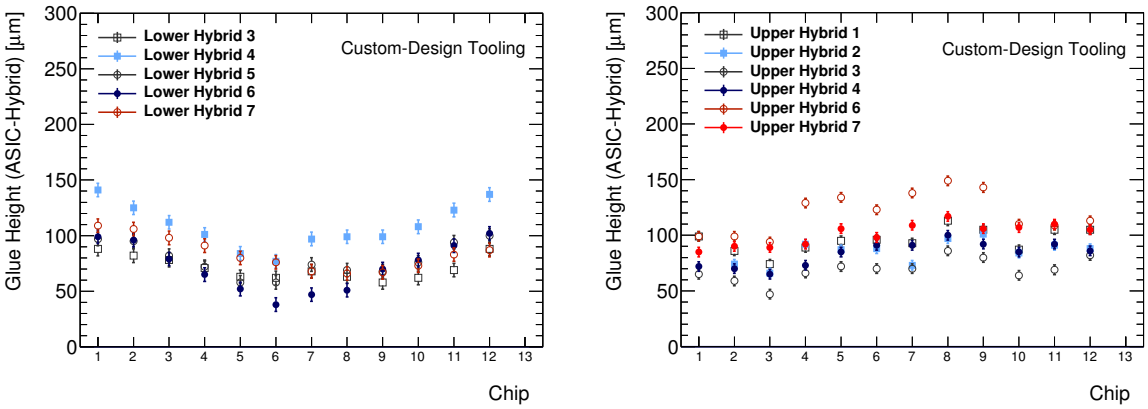

Figure 9. Measurements of the thickness of the glue for chips of a number of lower (left) and upper (right) hybrids in the split readout scheme. Chips 1 to 6 correspond to chips on the lower row of one hybrid, while chips 7 to 12 correspond to the upper row.

2.2.2 Flip-chip assembly method

This method was used for the production of the first hybrids in the common readout scheme since it does not require any custom-made tooling. In this procedure, glue is deposited on the PCB and the chips are placed by means of a flip-chip machine that applies controlled force to preserve the desired thickness of the glue. The deposition of the glue is done in two steps. First, some glue is spread over a turning plate. The thickness of the glue layer over the plate is controlled by an arm held a fixed distance from the top of the plate, such that rotating the plate results in a uniformly thick layer of glue. When the glue has been spread, the turning plate is stopped. A stamping tool is attached to the flip-chip machine and used to dip into the glue and deposit a known amount on a

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hybrid PCB, drawing the desired pattern. Tests with glass chips were carried out to determine the best glue pattern. These tests aimed to find the pattern covering the largest area while avoiding any overflow of glue. Two sizes of stamping tool as well as several glue layer widths on the plate were tested. Test PCBs and glass ASICs are used to evaluate the glue spread depending on the stamping tool size used to deposit the glue, the width of the glue layer on the turning plate and the number of dots in the glue pattern. The option of a 3×3 dots matrix using a 2 mm stamping tool with 1 mm width of glue on the plate was chosen by evaluating the glue tests by visual inspection. The left-hand side of figure 10 shows a test PCB with glass ASICs glued using the nine-dot pattern. An upper-left hybrid PCB with the conductive glue pattern is shown in the right-hand side of figure 10.

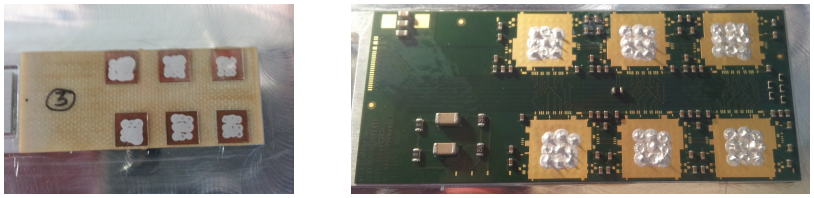

Figure 10. Photos of test PCBs and glass ASICs to evaluate the distribution of the glue (left) and of a nine-dots glue pattern deposited using a flip-chip machine on an upper-left hybrid (right).

Once the glue is deposited on every footprint, the flip-chip machine is used as a very precise pick-and-place machine. The cartridge of the flip-chip machine is changed, and a vacuum pick-up tool is mounted. Using this tool, the chips are picked and accurately positioned in their place by visual inspection using a camera. Finally, the chips are cured at room temperature for a nominal curing time of 24 hours. The force for picking the chips (70 g) and placing them (85 g) is programmed and controlled by the flip-chip machine. Measurements of the thickness of the glue show good uniformity among the chips of a given hybrid, as can be seen in figure 11. The dispersion of the thickness is controlled within $\pm 10\,\mu$m and is reproducible. This method proved to be valid for prototyping. Its main advantage is the possibility of producing a large amount of different hybrids in a chain without the need of having many sets of specific building tools. However, its main drawback is the time taken since the program is not automatised.

2.3 Electrical tests of hybrids

After the hybrids are equipped with all active and passive components, they are electrically tested to certify their full functionality and quantify their performance. The test setup and the test procedure are described in the next section, followed by a discussion of the test results for all hybrid types.

2.3.1 Test procedure

Specific PCBs, referred to as test frames, have been developed for all hybrid types. They allow for single hybrid testing as well as for the testing of a full module. Both the operation and detailed characterisation are performed as described in the following.

For the split readout scheme design, a test frame was constructed allowing the connection of both types of hybrid. To test the hybrids, the electrical interface from the edge of the hybrids is passively converted to pluggable connectors. For this purpose the test frame is used with wire-bond pads matching the ones on the edge of the hybrid and with large enough pad sizes to allow for

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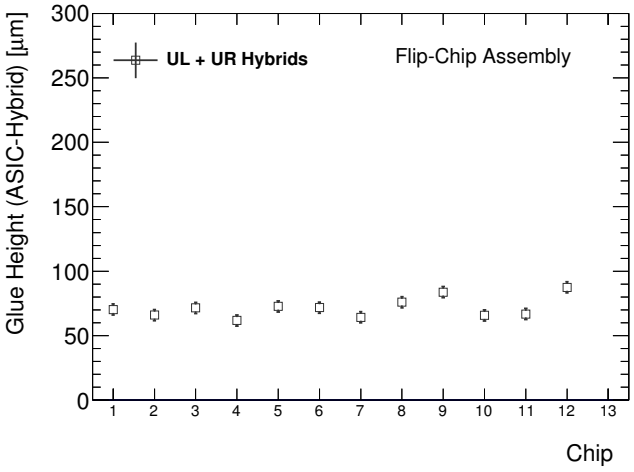

Figure 11. Measurements of the thickness of the glue for chips of two hybrids (one upper-left, UL and one upper-right, UR) in the common readout scheme glued with the flip-chip method. The chips 1 to 6 refer to the two rows of chip on the upper-left hybrids, while the values for chips 7 to 12 give results of the chips of the upper-right hybrid.

multiple bonding. The connections are then routed to four connectors, of which one connects to a daughter card providing power. Another one connects to a daugther card providing LVDS buffering. A third connector is used to directly access the temperature sensor located on the hybrid to monitor its temperature. The fourth connector functions as a jumper, allowing options on the ASICs to be configured, such as shunt operation or the communication clock speed. Additionally, an optional board for high voltage supply can be connected to the low voltage board. A photograph of a lower hybrid in a test frame is given in figure 12. It shows also the different readout boards and the frame mounted on an aluminium jig which allows cooling. The hybrid is fixed in its position by applying vacuum. The LVDS-buffer card is used to buffer the high-speed LVDS signal to and from the ASIC, such that they can be transferred over ∼1 m long flat-ribbon cables to the readout electronics, the HSIO data aquisition board. It also hosts a transceiver for buffering [11]. The low voltage board houses a low pass filtering circuitry and provides power to the test frame, which then routes it to the hybrid and the LVDS connector. The power board is connected to two laboratory-power supplies, which provide the operating voltage for the ASICs and the LVDS buffers.

The basic test consists of verifying the connectivity with all the chips on the hybrid by requesting their addresses. Damaged or incorrectly wire-bonded ASICs are detected in this step.

Since the ASICs are connected in a daisy chain, a failing chip makes it impossible to read out the complete stream. In other cases of failure, the chip does not receive the clock signal or configuration and consumes too little or too much current. Chips that, due to gross failures, draw an anomalous current can also get detected via thermal images. In figure 13, the measured temperature distribution (without any emissivity corrections) is shown for a faulty lower hybrid in the common readout scheme. It can be seen that the fourth chip in the upper row of ASICs has a higher temperature than the others, while the sixth one shows a lower temperature. Faulty chips can be replaced manually.

After the basic communication to the ASICs is assured, further tests are carried out using an HSIO data aquisition board that provides the computer interface. The quantities of interest, like the

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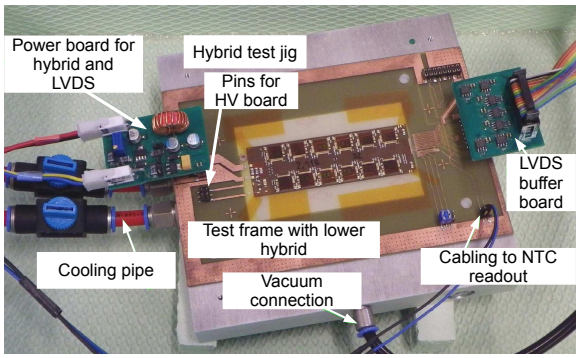

Figure 12. Photograph of a lower hybrid in the test frame in the split readout scheme. Various boards for readout and powering are also shown. The frame is mounted on an aluminium jig allowing cooling of the device under test. The hybrid is fixed by applying vacuum.

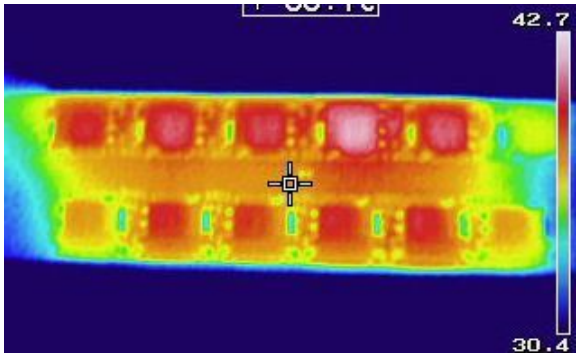

Figure 13. Distribution of the temperature (in °C) across a lower hybrid in the common readout scheme (without any emissivity corrections). The fourth (sixth) chip in the upper row shows a higher (lower) temperature than the others.

noise behaviour, gain and signal readout, are characterised and evaluated for every channel using threshold scans in a binary read-out architecture. In the threshold scans, the number of hits at a fixed injected charge versus the discriminator threshold voltage is recorded. This procedure is repeated for different values of the threshold voltage using 200 injected charge signals for each threshold value. Before conducting threshold scans to obtain noise and gain, the logical signal of all ASIC channels and the clock of the readout system have to be synchronised in a so-called *iDelay-Test*. To set the correct timing offset between the charge injection and the readout clock, a so-called *strobe delay* scan is performed. The occupancy curve (number of hits above threshold as a function of threshold) is recorded for each channel at a given injected charge. Due to noise contributions it is not a delta function but widened by a Gaussian distribution, resulting in a so-called s-curve. The output noise is extracted from the width, which determines the noise amplitude at the discriminator output. The 50% occupancy point of the s-curve ($vt50$) for various injected charge values leads to a so-called *response curve* for ten charge values and 3-*point gain curve* for three charge values.

The gradient of the response curve corresponds to the gain of the channel. It is expected to be around 100 mV/fC for both types of hybrids. The input noise in ENC (equivalent noise charge) is calculated by dividing the measured output noise by the gain. It corresponds to the noise at the input

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of the discriminator for every channel and is expected to be around 400 ENC without any sensor connected for the ABCN250. At the beginning an additional scan is possible using the internal trim circuitry of the ASICs. The aim is to obtain a uniform $vt50$ distribution for all channels. The results on input noise for hybrids and modules, presented in the following, show the average input noise in ENC as determined by fitting a Gaussian to the noise distribution for each channel of the respective readout chip. The uncertainty on the mean noise per chip in ENC is taken to be the standard deviation σ as determined in the Gaussian fit. Similarly the gain for a specific ASIC is determined by fitting a Gaussian to the gain distribution of the 128 channels of a specific chip and the Gaussian width is taken to be the uncertainty.

Additional tests were conducted in which the power was not directly fed from the power daughter board to the hybrid, but rather through an SM01C DCDC converter. This DCDC converter will also be used on the petalet to power the hybrids. Consequently, the proper operation of this setup has to be verified on the single hybrid level. When using the DCDC converter no degradation of the noise performance was detected. Thus, further single tests for hybrids in the split readout scheme were done by directly powering the hybrid by a laboratory power supply. In the tests for hybrids in the common readout scheme the DCDC converters were partially used.

2.3.2 Test results for hybrids in the split readout scheme

The input noise in ENC and its stability for seven lower and eight upper hybrids, respectively, are shown in figure 14. The average input noise in ENC typically amounts to 380 ENC per ASIC and can be reproduced reliably for the assembled prototype hybrids. The uncertainty gives an idea of the uniformity of the ENC noise of the different channels of an ASIC and is on average around 20–30 ENC. As demonstrated in figure 14 an average input noise of 380 ± 25 ENC is valid not only for the different readout chips on the same hybrid, but also for all hybrids of a specific type (lower or upper) and lastly, also for different hybrid types.

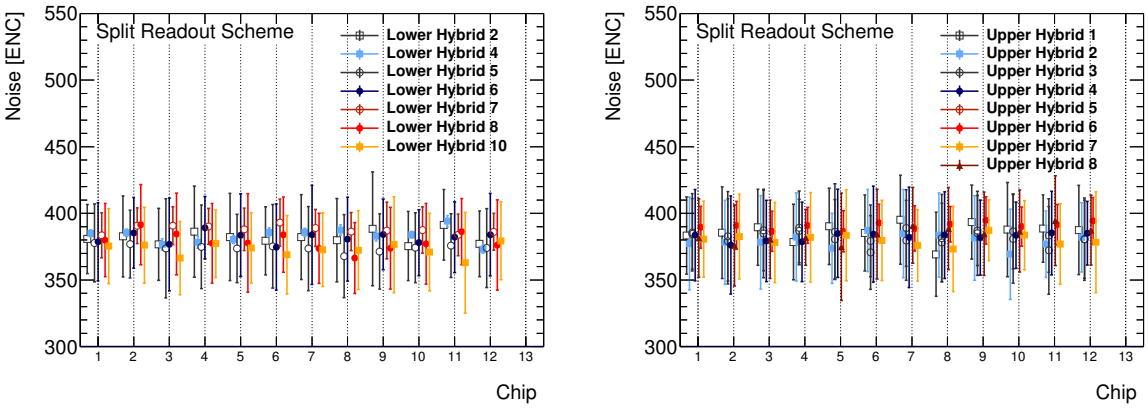

Figure 14. The measured noise in ENC for seven lower (left) and eight upper (right) hybrids for twelve ASICs (ASIC number on the x-axis) in the split readout scheme. The noise values have been averaged for all 128 channels of each chip for a specific hybrid using a Gaussian fit, whose width is taken as the uncertainty.

The gain and its stability for seven lower and eight upper hybrids, respectively, are shown in figure 15. The gain is found to be around 100–105 mV/fC and very uniform over the different chips and hybrids. The spread of the gain for the different channels of a chip is around 1 mV/fC, and

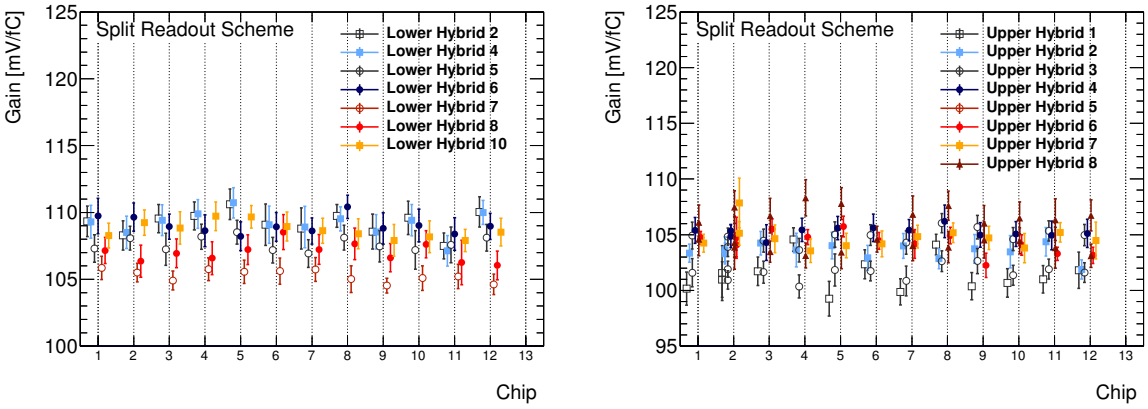

Figure 15. The measured gain for seven lower (left) and eight upper (right) hybrids for twelve ASICs (ASIC number on the x-axis) in the split readout scheme. The gain values have been averaged over all 128 channels of each chip for a specific hybrid using a Gaussian fit, whose width is taken as the uncertainty.

is comparatively much smaller than the spread of the noise. The reason is that the channels have been trimmed to obtain a uniform *vt50* distribution as explained above, which causes the gain to be uniform as well.

To further investigate the stability of the hybrid performance, the environmental conditions (i.e. the temperature of the cooling chuck and the humidity) were varied. Figure 16 displays the results of these tests for three selected ASICs of two lower hybrids. Within a humidity range from 15% to 55% and a temperature range from 5°C to 35°C, the noise level stays constant within the uncertainties. No strong correlation between the humidity and temperature values is observed in these measurements. The relation between the chuck and the hybrid temperatures is found to be linear as described later in section 3.2.1.

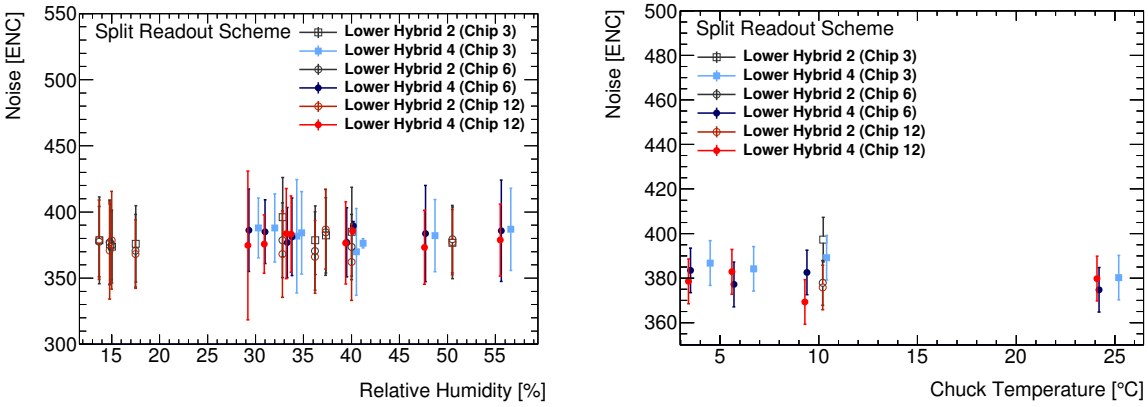

Figure 16. The measured noise in ENC for three given ASICs on two lower hybrids in the split readout scheme as a function of humidity (left) and chuck temperature (right).

2.3.3 Test results for hybrids in the common readout scheme

The results for hybrids in the common readout scheme are summarised in figure 17. All measurements were done with the chiller set to 6°C (resulting in hybrid temperatures between 20°C and

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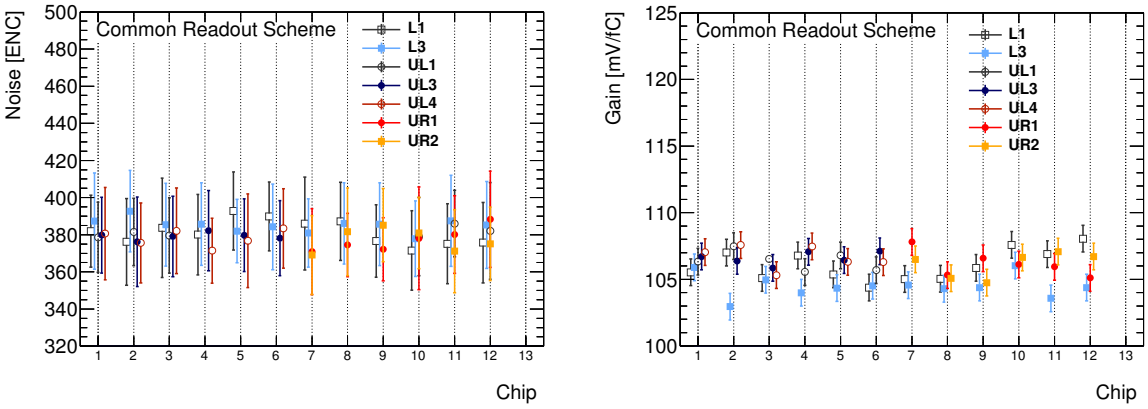

Figure 17. The measured noise in ENC (left) and gain (right) for several lower, upper-left and upper-right hybrids in the common readout scheme. The values have been averaged over all 128 channels of each chip for a specific hybrid using a Gaussian fit, whose width is taken as the uncertainty.

30°C) and for the humidity in the range between 19% to 25%. For the common readout scheme, the input noise values are in the range from 365 ENC to 400 ENC, again with a spread of about 20–30 ENC per chip (see figure 17, left). The values for the gain are in the range from 103 mV/fC to 108 mV/fC, independent of the hybrid type or the chip (see figure 17, right). Again, the values over a given ASIC are particularly uniform, with a spread of ~1 mV/fC.

In conclusion, the noise and gain measurements show a similar performance for both hybrid layouts.

3 Development and investigation of modules

Modules consist of n-in-p silicon strip sensors and hybrids. N-in-p strip sensors in wedge-shapes have been produced for the petalet modules at Centro Nacional de Microelectronica (IMB-CNM, CSIC), Barcelona, Spain. The substrates used are high-resistivity, Float-Zone silicon wafers with 300 μm thickness [5]. For test purposes, some of these sensors have embedded pitch adapters, where a second metal layer is used in order to integrate the signal routing to the ASICs into the sensor [12]. This leads to slightly different positions of the bond-pads on these sensors, facilitating the wire-bonding. The strips are AC-coupled to the readout. Detector modules are built by glueing assembled hybrids onto the silicon sensors and establishing electrical connections using wirebonds. In the following, the assembly of lower and upper modules in both readout schemes is described and the precision achieved is quantified. Moreover, results from electrical tests of all module types are presented and discussed.

3.1 Module assembly

The leakage current of the silicon sensors is measured before assembly into a module; only sensors exhibiting the expected depletion voltages of around 50 V and leakage currents of 0.6 mA/cm^2 or less at a bias voltage of 200 V are used. In addition, only hybrids with acceptable noise and gain values as given in section 2.3 are selected.

The basic assembly process is similar for all module types and deploys custom-design tools.

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In order to achieve sufficient positioning precision for the components, hybrids and sensors are placed on custom-made precision jigs using positioning pins for alignment. On these jigs, parts are kept in stable positions by applying vacuum. In figure 18 two tools are shown for the assembly of modules in the split readout scheme. The figure displays the module-building jig for sensor positioning (left) and the hybrid-glueing jig with one assembled lower hybrid in the split readout scheme (right). This jig is also used in the module assembly step for aligning and picking up the hybrid with the pick-up tool. Both, the module and the hybrid are positioned by pushing them towards three alignment pins.

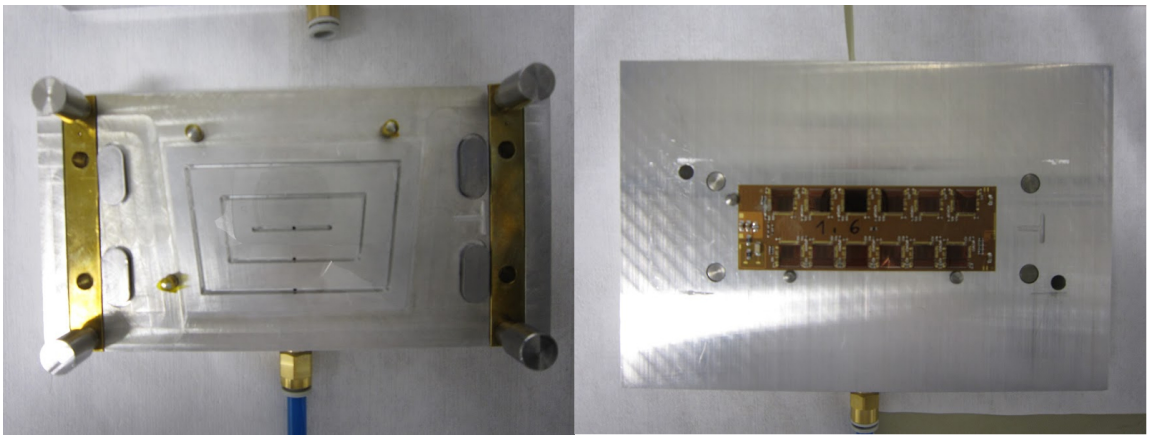

Figure 18. Photo of the module-building jig for sensor positioning and assembly of lower modules in the split readout scheme (left). Brass inserts on the left and right allow for different positions of the hybrid on the sensor. Photo of the hybrid-glueing jig with an assembled lower hybrid in the split readout scheme that is ready to be picked up with the tool (right).

Using the same pick-up tool as employed during the hybrid assembly (see section 2.2), the hybrid is picked up from the glueing jig and held with vacuum. The pick-up tool is placed on the holder with the hybrid turned upside down in order to apply glue on its back-side. For glue application, a steel stencil with a thickness of 250 μm is positioned on the hybrid and the glue Epolite FH-5313A [13] is spread (see figure 19). The stencil is removed and the pick-up tool with the hybrid is placed accurately on the sensor by means of the positioning pins on the pick-up tool. The glue is cured at room temperature for a minimum of six hours. The distance between sensor surface and hybrid back-side is calibrated before glueing using steel micro screws in the pick-up tool. After glueing, the ASICs and the sensor are connected electrically by wire-bonding the readout channels of the ASICs to the bond-pads of the sensor using an automatic wire-bonding programme. A photo of a fully assembled lower module in the split readout scheme is displayed in figure 20.

While the general assembly process is the same for all types of modules in both readout schemes, differences in the module geometry lead to subtle differences in the assembly steps for the two schemes.

A higher degree of relative alignment of the two sensors is necessary, when upper modules are built in the split readout scheme. In order to optimise the precise alignment, various upper modules in the split readout scheme have been built using either an xy-tilt stage or a shim to introduce the required 500 μm distance between the two sensors. Both methods have shown to result in

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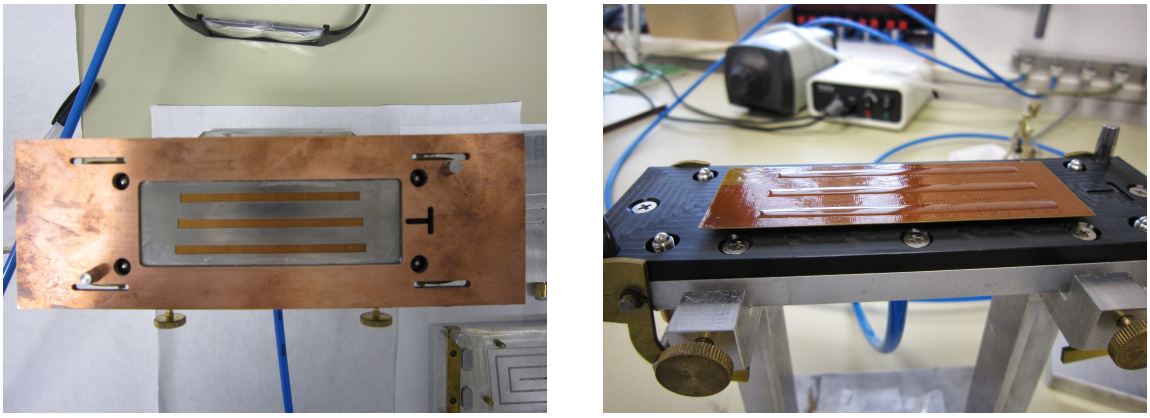

Figure 19. Photo of the pick-up tool with hybrid and stencil for glue application on top of it (left). After the application of glue and removal of the stencil, the glue pattern is visible on the back-side of the hybrid (right).

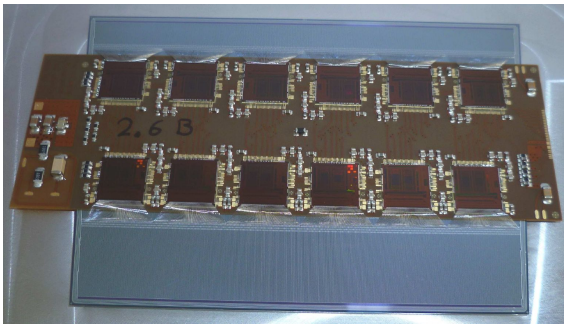

Figure 20. Photo of lower module without embedded pitch-adapters in the split readout scheme. ASIC channels and silicon strips are connected with wirebonds.

variations in height of less than 10 μm. However, this technically challenging alignment is very time-consuming and has led to the recommendation not to build upper modules with one hybrid and two sensors in future prototyping.

For the common readout scheme the assembly tools are designed in a very similar way. Here, the two upper modules are separated and therefore can be built in two separate assembly steps. It was also demonstrated that they can be assembled in one process, using a single pick-up tool and a single building jig that is designed to hold two upper modules at the same time.

As discussed above, two sensor types (with and without embedded pitch adapters) with different bond-pad layouts and positions were considered for module building, leading to two different positions of the hybrid relative to the sensor. Module building jigs were therefore designed with exchangable brass inserts with positioning holes matching both sensor bond-pad layouts, as shown in figure 18 (left).

The positions of the ASICs relative to the sensor surface were measured to monitor the glueing process. Figure 21 shows measurements of the glue thickness for a series of modules in the split readout scheme. The anticipated thickness of the glue of around 100 μm was achieved. Height differences among ASICs on the same module were found to be correlated among different modules

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and can be attributed to the imperfect flatness of the plastic top layer of the pick-up tool used for glueing. The latter will be more relevant if for hybrid and module assembly different batches of tools are used.

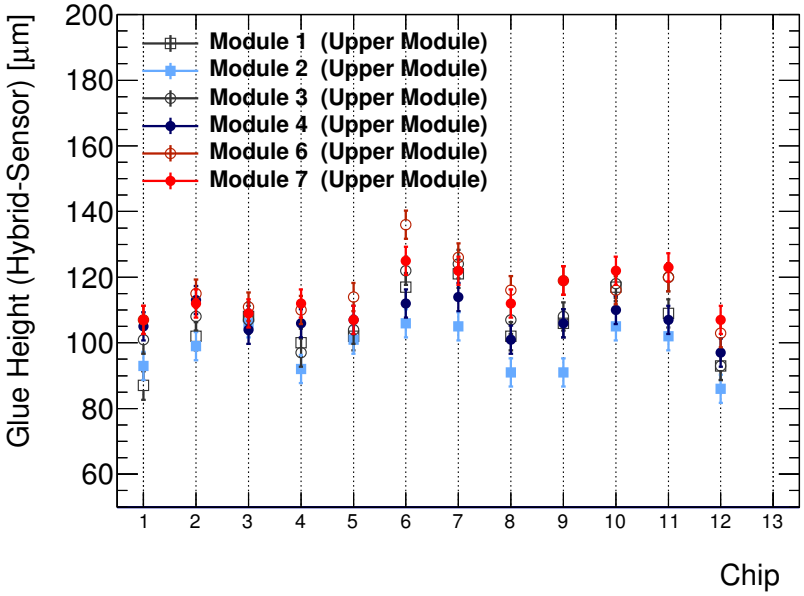

Figure 21. The average distance between the hybrid back-side and the sensor surface for all ASICs on various upper modules in the split readout scheme. The chip numbering is as follows: chips 1 to 6 are the lower row of chips on one hybrid, chips 7 to 12 correspond to the upper row of chips.

Moreover, it was shown that modules built with sensors with embedded pitch adapters have about 0.009% failed wirebonds, while for modules with the standard sensor design this number is slightly higher. About 0.025% of channels were found to be unconnected after this step. In addition, large angles can short-circuit neigbouring strips in case the wirebonds touch each other.

3.2 Electrical testing of modules

The single modules are tested standalone in test frames and can be assembled in a later step on larger structures. Tests as conducted with hybrids are also carried out for the characterisation of modules. In order to perform the electrical tests, the module is placed inside a light-tight Faraday cage and mounted onto a test jig. A flow of dry air or nitrogen reduces the humidity in order to keep the dew point significantly below the module temperature to prevent condensation when cooling it down.

The module test jig is provided with cooling pipes, connected to a chiller, for cooling of the sensor and the electronics. The jig also allows to hold the detector with vacuum, improving the contact to the backplane to provide the bias contact and to enhance electrical and thermal conductivity. A good ground connection to the aluminium jig is crucial in order to reduce noise. In case a DCDC converter is used, it is wrapped in a copper foil to reduce noise due to interference effects.

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3.2.1 Results for modules with hybrids in the split readout scheme

A total number of 18 upper and 21 lower modules in the split readout scheme have been built, including sensors with and without embedded pitch adapters. Figure 22 shows an upper module in the split readout scheme in its test frame.

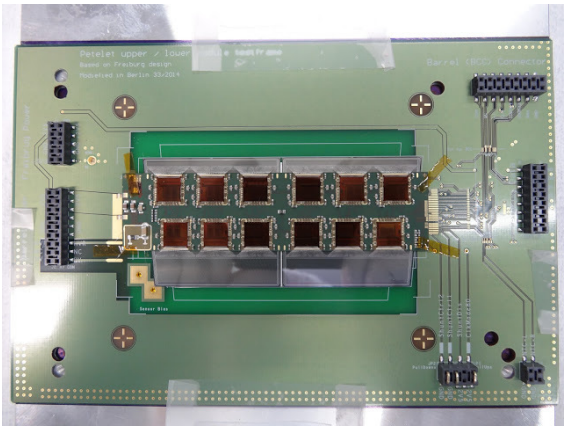

Figure 22. Photo of an upper module in the test frame in the split readout scheme. Connectors are provided for biasing, powering as well as for temperatue and data readout. In addition, jumpers can be set to change the readout mode.

While the noise values for this readout scheme vary between 380 ENC and 400 ENC for single hybrids, they are found to be in the range from 520 ENC to 600 ENC for modules with sensors without embedded pitch adapters and around 700 ENC for modules with sensors with embedded pitch adapters after full depletion at a bias voltage of 70 V. This can be seen in the left-hand side of figure 23. The additional noise observed in modules compared to hybrids results from the additional capacitance of the silicon sensor. The increase of the noise for sensors with embedded pitch adapters is attributed to the second metal layer, which adds an extra capacitance. Details can be found in ref. [14]. The noise behaviour is measured to be uniform across all ASICs of a hybrid or module, respectively. The measured noise values agree with the expectations from calculations. The gain for several hybrids and modules is displayed on the right-hand side of figure 23.

Figure 24 shows the noise dependence on the applied bias voltage. As expected it decreases as the sensor depletes. In addition, modules were tested at different temperatures. A small dependence of the noise on the temperature was observed, corresponding to two electrons (ENC) per degree for unirradiated modules. Figure 24 (right) shows the corresponding measurement at a bias voltage of 70 V. A stable and comparable performance was measured in the temperature range the tests were performed in. The relation between chuck and hybrid temperatures is linear as displayed in figure 25. Measurement for hybrids are only provided at values around room temperature resulting in a limited number of data points for hybrids. In addition, a potential hysteresis effect in the noise was studied by comparing a ramp-up from 0 to 250 V with a ramp-down over the same voltage range. No significant effect has been observed.

Since modules are foreseen to be assembled on a carbon core where they are readout using an additional ASIC for multiplexing of data, they were also tested in a test frame using this multiplexing ASIC with results fully in agreement with single-module readout.

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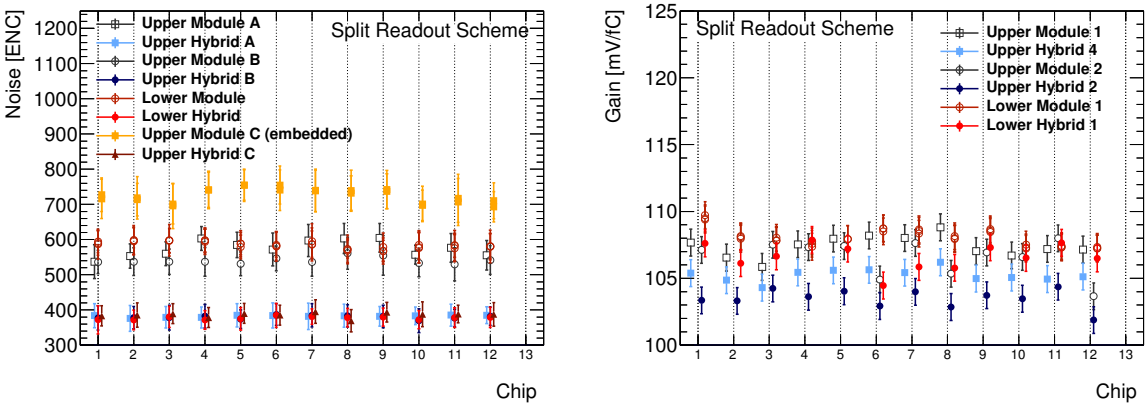

Figure 23. The measured noise in ENC (left) and gain (right) of each chip of hybrids and modules in the split readout scheme. The values are averaged for all channels on each chip for a specific hybrid/module using a Gaussian fit, whose width is taken as the uncertainty. "Embedded" denotes that the sensor has an embedded pitch adapter while all other sensors do not. The bias voltage is set to 100 V for the sensor with embedded pitch adapters and to 70 V for the others. Both voltages are above full depletion. The gain values have been averaged over all channels on each chip for a specific hybrid/module using a Gaussian fit, whose width is taken as the uncertainty.

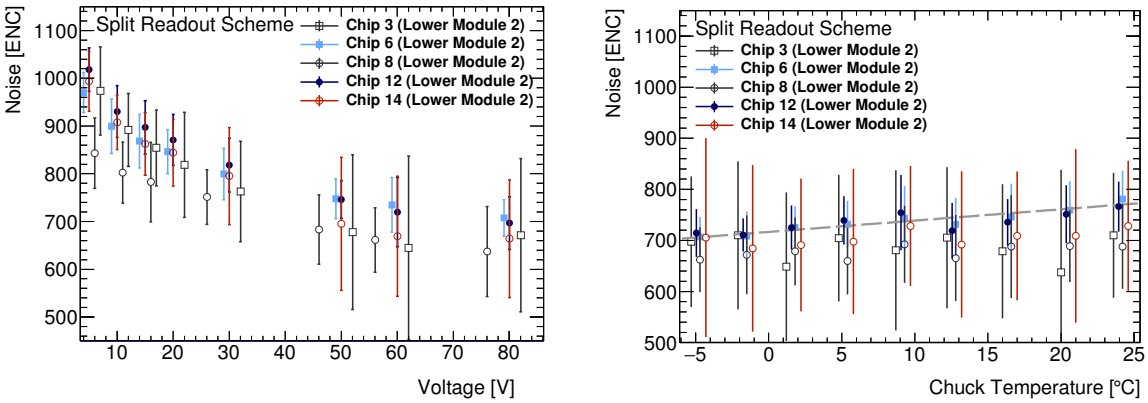

Figure 24. The measured noise as a function of the bias voltage for several ASICs of a lower module in the split readout scheme at a temperature of the test frame of T = 16.3°C (left). The noise for five ASICs of a lower module for varying chuck temperatures at a bias voltage of 70 V (right). For better visibility, the respective x-values of different ASICs have been shifted by 1–3% around the applied bias voltage/temperature value. Data points of chip 3 were linearly fitted.

3.2.2 Results for modules with hybrids in the common readout scheme

In total four upper modules (two left and two right ones) and two lower modules have been assembled in the common readout scheme. The results of the electrical tests are depicted in figure 26. The gain and noise behaviour of the modules (a lower LM1, an upper-left ULM1, an upper-right URM1) and of the hybrids (a lower L1, an upper-left UL3, an upper-right UR1) before being glued to the sensor are shown. The values are averaged per ASIC and the chiller was set to 6°C during these measurements resulting in hybrid temperatures between 20°C and 30°C. It can be seen that the presence of the sensor increases the input noise due to the input capacitance of the strip sensor.

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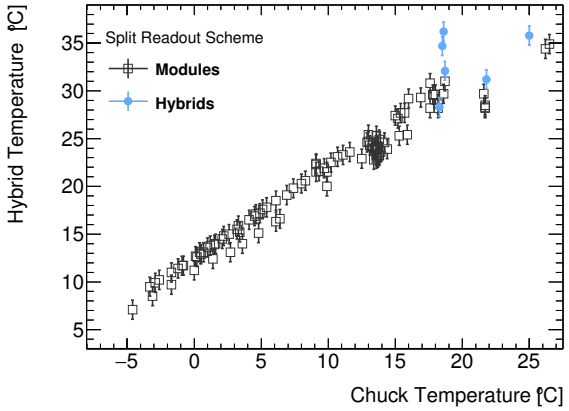

Figure 25. Relationship between the hybrid and chuck temperatures for a number of measurements on hybrids and modules in the split readout scheme.

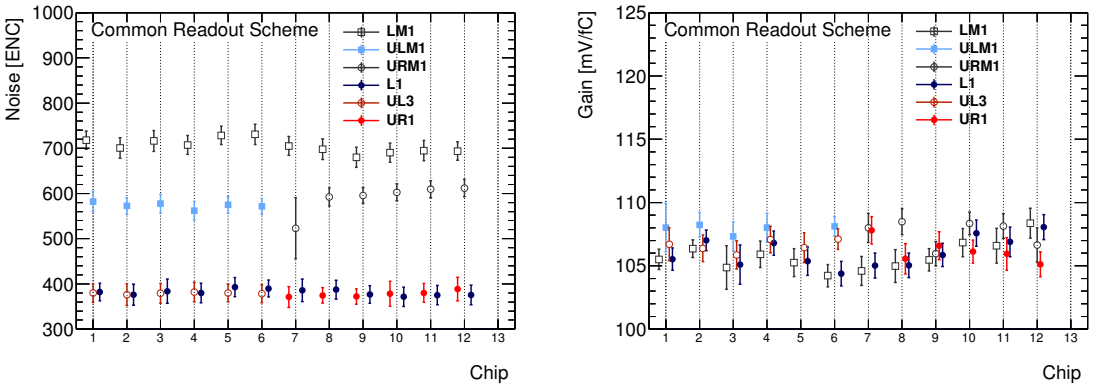

Figure 26. The measured noise (left) and gain (right) of each chip of hybrids and modules in the common readout scheme. The results are given for a lower (L1), an upper-left (UL3), an upper-right (UR1) hybrid and a lower (LM1), an upper-left (ULM1), an upper-right (URM1) module, respectively. The values are averaged for all channels on each chip using a Gaussian fit, whose width is taken as the uncertainty. Results are shown for three different modules and for the corresponding hybrids before being glued to the sensor.

While the input noise varies around 380 ENC for the hybrids, it ranges from 550 ENC to 750 ENC with an uncertainty of ±30 ENC for the assembled modules.

3.2.3 Comparison of readout schemes

No large differences in the noise performance have been observed between the two readout schemes for both hybrids and modules. A comparison can be found in table 1. Both schemes deliver adequate signals and can be read out. Their long-term behaviour was also tested by operating them for 24 hours. During these tests a stable and comparable performance was measured for both layouts. Detailed irradiation tests of the hybrids and modules have not been performed. However, the hybrids and sensors are expected to be radiation-hard under the HL-LHC conditions [15]. More detailed irradiation tests are planned with close-to-final components. Moreover, during operation the modules will be cooled down in order to prevent thermal runaway to occur in the sensors after irradiation. For this purpose the detector system will be cooled with CO_2, aiming for a coolant

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temperature of T = −35°C. It could be shown that modules perform well in the tested temperature range between T = −5°C – +20°C. In order to assure mechanical stability as well as full functionality of the modules after cooling down, tests with thermocycled components are foreseen. Individual components of the modules, like glue behaviour were already tested successfully cold [10].

Table 1. Comparison of averaged noise values of several hybrids and modules of both readout schemes. Modules of both schemes have noise values with similar uncertainties of ±30 ENC.

Readout scheme	Noise of hybrid [ENC]	Noise of module [ENC]
common readout scheme	380±20	550–750
split readout scheme	380±25	520–700

4 Conclusion

In the course of an R&D project in the framework of the development of the forward region of the silicon strip detector of the ATLAS experiment for the Phase-II upgrade, highly performing hybrids and modules were successfully developed, built and tested in two readout schemes. The petalet project aimed at evaluating the two readout schemes and demonstrating the feasibility of the components deploying ABCN250 chips. This was achieved and in total more than 40 fully functional modules have been built and evaluated at five institutes in the split readout scheme and in the common readout scheme. The assembly processes are well controlled and fully applicable to hybrids and modules with ABC130 chips. Differences in the number of hybrids per module, channels and wire-bond pads might have influence on the production yield, however not on the assembly method. Moreover, a flip-chip assembly method was evaluated and it was found that it is only applicable with glues of shorter curing time than the silver epoxy glue used in this study. Such glues are foreseen for petals.

The presented results of electrical tests show that noise levels of hybrids are uniform and values are close to the theoretically expected value of 380 ENC for the ABCN250 for all module types and readout schemes. Electrical tests of modules were performed at a bias voltage above full depletion and at room temperature. They result in noise values between 520 ENC and 750 ENC. The differences between modules are mainly attributed to differences in the sensor performance. The results compare well to the expectation as well as to corresponding results from the barrel part of the strip detector prototyping, where the noise values (with sensors of slightly longer strip lenghts) range around 650 ENC [6]. An important results of the petalet programme is that both readout schemes are fully functional with reasonably low noise. The institutes gained valuable experience in assembly and testing for future prototyping of components for petals.

For petals, it is suggested to modify the design of double modules, containing individual hybrids per sensor with internal lines routed to the surface and an electrical connection via wire-bonds between the two modules. This is mainly due to the time-consuming and technically challenging assembly of modules with the hybrid bridging across two side-by-side sensors. The knowledge gained on hybrids and modules in this 250 nm-ASIC technology based prototyping step can be transferred to full petals, which include larger sensors and all different sensor geometries needed for the strip detector end-cap.

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Moreover, at this stage of the petalet programme several fully functional modules are available and can be assembled to full petalets. This will allow further investigations and studies on integration and system aspects.

Acknowledgments

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