Upgrade of the CMS Drift Tube electronics for the High Luminosity LHC

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Upgrade of the CMS Drift Tube electronics for the High Luminosity LHC

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Abstract: The High Luminosity LHC (HL-LHC) upgrade mandates a comprehensive overhaul of the CMS Drift Tubes (DT) electronics due to trigger rates surpassing current capabilities. Accordingly, a new DT electronics has been designed that not only overcomes the readout limitations but also, will allow to improve the performance of the muon barrel trigger system by increasing the resolution and reducing the fake rates. The on-detector part of this new electronics will continue to perform the time digitization of the DT chamber signals with the required 0.78 ns but will achieve factors closer to 10 in terms of integration, reducing the power dissipation by half. The core of this new on-detector electronics is the On-detector Board for DT (OBDT) board that will allow integrating up to 240 time digitization channels and forward them without data losses, with ~10 W of power consumption and operating under radiation environment. The backend system will be based in Advanced Telecommunications Computing Architecture (ATCA) boards and for the first time we have successfully implemented the DT trigger primitive algorithm capable of using the OBDT streamline data and performing the DT muon track reconstruction in the available latency and with very similar to offline resolution. The deployment of OBDTs in a sector of the CMS has allowed to obtain the first results that validate the new architecture and its performance. Rigorous testing procedures have been conducted to ensure the suitability of these systems for the demanding operating conditions of the HL-LHC, with a primary emphasis on functionality and reliability. This report outlines an innovative approach to DT electronics, promising enhanced performance in a challenging HL-LHC environment.

Keywords: Electronic detector readout concepts (gas, liquid); Large detector systems for particle and astroparticle physics; Digital electronic circuits; Front-end electronics for detector readout

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1 The CMS DT upgrade for HL-LHC

The existing CMS [1] Muon DT detector [2] is essential for identifying and measuring muons at the required precision and accuracy needed to fulfil the CMS physics program. Therefore, it must be guaranteed that its performance will be sustained at high luminosity at the HL-LHC [3]. On the one hand, there is a concern about the obsolescence of the legacy system, which is complex and has a high power consumption, and may not be radiation tolerant enough for the full duration of the HL-LHC. On the other hand, the expected trigger rates (Level-1 Accept) at which CMS is expected to operate will increase from present 100 kHz up to 750 kHz, and present readout system will not be capable to sustain this rate. The DT chambers themselves should however be able to stand the operation under HL-LHC and therefore, will remain untouched [4]. The DT on-detector electronics presently consists of up to 17 boards of several types, heavily interconnected and compacted in a very tight structure embedded into the CMS wheels. Present plan is to substitute this system with a simpler architecture that reduces complexity and power consumption and eases maintenance as a by-product.

1.1 A new architecture

In the proposed architecture there will be only one type of board: so-called On-detector Board for DT (OBDT), whose primary function is to perform temporal digitization of signals originating from the DT chambers and forward this digital information to the next level of the electronics chain. With the presently available high speed links, it will now be possible to send all of the DT chamber time stamps outside of the detector in a full streaming mode, even at the occupancies expected in HL-LHC. Therefore, the OBDT system will not perform any filtering and no loss of information is expected from this system. This full stream of data will be available to the trigger system at the maximum resolution (factor 12 with respect to present resolution), achieving performances that can only be obtained nowadays in the offline computing farm.

The OBDT system will be made of 830 boards to readout 172200 channels from the DT chambers. It will be made of two type of boards: OBDT-phi, in charge of digitizing the signals coming from the DT wires that measure the azimuthal ϕ coordinate in CMS, and the OBDT-theta, which will digitize the signals from the wires that measure the polar angle θ coordinate. The two boards have slightly different requirements. The most critical is because of the impossibility to extract all DT chambers. Therefore, OBDT-theta needs to maintain the legacy cables and connectors. In the ϕ view, however, the legacy cables that interconnect the DT chambers and the Minicrates will be replaced with new cables that shield each differential pair to minimize noise.

At the next level in the electronics chain, all the complex tasks will be carried in the backend system, which is where the high performance electronics is located outside of the radiation environment of the experimental cavern. This has several advantages: (a) the trigger algorithms can be developed to become more powerful, (b) constraints on the CMS data acquisition conditions (readout rate, latency) are removed from the on-detector electronics, and (c) the accessibility to the complex decision-making hardware is no longer a problem.

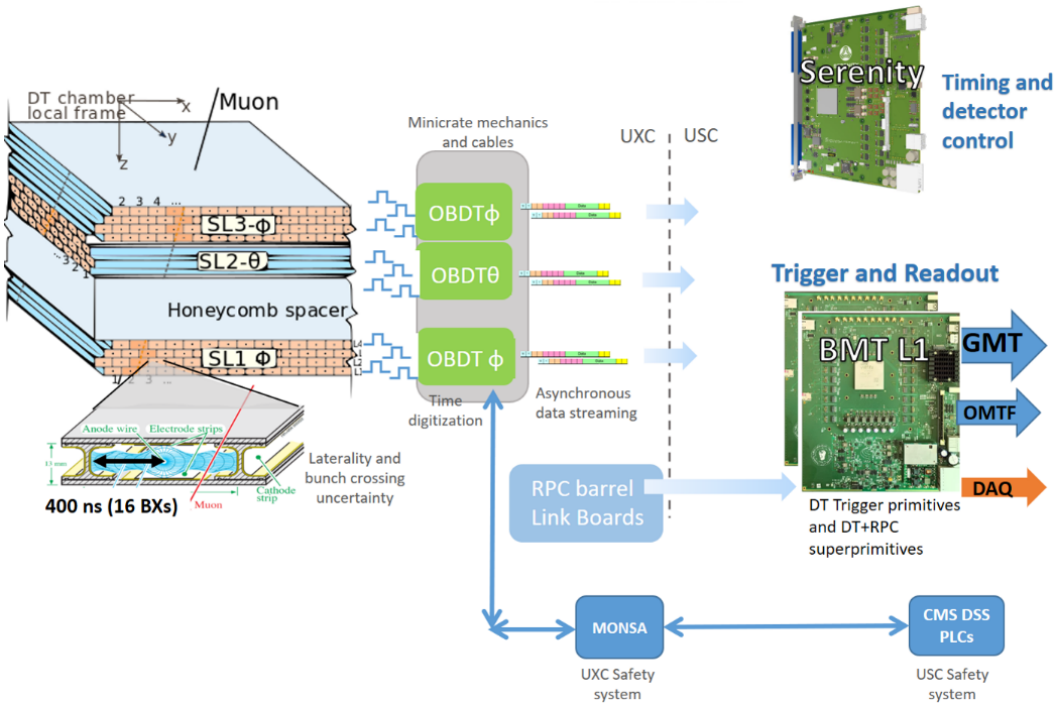

Figure 1. Diagram of the new architecture for the CMS Phase-2 DT systems that will be installed for operation during HL-LHC. GMT is the Global Muon Trigger system that receives the DT Trigger Primitives. DAQ refers to the Data Acquisition system that receives the readout data. DSS is the CMS Detector Safety System. UXC is the CMS experimental cavern and USC is the CMS Service cavern. BX refers to LHC bunch crossing which represents a unit of time of 25 ns.

The backend will be made of two systems: (a) timing and slow control and (b) trigger and readout system. The system (a) will oversee the configuration and monitoring of all OBDTs and also, of the precise distribution of the LHC clock and the fast commands. The system (b) will be in charge of performing the event building and the generation of the trigger primitives to reconstruct muon segment in the DT chambers. The system (b) will also receive the information from the RPC (Resistive

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Plate Chambers) muon detector and perform the readout of its hits and the construction of DT+RPC superprimitives [5] which profit from the characteristics of these two different muon detectors.

Finally, a safety system is also being developed to protect the OBDTs and as extension, the CMS detector. This system is made of different levels. Part of the protection is embedded inside the OBDT boards and detects over-voltages, over-currents and temperature increases, protecting the OBDTs accordingly. These faults are transmitted to a third backend, located in the tower racks MONitor for SAfety (MONSA) that re-transmit this information and has the possibility to also power off the OBDTs in case of an emergency.

The installation of all this new architecture will take place during the LHC Long Shutdown-3, which is expected in 2026–2029, right before the start of the HL-LHC phase. A diagram of the architecture of this new DT electronics chain can be seen in figure 1.

2 The OBDT boards

Both the OBDT-phi and OBDT-theta need to digitize the arrival time of the rising edge of the signals coming from the DT chamber front end electronics. These signals are generated by ionization when a muon crosses the DT cell, and after a drift time which can be up to 400 ns, they arrive to the DT anode wire. Since achieving a time digitization resolution in the order of 1 ns is beyond the DT cell resolution, a high integration implementation could be achieved by implementing the time digitization inside a Field Programmable Gate Array (FPGA). The method employed profits from using two input deserializers with a 640 MHz clock, one using the rising and the other the falling edge. By detecting the low to high level transitions, a time resolution of 25/32 (~0.78) ns can be achieved. This implementation in the Microchip Polarfire FPGA has allowed to implement 240 channels per FPGA in the OBDT-phi board (only 228 channels are needed in the OBDT-theta). The Polarfire FPGA has been selected because it has an excellent performance under the relatively mild radiation levels expected in the DT region where the maximum dose after 10 years of HL-LHC will be below 10 Gy.

The architecture of the OBDTs includes a communication path devoted to the clock reception, configuration and monitoring. This path is built around the LpGBT ASIC (Application-Specific Integrated Circuits) from CERN, which has been designed for much higher radiation doses and allows communication to the FPGA. The LpGBT is also connected to a SCA (Slow Control Adapter ASIC) from CERN which allows implementing several features such as: analogue to digital conversion of multiple voltage levels for voltages, current and temperature monitoring, generation of voltage levels required by the DT chamber and remote reconfiguration of the Polarfire FPGA through a serial peripheral interface. A secondary slow control link is built from the Polarfire FPGA directly, to have a redundant system.

After performing time digitization, the FPGA needs to funnel the information into one or several high-speed links for transmission to the backend. Up to 6 high speed links, that use the LpGBT protocol at 10.24 Gpbs, are output from the FPGA and sent through optical fibre using the VTRX+ optical transceivers from CERN.

Moreover, the OBDTs also include the safety circuitry that protects the system against over-temperatures, over-currents and over-voltages. Logic for generating timing calibration signals to the DT chamber is also included together with the several slow control interfaces required for the DT chamber operation.

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Both OBDTs are powered through two rails of 5 V and 3 V and the power consumption of each board is approximately 10 W, which will bring the power consumption of each chamber to ~40 W maximum, well below the 100 W presently required in the legacy system.

2.1 OBDT-phi

There is a total of 650 OBDT-phi boards in the detector which have been designed and produced by INFN Legnaro. They measure up to 240 DT chamber signals and are responsible of the generation of the bias and threshold voltages required by the DT chamber. They include embedded generation of the calibration signals for the DT ϕ view and auxiliary 1-wire interfaces for temperature sensors. The boards measure 280×90 mm and are made of 14 layers of halogen-free material EMC EM-890K. An image of this board can be seen in figure 2.

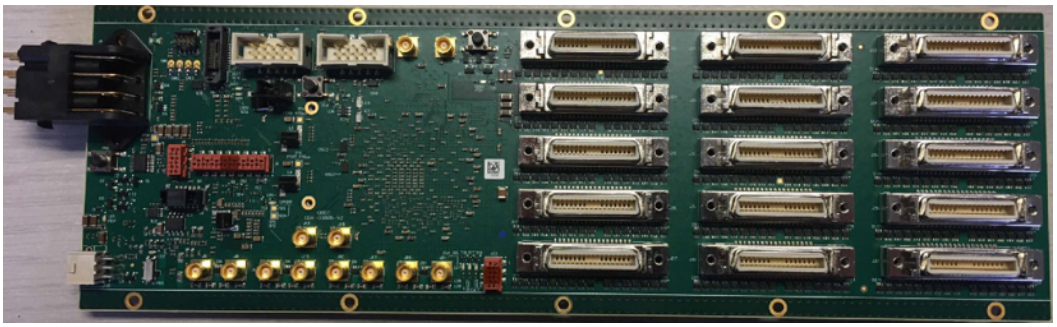

Figure 2. Image of an OBDT-phi board with the different connectors.

2.2 OBDT-theta

The OBDT-theta board has been designed and built by CIEMAT. Each OBDT-theta board digitizes 228 input channels, corresponding to the requirements of the DT chambers θ view and use the legacy 68 pins SCSI connectors.

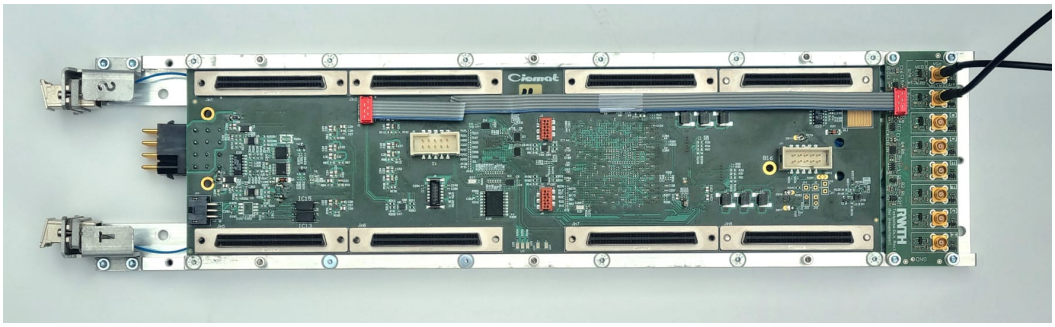

Figure 3. Image of an OBDT-theta and Testpulse-theta boards fixed to the mechanical frame that connects them to the Minicrate.

They have the same dimension as the OBDT-phi but are made of halogen-free Panasonic Megtron 6. They also include a water leak detection system and voltages monitoring but the generation of the calibration signals was built in a separate board, so called Testpulses-theta board which has been designed by RWTH (Rheinisch-Westfaelische Technische Hochschule) Aachen. An image of both boards attached to its frame can be seen in figure 3.

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3 The safety system, MONSA

The MONSA system has been designed and built by INFN Torino and implement a fully hardware solution to perform automatic actions. MONSA will be located in the tower racks on one side of the CMS wheels and they are in charge of multiplexing and demultiplexing the signals from the CMS central safety system to and from the OBDT boards following a pre-defined safety matrix. The system fulfills the functions to check the status (safe/alarm) of the OBDTs and set the control (active/cut) of each OBDT independently.

4 The backend system

The backend system will be located in the CMS underground service cavern, outside of the radiation environment and hosted in racks that have an active cooling through turbines and heat exchangers. The electronics hosted there will be built following the ATCA standard.

The timing and slow control system will perform configuration, control and LHC clock distribution to the OBDTs through the Serenity boards [6]. They are custom boards made by Imperial College which host an Virtex Ultrascale+ VU13P FPGA and up to 120 (receiver) RX and 120 (transmitter) TX optical links which can run at 16 Gbps.

The Trigger and Readout system will be implemented in the Barrel Muon Trigger Layer 1 board (BMTL1) [7], designed by University of Ioannina. This ATCA board is also built around a Virtex Ultrascale+ VU13P FPGA and contains 80 receiver optical links at 16 Gbps, 36 transmitter links at 16 Gbps and 40 bidirectional links at 25 Gbps.

Each BMTL1 board will receive the DT and RPC information from two CMS sectors, performing the data readout, matching to each Level-1 Accept trigger signal and forwarding to the CMS central data acquisition system. Furthermore, this board will generate the muon barrel trigger primitives (DT+RPC superprimitives), which will be later associated to build a muon track. The DT trigger primitives are built through the Analytical-Method algorithm whose firmware is ready and has been tested in the BMTL1 prototypes.

5 Validation of the new electronics

The different prototypes of the on-detector electronics have been tested in the laboratory and validated accordingly. The qualification of the electronics includes guaranteeing a reliable time digitization of all channels and uniform performance among them.

To validate the time digitization implementation in the FPGA, the Differential Non Linearity (DNL) has been measured by injecting random signals, non correlated with the operation clock, on each input channel. The results from these tests (figure 4) show that for a typical channel (left), the maximum deviation from the ideal flat case is in the order of 10% for any of the 32 bins. A see-saw pattern can be observed and this is attributed mostly to a non-perfect 50% duty cycle of the sampling clock signal.

In figure 4 right we can see the worst DNL measurement for all of the bins in all the 228 channels of the OBDT-theta board. As can be seen, all of the values are below 15% and most of them are at the 10% level. This proves that the time digitization errors achieved by this implementation are small and very similar to all of the input channels. This excellent performance guarantees that the time digitization errors that will be achieved with the new system will be well below any other source of uncertainty in the system.

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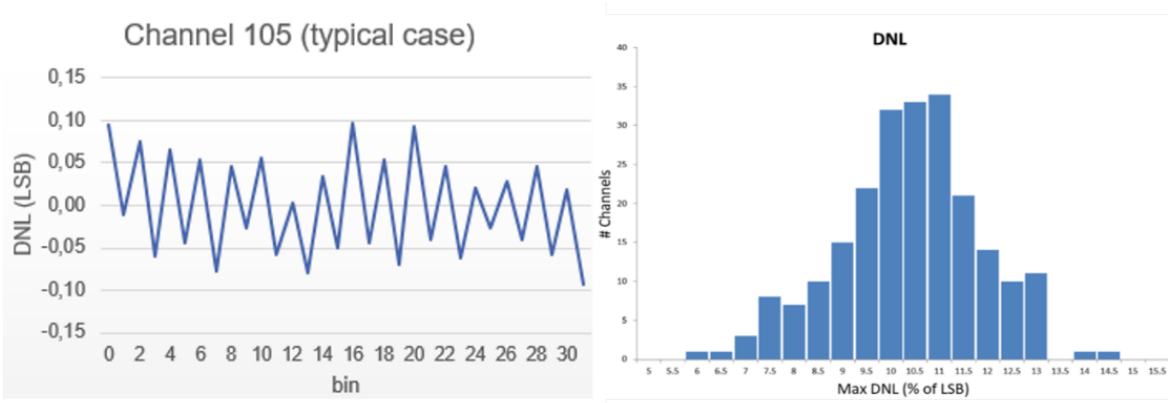

Figure 4. Left: DNL measurement of one channel in an OBDT-theta board versus the time bin. Right: distribution of the maximum DNL obtained in any bin for all the channels in one OBDT-theta board.

5.1 The CMS slice test

A full validation of the system has been performed at CERN, where two sectors have been instrumented with OBDT prototypes to be readout in parallel with the legacy system. The last sector, Sector 1 of CMS Wheel +2, includes prototypes of the full electronics chain (on-detector, MONSA and backend) that have been integrated and commissioned successfully. Achieving a fully operational system has allowed us to validate these electronics with real proton-proton collision data and operate it in similar conditions to those expected during HL-LHC, even though at reduced occupancies.

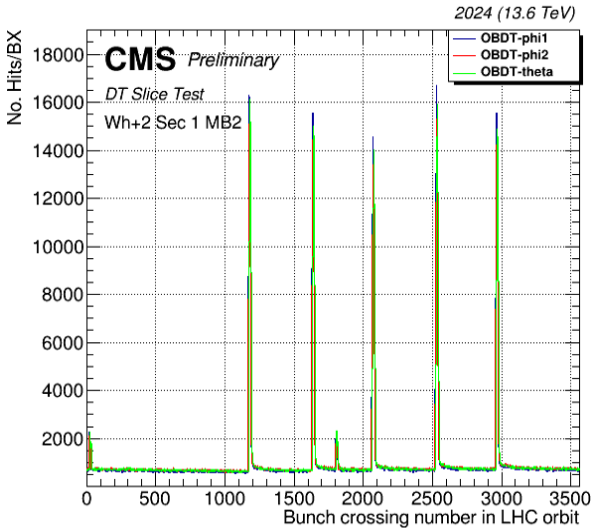

Figure 5. Distribution of the time measurements from the OBDT boards (phi and theta) installed in the CMS detector during proton-proton collision data taking. The time measurements are represented versus the LHC bunch crossing and the orbit structure is perfectly visible. In the plot label at the upper-left corner, the "Wh+2 Sec 1 MB2" indicates the Wheel +2, Sector 1 and Muon Barrel station 2.

Results from this setup under proton-proton collisions can be seen in figure 5 where the distribution of the time measurements from OBDTs-phi and OBDT-theta in one chamber of Sector 1 are plotted versus the LHC bunch crossing number. Data was taken with the CMS DT Slice Test in 2024

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proton-proton collisions at 13.6 TeV. No trigger was applied, all hits were streamed and collected asynchronously through the internal memories of the BMTL1 board.

The time distribution shown in figure 5 reflects, as expected, the LHC beam structure of the analysed fill, with 5 bunch trains of 12 colliding bunches (corresponding to higher peaks) each plus two single colliding bunches (corresponding to lower peaks). Flat background corresponds mainly to cosmic induced background.

The trigger algorithm inside the prototypes of the BMTL1 board was also operated during these data taking exercises and the performance of the track reconstruction was validated. Results from the time resolution achieved in the reconstruction of the new DT trigger primitives can be seen in figure 6. The resulting AM trigger primitive tracks are compared to the offline reconstructed segments and a difference better than 2 ns is achieved. This is to be compared to the 25 ns time bin that is obtained from the legacy system.

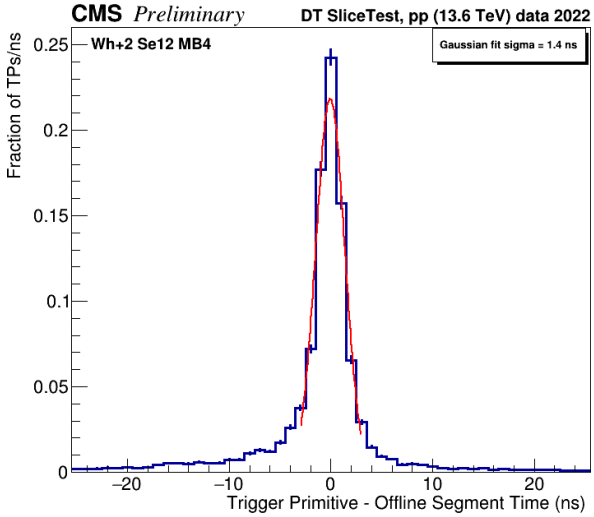

Figure 6. Difference between the measured time by the DT Trigger primitive generated in the trigger prototype boards and the DT offline reconstructed segment. As can be seen, the performance of both is very similar, although one is running in an FPGA within the L1A latency and the other in a computer farm.

6 Summary

A new electronics for the CMS Drift Tubes Phase 2 upgrade has been designed and fully operational prototypes have been built and validated through different tests both at the laboratories and at the CMS central facilities [8]. These new electronics will allow to ensure a reliable operation of the DT chambers throughout HL-LHC by removing present readout rates limitations, significantly reducing power consumption and moreover, will allow to achieve an offline-grade performance in the DT muon trigger system.

The performance of the newly designed OBDT boards show very adequate results, achiving a high integration while ensuring good and uniform time resolution through an implementation in a radiation tolerant FPGA.

A full installation of the DT electronics chain in the CMS detector has allowed to verify its safe and reliable operation in the final expected environment and has also provided very satisfactory results of the expected DT trigger performance under proton-proton collision data.

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The results that we have obtained are very satisfactory and has allowed to proceed with the final production in view of the installation on the CMS DT chambers.

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