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High Speed Digital TDC for DØ Vertex Reconstruction*

G.S. Gao† and Richard Partridge
Department of Physics
Brown University
Providence, RI 02912

Abstract

A high speed digital TDC has been built as part of the Level 0 trigger for the DØ experiment at Fermilab. The digital TDC is used to make a fast determination of the primary vertex position by timing the arrival times of beam jets detected in the Level 0 counters. The vertex position is then used by the Level 1 trigger to determine the proper $\sin\theta$ weighting factors for calculating transverse energies. Commercial GaAs integrated circuits are used in the digital TDC to obtain a time resolution of $\sigma_t = 226$ ps.

1 Introduction

The DØ detector, which is being built for use at the Tevatron collider, makes extensive use of transverse energy sums in its first level trigger. The $\sin\theta$ weighting factors used in these sums require knowledge of the interaction vertex position due to the large spread in the luminous region along the beam (z) direction: $\sigma_z \approx 30$ cm. Unless corrected for, the uncertainty in the vertex position will significantly degrade the transverse energy resolution[1].

The vertex position is determined by measuring the time difference between the outgoing beam jets that result from a collision. The beam jets are detected by the "Level 0" trigger counters, which consist of arrays of plastic scintillation counters that provide partial coverage over the angular range $1.5° - 18°$ with respect to the beam direction. Figure 1 shows a diagram of a Level 0 counter array. A Level 0 counter array will be mounted on the front face of both endcap calorimeters, ± 140 cm from the detector centerline. Since most particles at these small angles are highly relativistic, the vertex position, z_v, can be approximated by

$$z_v \approx \frac{c(t_- - t_+)}{2} \qquad (1)$$

where t_+ and t_- are the beam jet arrival times measured by the $+z$ and $-z$ Level 0 counters, respectively.

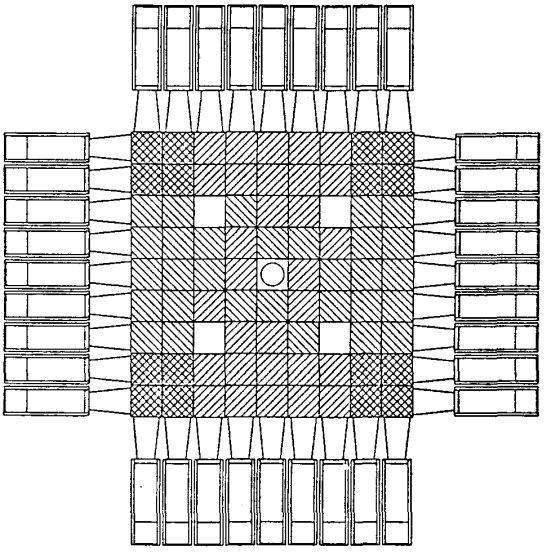

Figure 1: Diagram of a Level 0 counter array. The hatched areas indicate scintillator coverage.

The arrival times of the beam jets are determined by performing an analog sum of the 20 small counters at the center of the Level 0 arrays. Constant fraction discriminators are used to produce two timing pulses: a start pulse from the $-z$ array (which has a shorter cable delay) and a stop pulse from the $+z$ array. The time difference between these pulses is then digitized with the result directly related to the vertex position.

Since the vertex position is the first piece of information needed by the calorimeter trigger, a completely digital TDC design was selected to minimize the time needed to make the time difference measurement. The design features commercial GaAs integrated circuits that count the number of 2.4 GHz clock cycles between the start and stop TDC inputs. While this design optimizes the TDC accuracy and readout time, it does not provide the multi-hit readout, high channel density, and low power consumption needed for large drift chamber readout systems. Recent work [2-3] in high speed multi-hit digital TDC design

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†Permanent Address: Information Physics Department, Nanjing University, Nanjing, PRC

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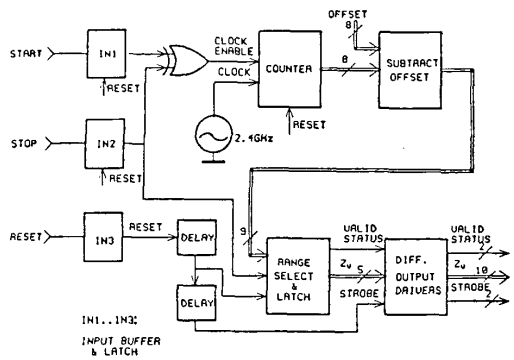


Figure 2: Block Diagram of the Digital TDC.

has achieved sub-nanosecond timing accuracy and may be more appropriate for this application.

2 Digital TDC Design

A block diagram of the Digital TDC is shown in Fig. 2. The input NIM signals are buffered and latched, with the start signal required to precede the stop signal by at least 2 ns. By making an exclusive-or of the latched start and stop signals, a pulse is created whose width is equal to the time difference between these signals. A counter is enabled for this time period, and counts the number of clock cycles during the period. The counter output is further processed to subtract an offset, negate and latch the results, and perform range checking to ensure the reconstructed vertex position is within the fiducial region $-97\text{cm} < z_v < 97\text{cm}$. If the vertex position lies in this range, the valid status bit is set and a 5-bit two's complement vertex position is output with a least significant bit (lsb) bin width of 6.25 cm. The reset signal is used to reset the counter and input latches on its falling edge; the rising edge is used to latch the counter output and initiate a data strobe. Differential ECL signals for the vertex position, valid status bit, and data strobe are available on two independent 20 pin output connectors.

A unique feature of this device is its use of commercial GaAs integrated circuits to provide the clock, exclusive-or, and counter functions. The clock is obtained from a Varactor Tuned Oscillator (Avantek VTO-8150) whose tuning voltage is set to yield a 2.4 GHz sinusoidal clock. The 2.4 GHz clock is counted by a GaAs ripple counter (GigaBit Logic 10G065) that incorporates a clock enable allowing the counter to count only during the time interval between start and stop signals. A GaAs exclusive-or (GigaBit Logic 10G002) is used to drive the clock enable signal, providing fast edges (150 ps typical rise and fall times) and differential inputs whose threshold is set to track the ECL 10KH logic transition level. The remainder of the circuit is conventional ECL 10KH circuitry, with an ECL PAL used to perform range checking and data validity checks.

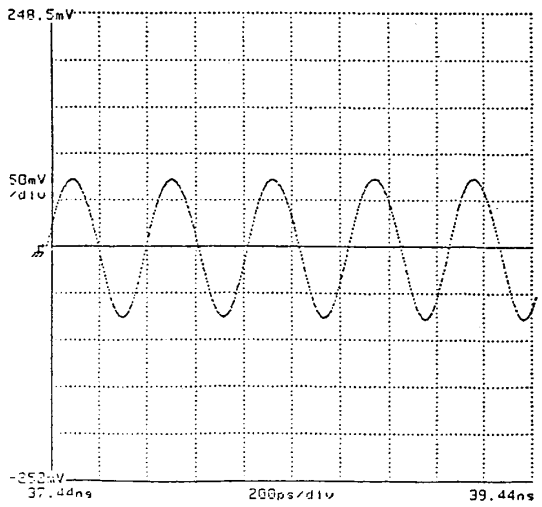
Prototype tests were made using a prototyping kit designed for use with Gigabit Logic chip packages (Gigabit Logic 90GUPB-40). The only major problem encountered was providing a sufficiently large clock signal to the counter, which requires a 2V p-p clock signal. This problem was largely due to the limitations of the board and sockets provided with the prototyping kit and was corrected by doing a proper printed circuit layout. Provision was made for using a more expensive buffered oscillator with a 40% larger amplitude (Avantek VTD-2000) as an alternative, but was not needed.

A four-layer circuit board was designed and fabricated for the digital TDC. Careful attention was paid to the layout of the GaAs section to ensure operation at high frequency. Striplines were used for critical signals with low-inductance surface mount resistors (Mini Systems WA47PG-500JNS) used to terminate all fast signals. The counter and exclusive-or circuits came in 40 pin LCC packages that were surface mounted directly to the board. Low-inductance surface mount bypass capacitors (Johanson Dielectrics 500-R11-W-102-MP4) were added to every power connection. The top side of the board was devoted to an extensive ground plane, with an internal power plane used to supply VSS (-3.4V) and VEE (-5.2V) to the GaAs and ECL circuits. Striplines and other traces were placed on the other internal layer, with additional traces and a VTT (-2V) plane on the bottom of the board.

3 Performance

It is first useful to analyze the expected performance of the circuit under an idealized model where the counter counts exactly the number of rising clock edges within the period defined by the clock enable. Since the 2.4 GHz clock is asynchronous with the clock enable, the number of rising edges will vary by one count depending on the relative phase of the clock and clock enable signals. However, when the width of the clock enable is an exact multiple of the clock period, the phase is no longer important and the counter should always count a unique number of clock cycles. The distribution of measurement errors should have a triangular shape, peaked at 0 error, with no measurements having an error larger than one clock period. The RMS measurement error for this distribution is given by $\sigma_t = (\sqrt{6}f)^{-1}$.

Several measurements were made to check the performance of the Digital TDC. Figure 3 shows the oscillator output measured using a sampling oscilloscope (Tektronix CSA803). The clock is quite symmetric with no obvious distortion with an amplitude of 3V p-p at the counter clock input. One check of the circuit is to see if a unique out-



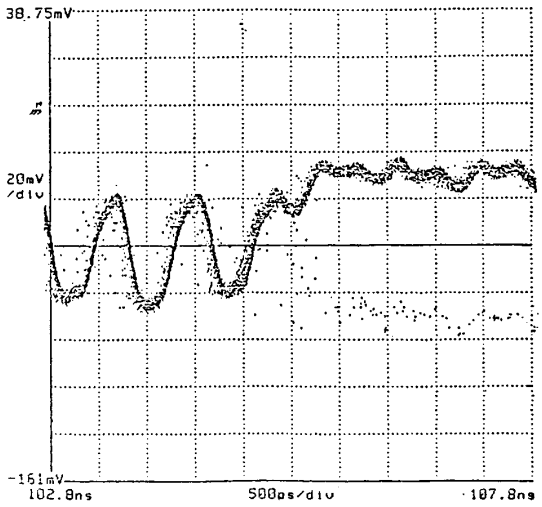


Figure 3: 2.4 GHz oscillator output.

put value is obtained when the width of the clock enable is an integral multiple of the clock period. Figure 4 shows a persistence plot of the counter's LSB as it is stopped for one particular multiple of the clock period. Note that the counter settles to a unique value nearly 100% of the time for this particular multiple of the clock period. While the measurement of Fig. 4 agrees with our predictions, other multiples of the clock period can be found where the counter output fluctuates by ± 1 from the expected result. While the reason for this behavior is not clear, it should be noted that the idealized model of the circuit neglects several features of the actual circuit. In particular, the asynchronous clock enable signal will not always meet the specified setup and hold times for this signal, which may lead to a one count difference in the results obtained. The action of the counter under these circumstances is unknown and may depend on factors such as internal noise or power droop that, in turn, depend on the value of the counter.

The time resolution of the TDC was determined by measuring the difference between the TDC digital output and the actual delay between the start and stop signals. A precision delay generator (Stanford Research Systems DG535) was used to generate the start, stop, and reset signals. The time difference between start and stop signals was found to be extremely stable with an RMS jitter of 20 ps measured using a sampling oscilloscope (Tektronix CSA803). Figure 5 shows a histogram of the measurement errors for delay times uniformly distributed over the range 20-50 ns in 100 ps steps. The accuracy of the digital TDC can be obtained from the width of this distribution; taking the RMS width yields an accuracy of 226 ps. While this is somewhat higher than the 170 ps accuracy predicted by

Figure 4: Persistence plot of the counter lsb showing how the counter settles for a clock enable width equal to a multiple of the clock period.

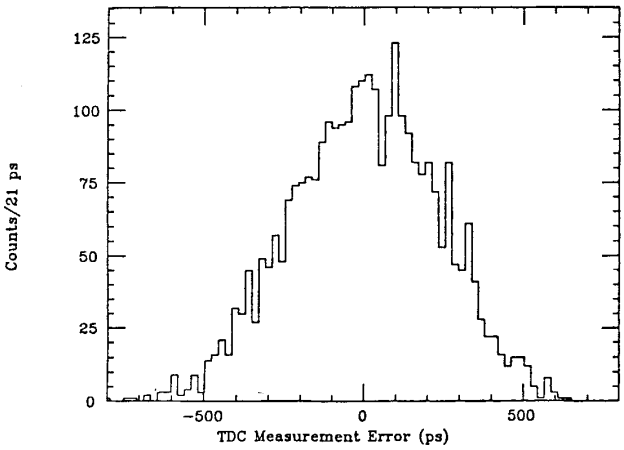


Figure 5: Distribution of the TDC measurement error. The idealized model of the circuit would have yielded a triangular distribution with a base 830 ps wide.

the idealized model, the corresponding error in the vertex position due to the TDC is only 3.4 cm, well below the design goal of 7 cm.

4 Summary

A digital TDC has been developed for determining the vertex position of collisions in the DØ detector. The TDC has an RMS error of 226 ps and features commercial GaAs integrated circuits. In principle, the technique used could be extended to make timing measurements over rather long time periods without degrading the timing accuracy. The current design is limited to measuring a maximum time difference of $\approx$ 100 ns, but could be easily extended by cascading additional counter stages. Ultimately, the ability of such a design to accurately measure long time periods depends on the stability and jitter of the clock; these were found to have negligible impact on the present design, with the clock jitter measured to be less than 12 ps after counting for 100 ns.

5 References

[1] The degradation of transverse energy resolution from not knowing the vertex position is worse for DØ than CDF due to the the smaller radius of the DØ calorimeter.

[2] Stuart Kleinfelder, T.J. Majors, K.A. Blumer, W. Farr, and Ben Manor, "MTD132 - A New Sub-Nanosecond Multi-hit CMOS Time-to-Digital Converter", these proceedings.

[3] Osamu Sasaki, "TKO 32-Channel Pipeline TDC Module using 1 GHz GaAs Shift Register", these proceedings.