India in Belle II Silicon Vertex Detector

A.B. Kaliyar[1],* G.B. Mohanty[2], K.K. Rao[2], and P.K. Behera[1]
[1] *Indian Institute of Technology Madras, Chennai - 600036, INDIA*
[2] *Tata Institute of Fundamental Research, Mumbai - 400005, INDIA*

Introduction

The next-generation B-factory, Belle II at the SuperKEKB accelerator, is expected to start physics data taking in 2018. The Belle II experiment is an upgraded version of Belle, which operated till 2010 at KEK in Tsukuba, Japan. The main goal of Belle II is to accumulate a 50 times larger data sample than its predecessor, which would offer a unique possibility to indirectly search for phenomena beyond the standard model through precision studies of rare decay processes. The Belle II detector is now being developed and constructed. It is a multipurpose instrument, which covers a large solid angle and has capability for a precise vertex reconstruction and momentum determination, and improved particle identification. All its sub-detectors have been redesigned to improve performances with respect to Belle as well as to cope with the expected steep increase in luminosity (leading to more backgrounds).

The silicon vertex detector (SVD) is one of the Belle II sub-detectors that would play a key role in locating beauty meson decay vertices towards CP violation measurements. In addition, it will provide vertex information for other decays involving charm mesons and tau leptons. The SVD consists of four layers of double-sided silicon microstrip detectors. The Indian groups, led by TIFR, are responsible for building one of the SVD layers. In this report, we will focus on the key design features, the status of ongoing production of SVD modules and India's role in the project.

*Electronic address: basithkaliyar@gmail.com

SVD Overview

Precise determination of the decay vertex position and low-momentum tracking are essential for the new physics searches in the beauty and charm sector. These tasks are performed by two silicon detectors: a four-layer microstrip detector at higher radii around the beam-pipe (SVD)[1] and a two-layer DEPFET-based [2] pixel detector (PXD) [3] as the innermost sensing device. The four layers of double-sided silicon strip detectors (DSSDs) are organised in a cylindrical geometry around the interaction point. It has a polar angle coverage from 17° in the forward region to 150° in the backward region, and radius ranging from 39 mm for the inner layer to 140 mm for the outer layer. The four SVD layers are named as Layer-3, 4, 5, and 6 (L3, L4, L5 and L6) going from the inner to outer layer (Layer-1 and 2 are the two PXD layers). Each layer consists of modules (ladders) which are an array of DSSD sensors. L3, L4, L5, and L6 have 7, 10, 12, and 16 ladders, respectively. Sensors are longitudinally organised in every ladders, which are made of 2, 3, 4, 5 sensors for L3-L6 respectively. Ladders in L3 are straight, whereas in remaining layers the last DSSD in the forward direction is slanted with angles of 11.91°, 17.21°, and 21.11° for L4 to L6. The purpose of the slanted shape is to improve the hit quality by avoiding shallow hits with large cluster widths with minimum material budget and the number of sensors. Figure 1 shows the three-dimensional model of the SVD.

Sensors and readout system

Three types of DSSD sensors, fabricated on silicon wafers with n-type substrate are used in the SVD, all having the same length of 12.3 cm and thickness of 300 or 320 μm [4]. The large rectangular DSSDs with 5.8 cm wide and smaller width (3.8 cm) DSSDs, which are cho-

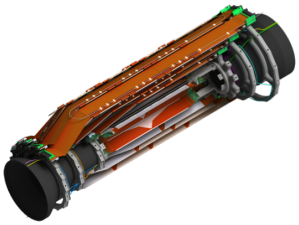

FIG. 1: The Belle-II silicon vertex detector.

sen for L3 to ensure a circular arrangement of DSSDs around the PXD, are made by Hamamatsu Photonics (Japan). Trapezoidal DSSDs with width ranging from 3.8 to 5.8 cm, made by Micron Semiconductor Ltd. (UK), are used for the slanted sensors. More details on the sensors can be found in Ref. [5].

In addition to the DSSDs, each ladder comprises of a support structure, flexible printed circuit boards, a CO_2 cooling pipe (in L4-L6 ladders), and APV25 chips [6] which read out the signals from DSSDs. The L3 ladder and both the forward and backward side DSSD in L4-L6 ladders adopt the conventional readout scheme of an edge-side readout with fanouts, as in Belle. In L4-L6, all DSSDs but for the forward and backward ones have the novel Origami chip-on-sensor readout scheme [7]. The Origami is a three-layer kapton hybrid circuit on which all APV25 readout chips of one sensor are placed and aligned. The Origami is first glued on the top side of the sensor, with a 1 mm thick layer of Airex [8] in between, to ensure electrical and thermal insulation. The sensor top side strips are connected to the APV25 chips through a planar flexible pitch adapter circuit, while the bottom side strips are routed to the other side of the sensor, toward the electronics, wrapping two different pitch adapters around the sensor edge, above the top side wire bondings. Two carbon fiber ribs are used as a support structure for the ladder. The Origami scheme minimize the distance between the DSSDs and readout electronics, which in turn reduces the capacitive noise.

SVD construction status

The ladder assembly procedure is highly complex and calls for a dedicated and attentive work. The procedure should be systematically consistent in L4-L6 ladders as much as possible, have a good assembly precision, and a short construction time. An assembly scheme matching these requirements has been designed and verified by building a number of prototype ladders. The construction work is distributed among several groups. The forward and backward sub-assemblies are produced at INFN Pisa and later shipped to other assembly sites: L4 (TIFR), L5 (HEPHY), and L6 (IPMU). The L3 assembly is performed by the Melbourne group. The R&D for the ladder assembly procedure is now over, and by now each site has assembled a number of production grade ladders. This have been thoroughly tested and studied for the overall performance and potential defects of the sensors. One such production-grade L4 ladder built by the Indian group is shown in Figure 2.

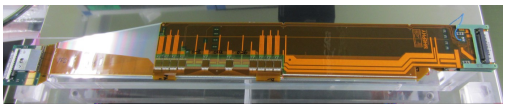

FIG. 2: A production-grade L4 ladder.

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