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Energy and power scaling in quantum computers based on rotated surface codes with silicon flip-flop qubits

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Abstract

Scalable solutions are essential to achieving the long-term goal of building a fault-tolerant quantum computer and energy-power consumption are fundamental limiting factors for this target. Among the available types of silicon qubits, this work focuses on Flip-Flop (FF) qubits. Energy consumption and power requirements are estimated for a square array of qubits that hosts the logical qubit. The logical qubit is implemented using the rotated Surface Code (SC) for Quantum Error Correction (QEC). By using a universal set of quantum gates, the energy usage, time and power requirements for a SC cycle are estimated based on noise level, code distance and control levels. These estimates are used to provide insights into the main scaling-up challenges for quantum computer development. This is achieved by extending a thermal model that includes energy contributions from both the cryogenic components (such as the qubit array, the cryogenic control electronics, and the cryostat) and the room temperature (RT) section (RT electronics and heat dissipation systems). The maximum numbers of physical and logical qubits are provided, as well as power consumption across the different temperature sections.

Keywords: Silicon qubits; Energy-power consumption; Quantum error correction; Surface code; Quantum computer architecture; Scalability

1 Introduction

Quantum technologies offer significant benefits across many critical areas of society. However, like any new technology, they require resources, especially energy, which is becoming increasingly limited. Therefore, it is essential for researchers to develop ways to understand and reduce the resource consumption of quantum technologies while preserving their advantages [1–4].

A quantum computer requires a significant number of physical qubits, typically between 10^5 and 10^8, to operate effectively. This high number is essential for error correction, as physical qubits are susceptible to errors caused by noise and environmental factors.

In Ref. [5], a comprehensive and detailed technical review is periodically updated with values for selected performance characteristics - such as qubit coherence, speed, fidelity, and qubit count - of semiconductor spin qubits defined in electrically controlled nanostructures. However, information on energy and power consumption is still lacking due to

the absence of a standardized set of parameters for comparing the energy and power dissipated by the various components of the system, along with the relatively recent focus on energy efficiency.

In semiconductor-based quantum technology [6], including silicon-based systems [7], these qubits must operate at extremely low temperatures, generally within the millikelvin (mK) to kelvin (K) range, to maintain stable quantum states and reduce thermal noise. Operating at such low temperatures requires sophisticated refrigeration systems that consume substantial amounts of energy [8, 9]. These systems must not only remove the heat generated by the qubits and control electronics but also counteract any heat that leaks into the system from the surrounding environment. As a result, the energy needed for cooling greatly exceeds the power required to operate the quantum circuits. This makes managing thermal conditions a major challenge in quantum computing. Additionally, theoretical frameworks have been proposed to understand and manage thermal effects at the quantum scale, which is crucial for the development of advanced nanoscale technologies [10].

A significant advancement in scaling silicon quantum computing was achieved with a cryogenic Complementary Metal-Oxide-Semiconductor (CMOS) chip that controls, with high fidelity, a small number of qubits defined on electron spins confined in silicon QDs, enabling the execution of quantum benchmarks and algorithms [11].

More recent developments in silicon-based quantum computing have focused on improving not only scalability, but also energy efficiency. For instance, Ref. [12] introduces a method for scalable on-chip multiplexing of silicon single and double Quantum Dots (QDs). This approach integrates cryogenic classical CMOS electronics with QD devices, aiming to reduce power dissipation and enhance the scalability of silicon-based quantum processors. Moreover, Ref. [13] presents a scalable cryo-CMOS demultiplexer chip for silicon qubits based on electron spins confined in QDs, with reduced power dissipation.

In this paper, we consider a donor-dot-based qubit, specifically the FF qubit [14]. This type of qubit is controlled by an electric field generated by a gate voltage, which shifts the position of the electron bound to a ^{31}P donor between a QD at the Si/SiO_2 interface and the ^{31}P nucleus in a ^{28}Si substrate. The qubit's logical states are defined by the two antiparallel spin states of the electron and nucleus. Rabi oscillations can be induced by an AC electric field through Electric Dipole Spin Resonance (EDSR). Long-range coupling between two FF qubits (ranging 100 to 500 nm) is enabled through the electric dipole-dipole interaction, easing the stringent distance constraints present in other QD-based qubit architectures. Several theoretical studies have been done on the performances of one and two FF qubits gates [15–18] and on small 1D [19] and 2D arrays of FF qubits [20, 21]. In particular, operations on an FF qubit have already been experimentally demonstrated [22].

We assess the energy consumption and power requirements for a square array hosting logical qubits constructed using one of the most used QEC codes: the rotated SC [23]. Furthermore, the development of quantum hardware with computational advantage relies on the quality of quantum gate operations, with imperfect quantum gates posing a significant challenge [24]. Our goal is to provide realistic energy and power estimates in a quantum computer based on FF qubits.

The paper is organized as follows. In Sect. 2, we present the FF qubit and the Hamiltonians that describe the one- and two-qubit systems, and the basic layout of the FF qubit

including the initialization and readout sections. Section 3 includes a description of the rotated SC, followed by the main results concerning logical errors and the average power per cycle consumption. Section 4 presents the quantum computer architecture and the thermal model used to estimate power consumption. Finally, the conclusions are provided in Sect. 5.

2 Flip-flop qubit

The Hamiltonian models for one and two interacting FF qubits are presented. Then, the basic layout of the FF qubit with the initialization and readout sections is illustrated.

2.1 Hamiltonian models

2.1.1 One FF qubit

The FF qubit is sketched in Fig. 1(a) and described by the following Hamiltonian model [14, 16] composed by three terms

$$H^{FF} = H_{orb} + H_{B_0} + H_A. \tag{1}$$

The first term is the orbital Hamiltonian:

$$H_{orb} = -\frac{\epsilon_0}{2}\sigma_z - \frac{d_{dip} e \mathcal{E}_{AC}(t)}{2h}\left(\frac{d_{dip} e \Delta\mathcal{E}_z}{h\epsilon_0}\sigma_z + \frac{V_t}{\epsilon_0}\sigma_x\right), \tag{2}$$

where V_t is the tunnel coupling between the donor and the interface potential wells; $\Delta\mathcal{E}_z = \mathcal{E}_z - \mathcal{E}_z^0$ where $\mathcal{E}_z^0$ is the vertical electric field at the ionization point, i.e. the

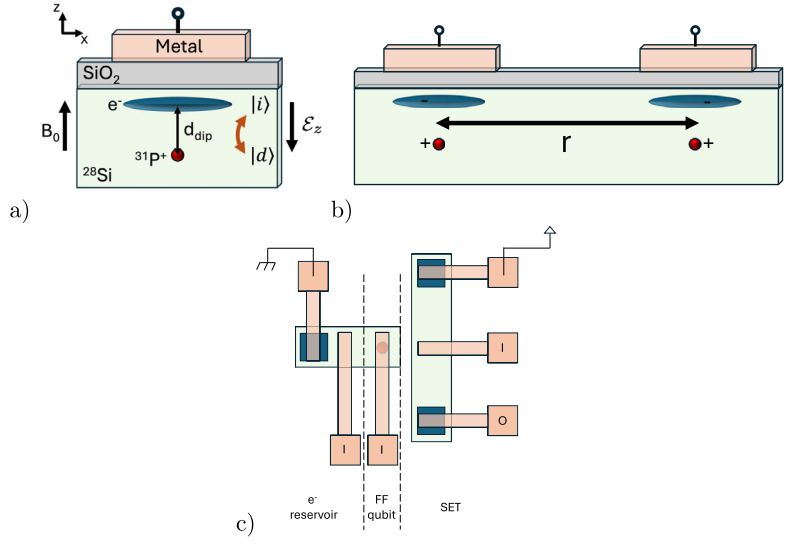

Figure 1 a) Scheme of an FF qubit. A ^{31}P donor atom is embedded in a ^{28}Si bulk, positioned at a distance z_d from a Si/SiO_2 interface and under the application of a constant magnetic field B_0. An electric field $\mathcal{E}_z$, generated along the $\hat{z}$-axis by an external gate voltage applied to the metal gate on the top, controls the system states by moving the electron position between the nucleus $|d\rangle$ and the QD at the interface $|i\rangle$. b) Scheme of two interacting FF qubits with an inter-qubit distance r. c) Basic layout (not in scale) of the FF qubit with the e^- reservoir and the SET. Metal pads labeled with I accept Input signals whereas pads marked with O provide Output ones. SiO_2 layer is not displayed for clearness

point in which the electron is shared halfway between the donor and the interface; $\epsilon_0 = \sqrt{V_t^2 + (d_{dip} e \Delta\mathcal{E}_z/h)^2}$ is the energy difference between the orbital eigenstates, with h the Planck's constant, d_{dip} the dipole distance, hereafter d_{dip} = 15 nm, and e the elementary charge. $\mathcal{E}_{AC}(t) = \mathcal{E}_{AC}\cos(\omega_E t + \varphi)$ is an AC electric field applied in resonance with the FF qubit, $\omega_E = 2\pi\epsilon_{ff}$ where ϵ_{ff} is the transition frequency of the FF qubit and φ is an additional phase. The Pauli matrices $\sigma_z = |g\rangle\langle g| - |e\rangle\langle e|$ and $\sigma_x = |g\rangle\langle e| + |e\rangle\langle g|$ are expressed in the basis of the orbital eigenstates $|g\rangle$ and $|e\rangle$ that are respectively the ground and the excited states.

The second term is the Zeeman interaction:

$$H_{B_0} = \gamma_e B_0 \left[\mathbb{1} + \left(\frac{\mathbb{1}}{2} + \frac{d_{dip} e \Delta\mathcal{E}_z}{2h\epsilon_0}\sigma_z + \frac{V_t}{2\epsilon_0}\sigma_x \right) \Delta_\gamma \right] S_z - \gamma_n B_0 I_z, \tag{3}$$

where B_0 is the static magnetic field oriented along the $\hat{z}$ axis, (B_0 = 0.4 T); Δ_γ quantifies the dependence of the electron Zeeman splitting on its orbital position, (Δ_γ = –0.2%); $\mathbb{1}$ is the identity operator on the orbital subspace and **S** and **I** are the electron and nuclear spin operators, respectively.

Finally, the hyperfine interaction given by:

$$H_A = A \left(\frac{\mathbb{1}}{2} - \frac{d_{dip} e \Delta\mathcal{E}_z}{2h\epsilon_0}\sigma_z - \frac{V_t}{2\epsilon_0}\sigma_x \right) \mathbf{S}\cdot\mathbf{I}, \tag{4}$$

where A is the hyperfine coupling that is a function of the applied electric field $\Delta\mathcal{E}_z$.

2.1.2 Two FF qubits

The two FF qubits scheme is depicted in Fig. 1(b) and described by the Hamiltonian model H^{2FF} obtained adding up two single-qubit Hamiltonians Eq. (1), supposed identical, and an interaction term

$$H^{2FF} = H_1^{FF} + H_2^{FF} + H_{int}. \tag{5}$$

H_{int} is the dipole-dipole interaction:

$$H_{int} = \frac{1}{4\pi\varepsilon_0\varepsilon_r r^3}\left[\mathbf{p}_1\cdot\mathbf{p}_2 - \frac{3(\mathbf{p}_1\cdot\mathbf{r})(\mathbf{p}_2\cdot\mathbf{r})}{r^2} \right], \tag{6}$$

where ε_0 (ε_r) is the vacuum permittivity (material dielectric constant, for silicon 11.7) and **r** is the two-qubit distance set to r = 360 nm. The dipole operator is $p_{1(2)} = d_{dip} e(\mathbb{1} + \sigma^{id}_{z,1(2)})/2$, where the electron position operators are defined as $\sigma_z^{id} = |i\rangle\langle i| - |d\rangle\langle d|$ and $\sigma_x^{id} = |i\rangle\langle d| + |d\rangle\langle i|$, the eigenvector $|i\rangle(|d\rangle)$ denotes the interface (donor) electron position and are expressed in the orbital eigenbasis by the following relations: $\sigma_z^{id} = \frac{d_{dip} e\Delta\mathcal{E}_z}{h\epsilon_0}\sigma_z + \frac{V_t}{\epsilon_0}\sigma_x$ and $\sigma_x^{id} = -\frac{V_t}{\epsilon_0}\sigma_z + \frac{d_{dip} e\Delta\mathcal{E}_z}{h\epsilon_0}\sigma_x$.

2.2 Basic layout

In Fig. 1(c), a basic layout of the FF qubit, along with additional structures needed for qubit operation, is illustrated.

The device of the FF qubit, which requires a single metal gate for its control, is sandwiched between an electron reservoir and a Single Electron Transistor (SET), both essential for qubit initialization and readout.

The electron reservoir is flanked by a metal gate to control the tunnel barrier for loading the electron into and out of the FF qubit during the initialization and readout steps.

The SET is realized by an electrostatically defined QD, separated by gate-controlled tunneling barriers from two electron reservoirs and operates as a charge sensor. The spin readout is performed using the Elzerman technique [25]. After the readout command, the electron may tunnel to the reservoir depending on its spin state, altering the electrostatic environment. This change affects the SET conductance, resulting in different current levels that reflect the electron's spin state.

In the proposed layout, three metal pads labeled with I accept input signals, whereas one single pad marked with O provides the output signal.

3 Rotated surface code

SCs are among the most promising approaches for building a quantum computer due to their ability to highly tolerate local errors [23].

A variant of the SC, known as the rotated SC, is established on a two-dimensional array of physical qubits that has been rotated 45° degrees counterclockwise, allowing a reduction of the total number of qubits with respect to the unrotated SC and maintaining the same logical error [26]. This arrangement places the qubits at the vertices, while the X and Z operators are situated on plaquettes in an alternating checkerboard pattern, as illustrated in Fig. 2(a).

The open circles represent the data qubits, while the solid squares denote the measurement qubits. These measurement qubits play a crucial role in stabilizing and controlling the quantum state of the data qubits. The green qubits are known as Z syndrome qubits, whereas the blue ones are X syndrome qubits. Each data qubit is linked to two Z syndrome qubits, which ensure that the neighboring data qubits are set into an eigenstate of the Z operator (Z stabilizer), and to two X syndrome qubits, which similarly enforce an eigenstate of the X operator (X stabilizer) on the neighboring data qubits.

Figure 2(b) (top) shows the quantum circuit for a single SC cycle involving a measure-Z qubit. This cycle consists of two identity operators, executed by simply waiting, and four CNOT operations operated in a specific zig-zag sequence [23]. Similarly, Fig. 2(b) (bottom) illustrates the case for a measure-X qubit, which also requires two Hadamard (H)

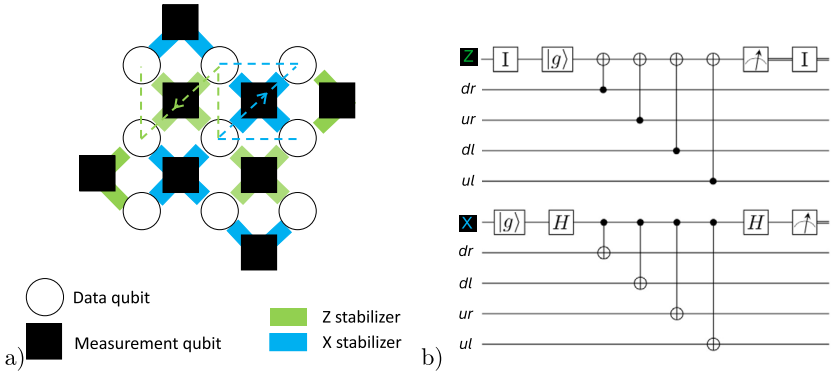

Figure 2 a) Schematic representation in plane view of the rotated SC with a code distance $d = 3$. The dashed green (blue) arrow represents the direction of the Z (X) stabilizer circuit operations indicated on the right. b) Circuit representation of Z (top) and X (bottom) stabilizers, where ul, ur, dl, dr (up-left, up-right, down-left, down-right) denote the generic four data qubits around the measurement qubit

gates. By placing the identity operators at both the beginning and the end of the sequence, the effect of any errors during these phases is reduced, while also ensuring that the timing of the measure-X qubit is synchronized with that of the measure-Z qubit, with the measure-X qubit undergoing two H operations.

3.1 Surface code error

An estimate of the SC error is derived from errors associated with the noisy gate operations that make up the sequences.

Charge noise represents the main source of decoherence in quantum devices that utilize isotopically enriched silicon. It results from adjacent charge fluctuators, which typically arise from defects and electron traps at the Si/SiO_2 interface. It shows a power spectral density that fluctuates as 1/f over a wide range of frequencies f and induces electrical fluctuations in FF qubits, affecting the control electric field.

We begin our analysis by calculating the fidelities in the presence of 1/f noise of the CNOT and H operations, which are obtained by combining the one qubit operations $R_z(-\frac{\pi}{2})$ and $R_x(-\frac{\pi}{2})$ and the two qubit operation $\sqrt{iSWAP}$ through the relations shown in Fig. 3, note that $iSWAP = \sqrt{iSWAP}\sqrt{iSWAP}$.

All the control signal sequences that implement the operations are outlined in Ref. [20]. By using the entanglement infidelities, denoted as $err_{R_z(-\frac{\pi}{2})}$, $err_{R_x(-\frac{\pi}{2})}$ and $err_{\sqrt{iSWAP}}$ for each gate under study, as error metrics and calculating the conditional probability while also accounting for the state preparation and measurement (SPAM) errors denoted by err_{SPAM} and set to 1%, we derive an estimate for the error associated to the Z stabilizer

$$err_Z = 1 - [(1 - err_{CNOT})^4(1 - err_{SPAM})] \tag{7}$$

and for the X stabilizer

$$err_X = 1 - [(1 - err_{CNOT})^4((1 - err_{R_z(-\frac{\pi}{2})})^2(1 - err_{R_x(-\frac{\pi}{2})}))^2(1 - err_{SPAM})]. \tag{8}$$

We point out that also the error for the CNOT gate is calculated as a conditional probability among the single and two qubit operations as

$$err_{CNOT} = 1 - [(1 - err_{R_z(-\frac{\pi}{2})})^6(1 - err_{R_x(-\frac{\pi}{2})})^5(1 - err_{\sqrt{iSWAP}})^8]. \tag{9}$$

Following Ref. [23] and having observed that $err_Z \simeq err_X$, we calculated the SC error p for each step by exploiting the following formula

$$err_Z = n_{step}p(1 - p)^{(n_{step}-1)}, \tag{10}$$

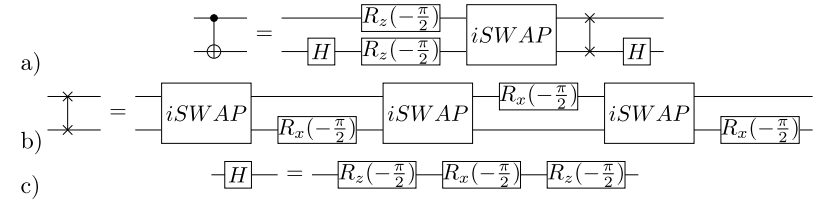

Figure 3 a) CNOT, b) SWAP and c) H gate decompositions

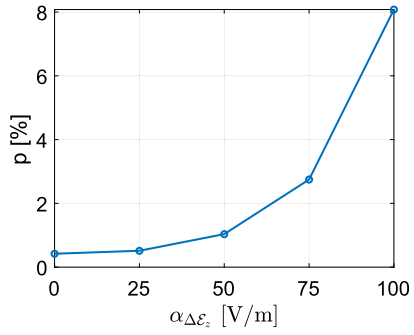

Figure 4 SC physical error per step p as a function of the noise amplitude $\alpha_{\Delta\mathcal{E}_z}$

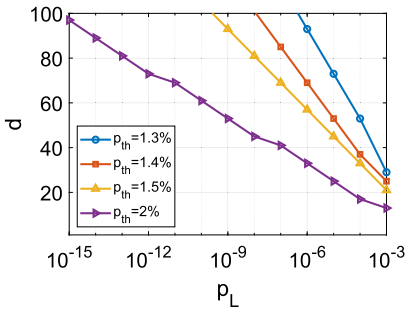

Figure 5 Code distance d as a function of the logical error p_L for different values of fixed threshold errors with $p = 1\%$

with $n_{step} = 8$, that is the number of steps needed for both stabilizers in a SC cycle.

In Fig. 4 we report the SC error per step p as a function of the noise amplitude $\alpha_{\Delta\mathcal{E}_z}$, observing an exponential dependence with respect to p with values ranging from 0.4% when noise is zero to around 8% in correspondence to $\alpha_{\Delta\mathcal{E}_z} = 100$ V/m, passing through 1% when $\alpha_{\Delta\mathcal{E}_z} = 50$ V/m. It should be noted that $p \neq 0$ at $\alpha_{\Delta\mathcal{E}_z} = 0$ V/m because the gate sequences are not perfectly adiabatic. All control sequences feature the same adiabatic factor, which represents a trade-off between the speed and fidelity of the quantum gate [14, 18].

We focus on a still realistic noise level, that is $\alpha_{\Delta\mathcal{E}_z} = 50$ V/m, and we exploit the relation between the logical (p_L) and physical error [23]

$$p_L \simeq 0.03(p/p_{th})^{(d+1)/2}, \tag{11}$$

where p_{th} is the threshold error rate and d is the code distance. In a rotated SC, as in our case, d is odd and even solutions are discarded. Figure 5 shows the code distance d as a function of the logical error p_L for fixed threshold errors ranging from 1.3% to 2% and p = 1%, which is the value when $\alpha_{\Delta\mathcal{E}_z} = 50$ V/m as reported in Fig. 4.

As expected, the code distance increases as the logical error and the threshold decrease. For example, we observe that when requiring a $p_L = 10^{-15}$ with a threshold of 2%, a code distance of $d = 97$ is needed. For a lower $p_L = 10^{-4}$ and $p_{th} = 2\%$, a lower $d = 17$ is enough.

3.2 Average power per cycle consumption

We calculate the average power per cycle as a function of the code distance by estimating the energy of the entire SC cycle E_{cycle} and dividing it by the total time t_{cycle}.

The energy E_{cycle} is calculated as the sum of three main contributions: the energies E_Z and E_X, which correspond to the Z and X stabilizers, and the energy required for syndrome decoding, denoted as $E_{decSynd}$, as outlined below:

$$\begin{aligned} E_{cycle} =& E_Z + E_X + E_{decSynd} = \\ =& \frac{n_{stab}}{2}(4E_{CNOT} + E_{readout} + E_{init} + p^* E_{corrZ}) + \\ &+ \frac{n_{stab}}{2}(2E_H + 4E_{CNOT} + E_{readout} + E_{init} + p^* E_{corrX}) + \\ &+ E_{decSynd}. \end{aligned} \tag{12}$$

The energies of the Z and X stabilizers each account for half of the total number of stabilizers $n_{stab} = d^2 - 1$. These energies include the contributions from the operations that compose the sequence (CNOT or H plus CNOT). We define the manipulation energy as the average energy of the operations in both stabilizers, given by $E_{manip} \equiv (4E_{CNOT} + 4E_{CNOT} + 2E_H)/2$. Additionally, the total energy includes the energy for initialization E_{init}, due to the tunneling of an electron from a nearby reservoir to the FF qubit, and the error correction $E_{corrZ}(E_{corrX})$, which corresponds to an $R_x(-\pi)$ ($R_z(-\pi)$) and is implemented as a series of two $R_x(-\frac{\pi}{2})$ ($R_z(-\frac{\pi}{2})$) when the Z syndrome (X syndrome) is sensed. As with E_{manip}, we define $E_{corr} \equiv (E_{corrZ} + E_{corrX})/2$ as the average of the two energies. Finally, it also includes the energy for FF qubit readout $E_{readout}$, extracted from Ref. [22], due to the operation of a SET coupled to the FF qubit.

The parameter $p^* \equiv p(50)$ is calculated using Eq. (10) and reported in Fig. 4 in correspondence to $\alpha_{\Delta\mathcal{E}_z} = 50$ V/m where it is equal to 1%.

The energy required for syndrome decoding $E_{decSynd}$ depends on the method adopted and here a neural network decoder is used. $E_{decSynd}$ includes the energy required by the digital electronics for implementing the neural network decoder and is extrapolated from Ref. [27], which provides the time and power values for $d = 3, 5, 7, 9$. Specifically, we performed a linear extrapolation of the reported data and then calculated the exponential value to estimate the energies for code distances $d > 9$.

Other types of decoders also exist, such as those based on the well-known Minimum-Weight Perfect Matching (MWPM) method, Renormalization Group (RG) decoders, Union-Find (UF) decoders, and Tensor-Network (TN) decoders [28, 29]. We plan to investigate these in future work.

The energies related to the CNOT and H operations are derived by combining the energies of the $R_z(-\frac{\pi}{2})$, $R_x(-\frac{\pi}{2})$ and $\sqrt{iSWAP}$ gates (see Fig. 3), which are calculated as integrals over the total duration of each respective operation:

$$E_{R_z(-\frac{\pi}{2})} = \frac{1}{2}\epsilon_0\epsilon_r \frac{1}{t_{R_z(-\frac{\pi}{2})}} \left[\int_0^{t_{R_z(-\frac{\pi}{2})}} (\mathcal{E}_z^0 + \Delta\mathcal{E}_z(t))^2 dt\right] V, \tag{13}$$

$$\begin{aligned} E_{R_x(-\frac{\pi}{2})} = E^{DC}_{R_x(-\frac{\pi}{2})} + E^{AC}_{R_x(-\frac{\pi}{2})} =& \frac{1}{2}\epsilon_0\epsilon_r \frac{1}{t_{R_x(-\frac{\pi}{2})}} \left[\int_0^{t_{R_x(-\frac{\pi}{2})}} (\mathcal{E}_z^0 + \Delta\mathcal{E}_z(t))^2 dt\right] V \\ &+ t_{\mathcal{E}_{AC}} \frac{((A_{AC}/K)/\sqrt{2})^2}{\rho}, \end{aligned} \tag{14}$$

$$E_{\sqrt{iSWAP}} = \frac{1}{2}\epsilon_0\epsilon_r \frac{1}{t_{\sqrt{iSWAP}}} \left[\int_0^{t_{\sqrt{iSWAP}}} (\mathcal{E}_z^0 + \Delta\mathcal{E}_{z_1}(t))^2 dt + \right. \\ \left. + \int_0^{t_{\sqrt{iSWAP}}} (\mathcal{E}_z^0 + \Delta\mathcal{E}_{z_2}(t))^2 dt \right] V. \tag{15}$$

The times $t_{R_z(-\frac{\pi}{2})}$, $t_{R_x(-\frac{\pi}{2})}$ and $t_{\sqrt{iSWAP}}$ indicate the total duration of the corresponding operations. $\mathcal{E}_z^0 = 4.086 \cdot 10^6$ V/m represents the vertical electric field at the ionization point, where the electron is equally shared between the donor and the interface. $\Delta\mathcal{E}_z(t)$ refers to the applied DC electric fields, with their sequences detailed in [20]. For the two-qubit gate $\sqrt{iSWAP}$, two electrical fields, $\Delta\mathcal{E}_{z_1}(t)$ and $\Delta\mathcal{E}_{z_2}(t)$, are applied to qubit 1 and 2, respectively. The R_x operation requires the application of both a DC electrical field and an AC electrical field. The AC field is characterized by its activation time ($t_{\mathcal{E}_{AC}} = 40$ ns), its amplitude ($A_{AC} = 180$ V/m), a conversion constant ($K = 10^7$ 1/m) and a resistance ($\rho = 50\,\Omega$) in which a 1 μV AC voltage produces a 10 V/m AC vertical electric field [14]. V denotes the volume of the FF qubit, calculated as $V = l_q w_q h_q$, where we set the three dimensions as $l_q = 120$ nm, $w_q = 40$ nm and $h_q = 30$ nm.

The energy required by analog electronics needed for qubit control can be relevant. This contribution strictly depends on how the control signals are generated and routed to the FF qubits and it is not accounted for here but included in the model presented in Sect. 4.

The total time is written as

$$t_{cycle} = t_{manip} + t_{readout} + t_{init} + t_{decSynd} + t_{corr}, \tag{16}$$

where $t_{decSynd}$, as well as $E_{decSynd}$, is extrapolated from the data reported in Ref. [27].

The manipulation time is defined as the total duration of the operations in the X stabilizer (the longer of the two stabilizers), expressed as $t_{manip} \equiv 4t_{CNOT} + 2t_H$, as well as the correction time, defined as $t_{corr} \equiv t_{R_x(-\pi)}$.

Table 1 summarizes all the quantities included in Equations (12) and (16) that are used in the subsequent analysis. The energy and time values for syndrome decoding range from $d = 3$ to $d = 17$.

As can be observed, the energy associated with error syndrome decoding is the dominant term, while the energy required for qubit readout is the second most significant. The same statement holds for the corresponding powers.

Figure 6 illustrates the average power per cycle per qubit $\langle P_{cycle}\rangle/n \equiv E_{cycle}/(t_{cycle}n)$, where n is the total number of physical qubits in a single logical qubit, calculated as the sum of the data qubits (d^2) and measurement ($d^2 - 1$) qubits.

Table 1 Energies and times associated with each step of the SC cycle

	Energy [J]	Time [ns]
init	$1.6 \cdot 10^{-19}$	100
$R_z(-\frac{\pi}{2})$	$1.2 \cdot 10^{-19}$	36.08
$R_x(-\frac{\pi}{2})$	$1.3 \cdot 10^{-19}$	102.5
$\sqrt{iSWAP}$	$2.5 \cdot 10^{-19}$	427.6
CNOT	$17 \cdot 10^{-19}$	2000
H	$5 \cdot 10^{-19}$	174.7
manip	$73 \cdot 10^{-19}$	8349.4
readout	$1 \cdot 10^{-13}$	1000
corr	$2.5 \cdot 10^{-19}$	205
decSynd	$10^{-13} - 2.1 \cdot 10^{-6}$	10 – 63.21

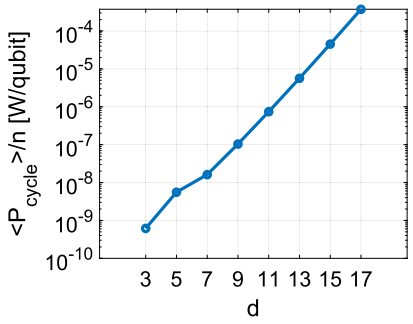

Figure 6 Average power per cycle per qubit as a function of the code distance d in a rotated SC with FF qubits

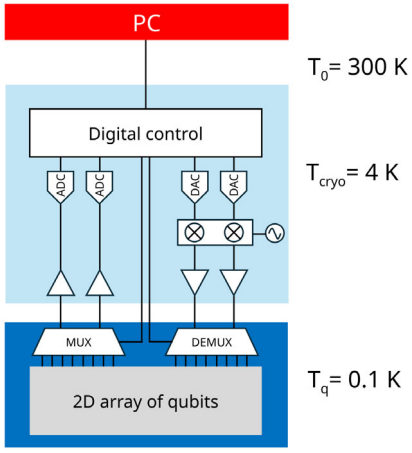

Figure 7 Scheme of the quantum computer architecture. A PC at T_0 controls the entire system, sending signals to and receiving signals from the cryogenic section at T_{cryo}. The cryogenic section is composed of a digital control unit and analog devices. The digital control unit is responsible for SC error syndrome decoding, while the analog control part handles input/output operations, including DACs, mixers, LOs, LNAs, and ADCs. Interconnections extend to the cryogenic base section at T_q, where analog MUX and DEMUX circuits route input/output signals to interface with the entire 2D array of qubits

The average power per cycle per qubit increases exponentially with the computational space dimension d, meaning that as the number of FF qubits for logical ones grows, power consumption enlarges.

In conclusion, for a single logical qubit implemented on a rotated SC with FF qubits, power consumption per cycle per physical qubit increases significantly as the system size grows. Specifically, power ranges from 0.6 nW for $d = 3$ to 371 μW for $d = 17$. The exponential scaling of the power with the code distance d, mainly due to the power consumption of the selected type for error syndrome decoding, stresses the need for low power Application Specific Integrated Circuits (ASIC) optimized for this task.

4 Quantum computer

4.1 Architecture

The quantum computer architecture that uses FF qubits is presented in Fig. 7 and is inspired by Ref. [30].

It consists of various components operating at different temperatures. The 2D array of FF qubits is kept at a base temperature of $T_q = 0.1$ K within a cryostat. Each FF qubit is supplied with pulsed DC signals and AC control signals in the microwave range and the coupled SET requires an output line to provide the readout signal. In this section, the electronics for MUltipleXing (MUXing)/DEMUltipleXing (DEMUXing) of control and readout lines are included. The MUX/DEMUX approach is chosen to reduce the number of interconnection lines between the T_{cryo} and T_q sections, limiting the heat load from the

hotter section to the cooler one. The cryostat also houses circuits and sensors that operate at cryogenic temperatures T_{cryo} = 4 K. Key components of the control/readout system include analog devices and a digital controller based on cryo-CMOS technology. The analog devices for the control section are Digital to Analog Converters (DACs), up-converting mixers, frequency synthesizers, and amplifiers, while Low-Noise Amplifiers (LNAs) and Analog to Digital Converters (ADCs) constitute the readout section. The digital controller coordinates all input and output signals to and from the analog devices and computes all the operations required for the error syndrome decoding. The digital controller is then connected to the external control system, which operates at RT of T_0 = 300 K, constituted by a general-purpose Personal Computer (PC) orchestrating all operations for the algorithm implementation.

4.2 Thermal model

We propose a new thermal model, extending the one presented in Ref. [1] and schematized in Fig. 8. This model details the power consumption of qubits operating at cryogenic temperatures and external circuits operating at RT T_0 or a higher temperature T_{hot}, along with the corresponding heat loads.

The definitions of all parameters included in the analysis, along with their values and respective references, are reported in Table 2.

We assume that power can be divided between cryogenic ($P_1 + P_2 = \phi P_c$) and RT ($P_3 = (1-\phi)P_c$) electronics, where P_c is the total computational power. For the cryogenic cycles the work is calculated by dividing the heat by the Carnot coefficient of efficiency ($COP(T_i)|_C$) multiplied by a coefficient $\eta_C < 1$. η_C accounts for realistic cryostat efficiencies by reducing the ideal efficiency of a Carnot cycle. For the cooling energy cost of the RT electronics, which is not cooled by a direct refrigeration cycle, a figure of merit denoted as $FOM(T_0)$ is exploited. The heat is proportional to the cryostat's heat transfer coefficient (U), the area of the cryogenic chambers ($C_1 V_i^{2/3}, i = 1, 2$) and the temperature differences.

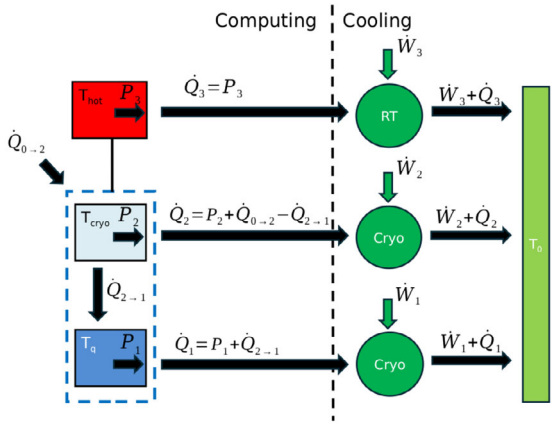

Figure 8 Quantum computer thermal scheme and energy fluxes. On the left, the scheme includes thermal sources related to the computation, with the different sections of the cryostat at hot and cryogenic temperatures. On the right, the scheme highlights thermal sources due to the cooling process of each section. Black arrows indicate the energy transfers between the blocks

Table 2 Model parameters, their values and source references

Variable	Description	Value	Ref.
T_q	Qubit temperature	0.1 K	
T_{cryo}	Cryo temperature	4 K	
T_0	Ambient temperature	300 K	
V_1	Volume @T_q	0.4 cm^3	
V_2	Volume @T_{cryo}	25 cm^3	
U	Cryostat heat transfer coefficient	0.3 $mW/(m^2K)$	[1]
C_1	Geometric constant (cubic volume)	6	[1]
$P_{MUX/DEMUX}$	Power per channel	5.12 $\mu W/line$	[31]
P_{an}	Power per each input/output line	3.375 $mW/line$	[32]
$\dot{Q}_{1max}$	Transferred heat per second @T_q	1 mW	[33]
$\dot{Q}_{2max}$	Transferred heat per second @T_{cryo}	2 W	[33]
$\dot{Q}_{3max}$	Transferred heat per second @T_{hot}	10 kW	
$n_{int\,3\leftrightarrow2}$	Nr. of interconnections between @T_{hot} and @T_{cryo} sections	64	
$\dot{q}_{int\,i\rightarrow j}/\Delta T_{ij}$	Heat load over the temperatures difference	3 $\mu W/K$	[1]
η_C	Fraction of Carnot efficiency achieved by the cryogenic section	0.03	[1]
ϕ	Split in power between cryo and non-cryo electronics	0.001	[1]
$COP(T_i)\|_C$	Carnot coefficient of efficiency of i-th cryogenic cycle	$T_i/(T_0 - T_i)$	[1]
$FOM(T_0)$	Figure of merit for cooling ambient electronics	5	[1]

The total power required is written as

$$P_T = P_c + \sum_{i=1}^{3} \dot{W}_i \tag{17}$$

with the computational power equal to

$$P_c \equiv P_1 + P_2 + P_3 = n\dot{q}, \tag{18}$$

where

$$P_1 = \frac{n}{2d^2 - 1} \frac{E_Z + E_X}{t_{cycle}} + P_{MUX/DEMUX} n_{int\,2\leftrightarrow1}, \tag{19}$$

is the power related to the cryogenic electronics at 0.1 K. The first term in Eq. (19) represents the power required for controlling and reading out all n FF qubits coded with a SC, whereas the second term refers to the MUX/DEMUX power. The power per channel $P_{MUX/DEMUX}$ has the value specified in Table 2, and the number of interconnection lines $n_{int\,2\leftrightarrow1}$ is derived as in Ref. [31]. More specifically, we used the same MUX/DEMUX circuitry of the control section for the readout one. Therefore, we obtain $n_{int\,2\leftrightarrow1} = n_{int\,2\leftarrow1} + n_{int\,2\rightarrow1}$ where $n_{int\,2\rightarrow1} = CX + 4k$ is the total number of global and local control lines entering the DEMUX. Here, $X = (\log(n^2k))/(M\log(2))$ is the number of shift registers, with C representing the number of control lines to each M bit serial-in parallel-out shift register and k the number of local lines ($C = 4$, $M = 8$, $k = 3$). $k = 3$ corresponds to the number of local input pads I in the qubit layout of Fig. 1(c). Correspondingly, the readout outputs that exit the MUX are $n_{int\,2\leftarrow1} = CX + 4k$ with $k = 1$ because only a single local output pad O is considered, as depicted in Fig. 1(c).

The power of the cryogenic electronics at 4 K is given by

$$P_2 = \frac{n}{2d^2 - 1} \frac{E_{decSynd}}{t_{cycle}} + P_{an} n_{int\,2\leftrightarrow1}, \tag{20}$$

where the first term includes the power of digital electronics for SC error syndrome decoding, while the second term includes the power of all analog electronics (LNAs, ADCs, mixers, Local Oscillators (LOs) and DACs). P_{an} is a lumped parameter for power per each input/output line. It has been derived using the value reported in Ref. [32] related to the control (output) lines and is multiplied by 2 to account for the commonly higher power required for qubit readout (input) lines. The derived value is reported in Table 2.

The power for the RT electronics is modeled as in Ref. [1] and written as

$$P_3 = \frac{1-\phi}{\phi}(P_1 + P_2), \tag{21}$$

with ϕ, representing the split in power between cryo and non-cryo electronics, set to a constant value.

The transferred heat per second between the different sections of the system is obtained as:

$$\dot{Q}_1 = P_1 + \dot{Q}_{2\to1}, \tag{22}$$

$$\dot{Q}_2 = P_2 + \dot{Q}_{0\to2} - \dot{Q}_{2\to1}, \tag{23}$$

$$\dot{Q}_3 = P_3, \tag{24}$$

with

$$\dot{Q}_{2\to1} = UC_1(T_{cryo} - T_q)V_1^{2/3} + n_{int\,2\leftrightarrow1}\dot{q}_{int\,2\to1}, \tag{25}$$

$$\dot{Q}_{0\to2} = UC_1(T_0 - T_{cryo})V_2^{2/3} + n_{int\,3\leftrightarrow2}\dot{q}_{int\,0\to2}. \tag{26}$$

Finally, the required powers to keep constant the temperatures in the different sections entering also in Eq. (17), are defined as follows [1]:

$$\dot{W}_1 = \frac{P_1 + \dot{Q}_{2\to1}}{\eta_C COP(T_q)|_C}, \tag{27}$$

$$\dot{W}_2 = \frac{P_2 + \dot{Q}_{0\to2} - \dot{Q}_{2\to1}}{\eta_C COP(T_{cryo})|_C}, \tag{28}$$

$$\dot{W}_3 = \frac{\dot{Q}_3}{FOM(T_0)}. \tag{29}$$

Figure 9 reports the results for P, $\dot{Q}$ and $\dot{W}$ as a function of the physical qubit number n. These quantities are detailed for the different sections at T = 0.1, 4 and 300 K (rows) and for different code distances d = 9, 13 and 17 (columns).

We note that the P_3 and $\dot{Q}_3$ curves overlap, as stated in Eq. (24). A remarkable point is where the red curve intersects the constant dashed line. This intersection represents the maximum number of qubits $n|_{\dot{Q}_{imax}}$ achievable under the given constraint $\dot{Q}_{imax}$, indicating a significant threshold for design considerations. Then, the maximum number of implementable physical qubits n_{max}, satisfying all the constraints, is obtained by taking the closest smaller integer to the minimum among those obtained in each section:

$$n_{max} = min(n|_{\dot{Q}_{1max}}, n|_{\dot{Q}_{2max}}, n|_{\dot{Q}_{3max}}). \tag{30}$$

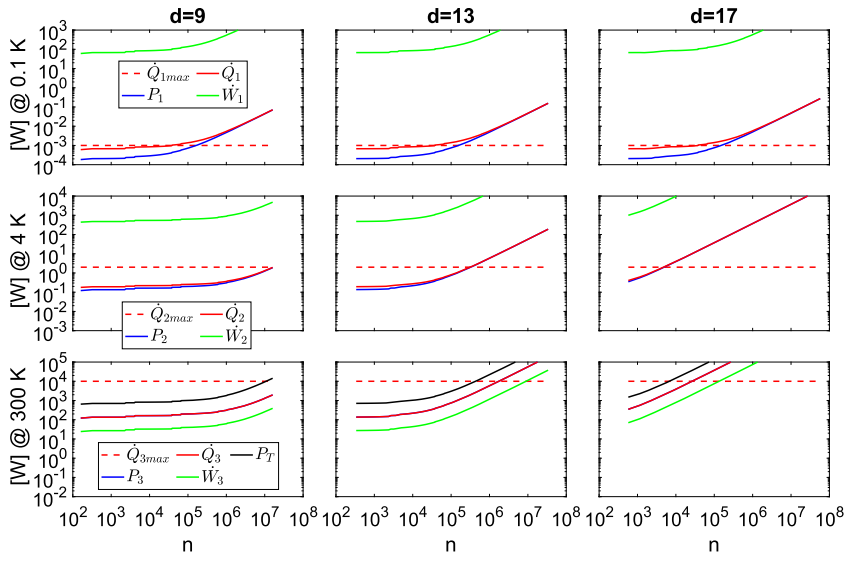

Figure 9 P, $\dot{Q}$ and $\dot{W}$ as functions of the physical qubit number n. P_i, $\dot{Q}_i$ and $\dot{W}_i$ are detailed for the $T = 0.1$, 4 and 300 K sections (rows) and for $d = 9$, 13 and 17 (columns). In the last row, the total power P_T (black line) is also shown

Table 3 Power consumption for state-of-the-art quantum computers based on different qubit technologies

Qubit type	Cryogeny [kW]	Qubit gate control [kW]	Computing [kW]	# Qubit	Total [kW]
Trapped ions	$300{\cdot}10^{-3}$-6	<1.4	$300{\cdot}10^{-3}$	24	2
Cold atoms	8-10	5.8	1	100-1000	7-20
Superconductor	16-105	$2{\cdot}10^{-5}$-10^{-1} (per qubit)	1	53-433	25-140
Silicon (single-spin)	12	$2{\cdot}10^{-5}$-10^{-1} (per qubit)	1	12	21
Photons	3	$300{\cdot}10^{-3}$	$700{\cdot}10^{-3}$	20	4

Using the results obtained, we estimate a computational power per qubit $\dot{q} = P_c/n_{max}$ between 4.47 and 406 mW/qubit for d = 9 and d = 17, respectively.

To compare our results with the current literature, Table 3 shows the power consumption of each system section for the types of quantum computers that are currently available, as reported in Ref. [34].

In the case of silicon, which is the smallest system among those reported in Table 3 and is made up of 12 qubits defined in the spin states of an electron confined in electrostatically defined QDs [35], a value of 183 W/qubit is derived by adding the computing and gate control powers and dividing it by the number of qubits. The $\dot{q}$ values estimated in our study, within the hundreds of mW/qubit range, are definitely lower than the value derived from Table 3, reinforcing the significant scaling potential of silicon technology.

Future research will investigate a comprehensive optimization of the different resources for a quantum computer utilizing FF qubits, focusing on a particular metric affected by a specific noise level, in line with the method outlined in Ref. [2].

Then, by focusing on the logical qubits counting, the maximum number of logical qubits n_{Lmax} is obtained as

$$n_{Lmax} = \left\lfloor \frac{n_{max}}{2d^2 - 1} \right\rfloor . \tag{31}$$

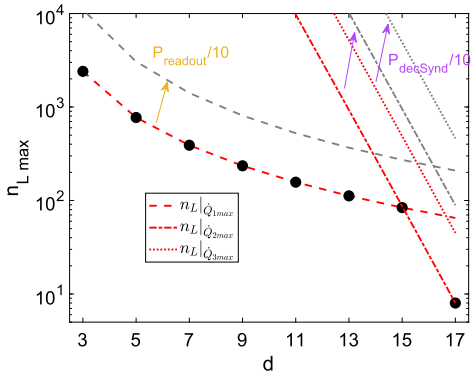

Figure 10 Full circles represent the largest number of logical qubits n_{Lmax} for which all the constraints $\dot{Q}_i \leq \dot{Q}_{imax}$ for $i = 1, 2, 3$ are satisfied, vs. the code distance d. The dashed, dot-dashed and dotted red curves represent the maximum number of allowed logical qubits if only $\dot{Q}_{1max}$ or $\dot{Q}_{2max}$ or $\dot{Q}_{3max}$ holds, respectively. The gray curves represent the new limits if a ten-fold reduction in the readout power or syndrome decoding power could be achieved

Figure 11 P_1, P_2, P_3, P_c and P_T as a function of the maximum number of logical qubits n_{Lmax}

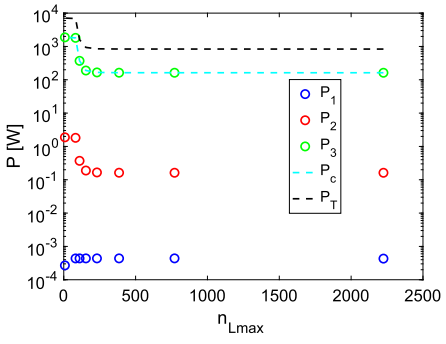

Figure 10 shows n_{Lmax} as a function of d along with the n_L limiting curves if only $\dot{Q}_{1max}$ or $\dot{Q}_{2max}$ or $\dot{Q}_{3max}$ holds. An obvious reduction in n_{Lmax} is observed as d increases, being mainly limited by $\dot{Q}_{1max}$, with values ranging from 2225 to 82 logical qubits when d increases from 3 to 15, respectively. n_{Lmax} is limited to 8 logical qubits by $\dot{Q}_{2max}$ only when $d = 17$. Moreover, additional curves for ten-fold reductions in readout power or syndrome decoding power are also included in Fig. 10, showing how a significant reduction of the most dominant limiting factors would affect n_{Lmax}. A reduction in the current flowing through the SETs could help minimize $P_{readout}$, but at the expense of a worse signal-to-noise ratio. Another qubit readout approach to reduce the $E_{readout}$ could be the exploitation of radio frequency reflectometry on a nearby QD coupled to the qubit, avoiding SET implementation and thus its energy dissipation [8]. Regarding the power reduction associated with SC syndrome decoding, it would be beneficial to consider low power cryogenic ASICs, specifically designed for the syndrome decoding task. Obviously, an increase in each $\dot{Q}_{imax}$ ($i = 1, 2, 3$) would surely benefit the scaling-up of the system, underlining the importance of advancements in cryostat technology [33].

To complete our analysis, Fig. 11 shows the separate contributions of the powers associated with the cryogenic (P_1 and P_2) and RT (P_3) sections, as well as the computational power (P_c) and the total power (P_T) as a function of n_{Lmax}.

As expected, $P_1 < P_2 < P_3$ with P_3 being the dominant contribution to P_c. The powers in the different sections of the system remain basically constant for quantum computers with more than 200 logical qubits ($d < 9$), showing a total power P_T in the 848 - 834 W range. Systems with a smaller memory capacity, below 200 logical qubits but higher code distance ($d \geq 9$), generally show higher powers than the previous ones in the different sections, with a P_T up to 7.1 kW for $d = 17$.

5 Conclusions

In this paper, we estimated the power and energy requirements for quantum computers based on silicon FF qubits by integrating analyses of gate fidelity, error correction, and thermal management.

Using the Hamiltonian model with realistic noise levels for FF qubits, we chose the rotated SC as the QEC code and evaluated the logical error along with the average power consumption.

We presented an architecture for a quantum computer and extended a thermal model for the system. This model accounted for all power and heat contributions, enabling a comprehensive evaluation of thermal constraints. Through this analysis, we identified the most significant limiting factors affecting scalability, demonstrating the maximum achievable numbers of physical and logical qubits under current technological and thermal boundaries. We estimated the computational power per qubit to be between 4.47 and 406 mW/qubit for d = 9 and d = 17, respectively, which is considerably lower than the state-of-the-art values associated with silicon technology, highlighting its substantial scaling capability. We showed that quantum computers with memory capacities ranging from 2225 logical qubits (for d = 3) to 8 logical qubits (for d = 17) are feasible, with total power requirements ranging from 834 W to 7.1 kW.

These results pave the way for the development of large-scale quantum computers based on FF qubits with reduced power consumption. By reducing power consumption per qubit and improving thermal management, quantum processors could scale to support more FF qubits while addressing crucial thermal challenges. The theoretical analysis presented here provides a first quantitative estimate of the energies involved, and the adopted thermal model could be further extended to predict more realistic scenarios based on more than two cryogenic stages.

Practical solutions for efficient cooling and power demands are essential, such as developing more energy-efficient cooling methods, optimizing qubit architectures to reduce power requirements, and integrating advanced materials and low-power electronics. As an example, a readout performed using radio frequency reflectometry instead of a SET could reduce energy dissipation. Overcoming these limitations is crucial for the practical scalability of quantum computers in real-world applications.

Abbreviations

FF, Flip-Flop; SC, Surface Code; QEC, Quantum Error Correction; QD, Quantum Dot; EDSR, Electric Dipole Spin Resonance; SET, Single Electron Transistor; CMOS, Complementary Metal-Oxide-Semiconductor; H, Hadamard; LNA, Low Noise Amplifier; ADC, Analog to Digital Converter; DAC, Digital to Analog Converter; MUX, MUltipleXer; DEMUX, DEMUltipleXer; LO, Local Oscillator; ASIC, Application Specific Integrated Circuit; PC, Personal Computer.

Author contributions

Conceptualization: MDM. Code development and results analysis: MDM and EF. Writing of the paper: MDM and EF. All authors have read and approved the final manuscript.

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Data Availability
No datasets were generated or analysed during the current study.

Declarations

Competing interests
The authors declare no competing interests.

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