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The CDF TESTCLK Module – Providing System Level Clocking and Triggering for Run 2 Prototyping Crates

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Abstract

The TESTCLK module was specifically designed for use in prototyping crates for the Colliding Detector Facility (CDF) Run 2 Experiment at Fermi National Accelerator Laboratory. The TESTCLK Module allows the user to supply system clocks and trigger signals to stand-alone crates.

This module has allowed designers of the CDF Run 2 electronics to thoroughly test their modules, despite the lack of a DAQ system supplied clock and trigger interface. This paper will explore the features that were found important to incorporate into the TESTCLK, and describe how they were implemented.

The paper will also describe how the TESTCLK module has been used to support the initial implementation of the DAQ system at CDF. This has allowed data taking and testing of CDF Electronic modules before production clock and trigger modules became available.

I. INTRODUCTION

The TESTCLK module was designed to allow the user to work with modules that require the signals from the CDF Master Clock[1] and the Trigger System Interface[2] (TSI), in a test crate where one or both of these facilities are not available.

The TESTCLK can provide the clock and trigger signals directly to the backplane of the CDF Run 2 Crate[3], or provide front panel connections to feed a TRACER[4] module. The TRACER module is the board used in the runtime data acquisition system to receive and distribute the clock and trigger signals.

The TESTCLK is meant for use in teststands where prototype or production checkout is taking place. It will not be used during normal data acquisition.

II. THE CLOCK GENERATOR

A main function of the TESTCLK module is to provide system level clocking. By definition, this implies delivering a stable and precise 132 ns 50% duty cycle clock, CDF_CLOCK, as well as three clock gates. The clock gates are markers for Beam Zero (a once around marker), Beam Crossing (an active crossing marker), and Abort Gap (the abort gap marker). The clock gates are validated by the rising edge of the CDF_CLOCK signal, and must be implemented such that they provide a minimum of 10 ns setup and hold time.

Figure 1 provides a general block diagram of the TESTCLKs clock generation scheme. A delay line on the output stage is used to adjust the phasing of the clock signals to the trigger signals.

A. External Clock Source

The clock generator of the TESTCLK can derive the 132 ns clock and its gates through one of three sources. First, it can receive the clocking signals from the real CDF Master Clock System. This option might be used, if the Master Clock was available, but the TSI was not. The TESTCLK would then be used to provide trigger signals. In this case, the TESTCLK receives the clock and gates on a front panel connector using the standard clock cable.

If the above method is used, it is possible to synchronize several crates by running the Master Clock signals into a TESTCLK. The TESTCLK would then make use of the Master Clock signals to run its internal logic which controls the outputting of trigger signals.

For instance, to synchronize the operation of several different crates, the user could download the same trigger pattern to multiple TESTCLKs in different crates. The trigger pattern could then be executed upon the receipt of a validated Beam Zero clock signal.

B. Internal Clock Source

In the absence of the CDF Master Clock, the TESTCLK can make use of an internal oscillator to provide the 132 ns clock. When the oscillator is used to provide the CDF_CLOCK signal, the user must supply the clock gates.

A clock gate pattern can be downloaded into Flash RAM. It is necessary to download a pattern that is 159 stages deep. This number represents the number of bunches on a once around the beam accelerator trip. The internal logic of the TESTCLK will simply treat the Flash RAM as a circular buffer and output the contents of successive address locations every 132 ns.

The TESTCLK is delivered to users with a default pattern in the Flash RAM which matches expected operating conditions.

[1]Work supported by the U.S. Department of Energy under contract No. DE-AC02-76CH03000.

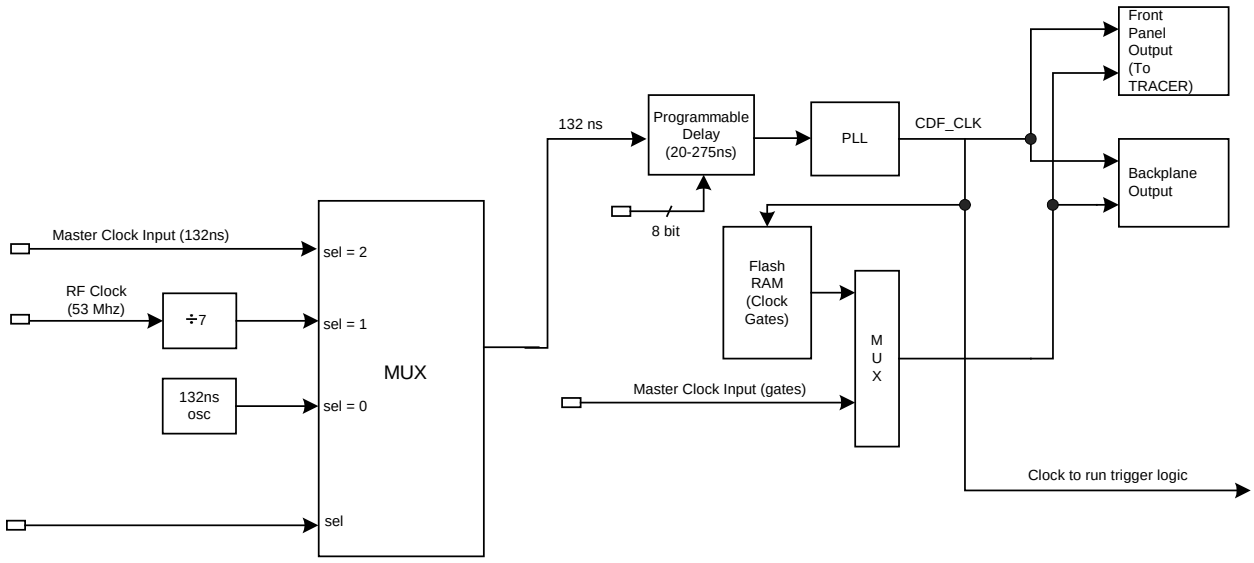

Figure 1. MC and TSIE Clock Sources

The internal clock source should be selected if the user is working with a single crate and no Master Clock signals are available. The majority of prototyping teststand crates would use this method.

C. RF Clock Source

The TESTCLK also provides the ability to use the 53 Mhz RF signal which is provided by the accelerator to produce the 132 ns CDF_CLOCK. In this case, the TESTCLK will receive the 53 Mhz clock and produce clock which is phase locked and divided by 7. This yields the desired 132 ns CDF_CLOCK.

Just as in the case of the internal oscillator, the user must rely upon the Flash RAM to provide clock gating signals.

This clock source should be selected when the user is doing something which requires them to be synchronizeded to accelerator beam operation.

III. TSI EMULATOR

The TSI Emulator (TSIE) portion of the TESTCLK, represented in Figure 2, allows the user to download a desired trigger pattern and to have it run upon a software command or external input.

The output of the TSIE, the trigger sequence, can be sent to a TRACER through the optical interface on theTESTCLK's front-panel or the data is can be decoded and asserted on the CDF backplane.

By using an optical splitter on the TESCLK's front-panel output, optical trigger data can be sent to multiple TRACERs, each residing in a separate crate.

A TESTCLK user is, thus, able to issue a wide variety of commands and L1 and L2 data accepts and control data flow within their own crate.

A. System Protocol for sending Trigger Signals

The protocol for sending trigger signals to the CDF Run 2 readout crates from the Trigger System Interface (TSI) involves sending two 9-bit trigger words every 132 ns. One of these words indicates whether a Level 1 Accept has occurred. The second word is either a synchronization word or a special command, such as an order to execute a calibration sequence.

The protocol to send these 9-bit command word involves the use of TaxiChip serializing protocol and optic fibers for data transmission.

In normal running mode, the TRACER module receives the TSI optical fiber. The TRACER would then decode the data and place it on the backplane.

When using the TESTCLK, the user can choose to put the data directly unto the backplane or to send serialized data out a fiber optic front panel connection. The front panel connection allows the data to be fed directly to a TRACER module.

B. Sending a simple TSIE Pattern

The TESTCLK uses up to two FIFOs to store and execute trigger patterns. In the simplest operation, one of the FIFOs is loaded with a pattern of 9-bit words which represent the 9-bit serialized commands sent by the TSI. After loading the FIFO with a trigger sequence, a command could be issued to enable the trasmission of the FIFO data. The data would either go through the TaxiChip transmitter and out the front

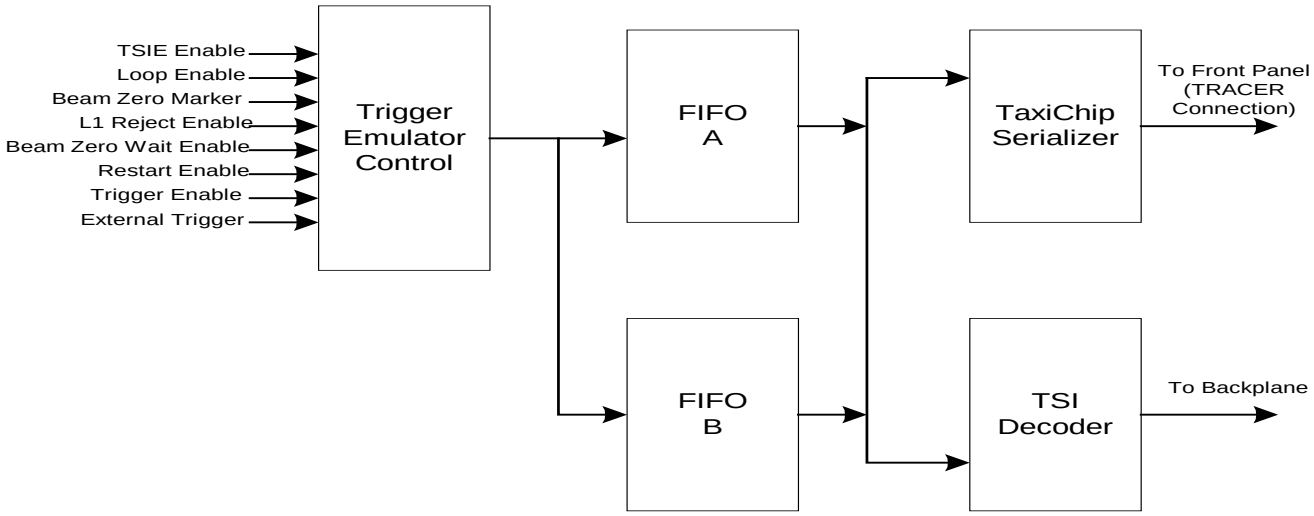

Figure 2. Block Diagram of the TSI Emulator

panel to a TRACER, or it would go through internal trigger word decoder logic and onto the backplane. The trigger word decoder logic on the TESTCLK is identical to the decoder logic on the TRACER.

An example of a simple trigger pattern which would be loaded into the FIFO would be as follows:

" Example of

" Halt/Reset/Run Sequence

0x007 "Control Word : HALT

0x000 "L1 Word – Null

0x00B "Control : RECOVER

0x000 "L1 Word - Null

0x023 "Control : RUN

0x000 "L1 Word – Null

…

The data loaded into the FIFO would be the hexidecimal numbers. The encoded meaning would be to issue a Halt-Recover-Run command sequence.

It is possible to send a looping trigger pattern from the TSIE by setting a loop enable bit. It is also possible to cause the transmission out of the FIFO to be held up until the control logic sees a Beam Zero Marker. This second feature allows us to do some synchronization among multiple modules and crates.

C. Sending a Triggered TSIE pattern

Another method of sending a trigger pattern is to make use of an external trigger. This is of course very useful when trying to do physics with the TESTCLK.

To set the TESTCLK up for a typical physics application, the user would make use of both TSIE FIFOs. FIFO B would be loaded with a pre-trigger command. This would consist of something like a Halt-Recover-Run command which would reset all electronics and get a crate ready for data taking.

FIFO A would contain the post-trigger command sequence. This sequence would typically contain L1 and L2 accept commands.

The user would then set a bit to force the TESTCLK to utilize an external trigger. Now, when the TSIE is enabled, its sequencer will cause the execution of the pre-trigger sequence. The TESTCLK will then issue a series of L1 Rejects until it receives an external trigger. The external trigger causes the post-trigger sequence to be executed.

The user is now able to read out the data for which they have issued a L1 and L2 accepts.

The entire sequence can be restarted again, after data is readout, by simply issuing another go command to the TSIE.

IV. The Bus Monitor

The TESTCLK also provides a CDF Run 2 backplane monitor on its front panel. It brings CDF_CLOCK, as well as all clock and trigger gates to multi-conductor connectors which easily interface to a logic analyzer.

V. Conclusion

The TESTCLK module has been used very successfully with prototype crates of various CDF collaborators.

Additionally, it is boot strapping the beginnings of the CDF DAQ system for Run 2. The TESTCLK has been used in test beam operation to collect and analyze data. It has allowed early analysis of calorimetry data.

VI. REFERENCES

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