



Intelligent Front-end Electronics for Silicon photodetectors (IFES)



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ABSTRACT

While high channel density can be easily achieved for big experiments using custom made microchips, providing something similar for small and medium size experiments imposes a challenge. Within this work we describe a novel and cost effective solution to operate silicon photodetectors such as silicon photo multipliers (SiPM). The IFES modules provide the bias voltage for the detectors, a leading edge discriminator featuring time over threshold and a differential amplifier, all on one printed circuit board. We demonstrate under realistic conditions that the module is usable for high resolution timing measurements exploiting both charge and time information. Furthermore we show that the modules can be easily used in larger detector arrays. All in all this confirms that the IFES modules are a viable option for a broad range of experiments if cost-effectiveness and small form factor are required.

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1. Introduction

One of the main challenges that small and medium sized experiments face is reading many detector channels with high channel density and for a reasonable price. The big experiments can solve this issue by construction of application specific integrated circuits (ASIC) like the NINO [1] chip, the SPIROC [2], or the MAROC [3]. Developing or operating an ASIC is not realistic for experiments with low channel density, therefore standard equipment is used. A typical setup for operating silicon photo multipliers (SiPMs) for a small or medium sized experiment consists of a bias supply, a discriminator and an amplifier for every readout channel in the setup.

To address this problem a small versatile and compact front-end module was developed. The Intelligent Front-end Electronics for Silicon photodetectors (IFES) module is made of standard, industry grade and off the shelf available components. The IFES module features a current stabilized bias voltage source, a broad band differential amplifier and a leading edge discriminator with time over threshold (ToT) signal for very affordable production costs of less than 50 Euros per channel. Current boards feature two channels with an overall dimension of $80 \times 32 \text{ mm}^2$. The system can be remotely controlled for both bias voltages and discriminator thresholds. For basic operation without remote control the only connection required is the one to the detector and to an

ADC or TDC readout module afterwards. The IFES module provides an easy to use, cost-effective, high channel density and low noise detector readout.

2. Hardware and operation

2.1. Electronics

In Fig. 1 the block diagram of the IFES modules is shown. Section A displays the relation of the bias voltage supply, differential amplifier and leading edge discriminator. Section B shows the main power supply of the board and Section C shows the internal bus system.

The bias voltage is produced by a Boost DC/DC converter (Linear Technology LT3482¹). The output of the converter produces a feedback loop with the aid of a current mirror. Together with a current amplifier this ensures that the bias voltage is stabilized while being controllable via a digital to analogue converter (DAC). A bias voltage calibration is foreseen, by measuring the dark current on the measuring port (compare Fig. 2), and tuning the bias voltage till a defined dark-current is reached. The pulse produced by the SiPM is read out as differential balanced signal over a twisted pair cable. The differential signal is received by a broad band amplifier (Analog Devices AD8351). We measured that the

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¹ Special caution is required when placing the IFES module in strong magnetic fields, as the LT3482 requires an inductance of 10 μH for operation.

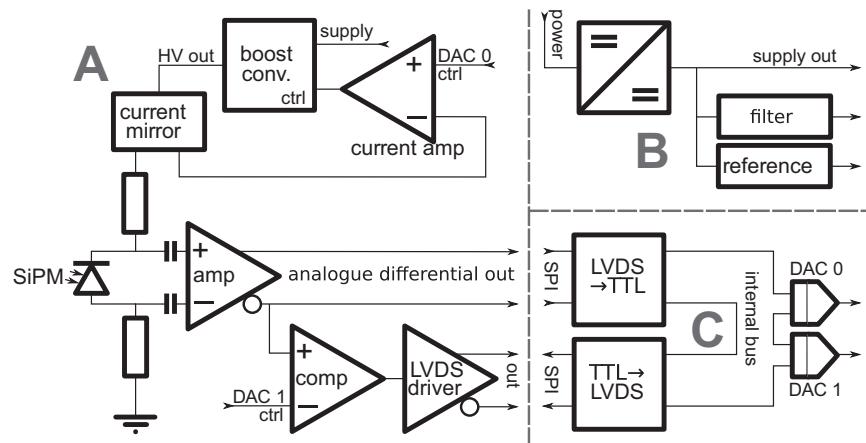


Fig. 1. IFES block diagram. (A) Detector bias, differential amplifier and comparator, the signal is produced within the detector marked as SiPM. (B) Power supply with filter and reference voltage. (C) Control bus with daisy chain capability and DAC connections.

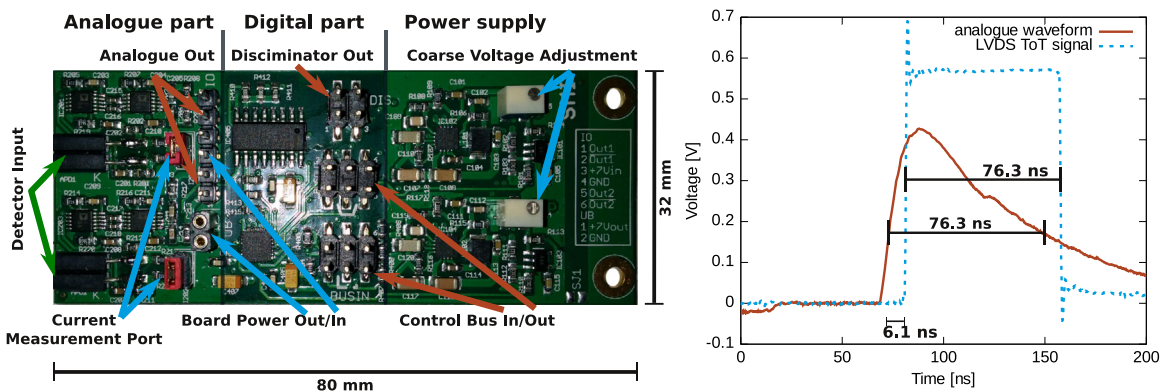


Fig. 2. Left: Photograph of a fully assembled IFES module with detector inputs in green, signal inputs and outputs in red and power/bias components in blue. Right: A typical analogue waveform measured with a CEAN V1742 waveform digitiser (solid) The digital ToT pulse (dashed) was converted from LVDS to NIM standard for the measurement with the V1742.

differential setup allows for a cable length up to 50 cm between SiPM and IFES module without signal distortion. In case no precise timing is required the cable length can be up to 10 m for counting experiments. The input stage has similar features as the NINO [1,4] chip. After the amplification stage the signal is provided to the user as analogue differential signal. This signal is fed to the leading edge discriminator.

Noise reduction was one of the main design goals for the IFES module. To ensure proper operation in harsh environments like accelerator facilities all signals are differential. This also suppresses the formation of ground loops between detector and IFES module and between the IFES module and the readout electronics. Following the LVDS standard, the connection can withstand a potential difference of ± 1 V between transmitter and receiver ground. It follows that good grounding is essential for successful operation of the experiment. If required, the IFES modules can be grounded by closing a soldering bridge on the board.

By changing a single resistor on the boards the IFES modules can be adapted to support various detector types with a bias voltage up to 90 V. Most SiPMs currently available on the market operate with a bias voltage between 20 V and 70 V. Depending on the model two to three SiPMs can be operated in serial connection. Under normal conditions the amplification of the boards is fixed. If required it is also possible to change fixed amplification by replacing one resistor on the board. In Fig. 2 a fully assembled IFES module with two channels is displayed on the left side. The right graph shows a typical signal produced by an IFES module in combination with an Advansid ASD-RGB3S-P (3×3 mm² active

surface) and a plastic scintillator (EJ-200). The measurement was done with a CEAN V1742 waveform digitizer. To simultaneously record the digital ToT pulse the LVDS signal was converted to a NIM signal. The rise time (10–90%) of the analogue signal is 6.1 ns.

2.2. Operation principle

The modules are constructed in a way to allow the readout of large detector arrays. This is done by daisy-chaining several modules. The supply voltage for the modules can be connected from one module to the next allowing the supply of several modules by one low voltage power supply (7–20 V). The slow control of the boards can be done with any micro controller or single board computer featuring the serial peripheral interface (SPI) bus. Connecting the control bus in a daisy chain was made possible by the choice of a DAC (Maxim Integrated MAX5135) that issues a ready signal after an instruction is processed. This ready signal is used to select the DAC chip on the next IFES module in the daisy chain. The LVDS drivers ensure proper quality of the signals even for long signal paths. This was tested for cable lengths up to 10 m under laboratory conditions and in an accelerator environment.

By issuing sequential commands to the on-board DACs the controller can set all bias voltages and thresholds individually. Theoretically, the design does not limit the number of channels per controller. In case of the ASACUSA [5] antihydrogen detector [6] at the CERN antiproton decelerator (AD) facility 128 channels

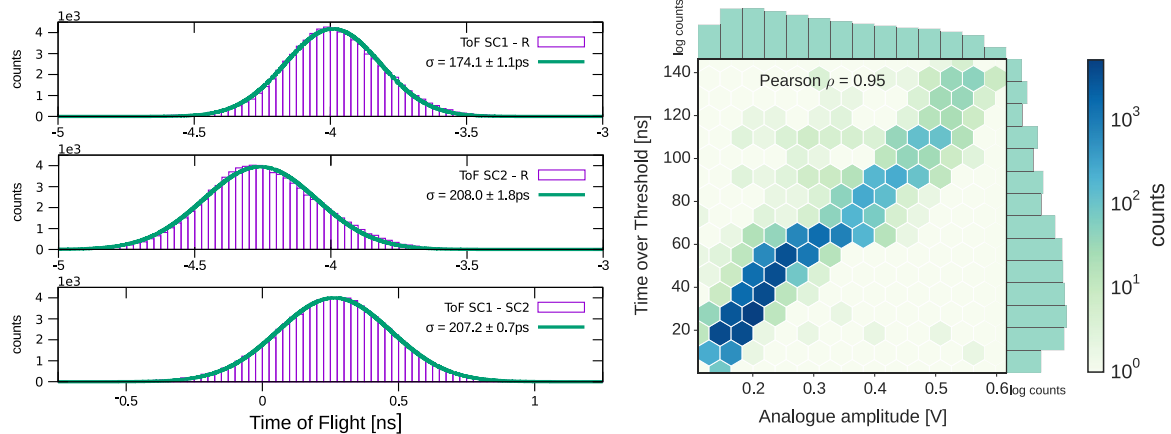


Fig. 3. Left: Time of flight measurements between the scintillators (SC1 and SC2) and a mean time reference counter (R). Right: Correlation between analogue pulse height and ToT. The bin content for the bivariate histogram and both marginalised distributions is on a logarithmic scale to emphasize the correlation. The Pearson product–moment correlation coefficient ρ is 0.95.

resulting in 64 modules were successfully operated by a single Arduino micro controller board.

3. Test results

3.1. Experimental setup

Measurements for timing resolution have been performed in January 2014 as a parasitic experiment at the JESSICA beamline at the COSY facility of the Forschungszentrum Jülich in Germany with a 1.471 GeV/c proton beam. The tests were done using EJ-232 (SC1) and EJ-228 (SC2) scintillators with dimensions $28.5 \times 28.5 \times 5$ mm³ as detector material. KETEK 3350TS and KETEK 3360TS SiPMs (3×3 mm² surface area and 50×50 μ m² and 60×60 μ m² micropixel size and optical trench separation) were used as photodetectors [7,8]. The SiPMs were mounted on opposite sides on the center of the small surfaces of the scintillator. All signals were recorded using CAEN V1742 VME waveform digitizers operated at 5 GHz sampling rate. The analysis of the waveforms was performed using a self-library [9], ROOT [10] and rootpy [11]. The bandwidth was limited by a software Fourier filter to 204 MHz.

Further tests for the correlation between digital ToT signal and analogue pulse height have been performed in the laboratory with an oscilloscope.

3.2. Performance

For evaluation of the timing performance the time of flight (ToF) spectra between the reference counter and the detectors SC1 and SC2 and in between those detectors were measured. The reference signal was produced by calculating the mean time of three scintillators that were read by two photomultipliers each.

The ToF measurements used for the determination of the timing resolution for the detectors is shown within the left graph of Fig. 3. The histograms were created using constant fraction timestamps derived from the analogue waveforms. The time of flight resolution between reference counter and SC1 (EJ-232, KETEK 3360TS) was 174.1 ± 1.1 ps. Between SC2 (EJ-228, KETEK 3350TS) and the reference signal the ToF resolution was 208 ± 1.8 ps and between SC1 and SC2 a resolution of 207.2 ± 0.7 ps was measured. The individual contributions of the detectors were calculated using a likelihood method. SC1 has a timing resolution of $\sigma = 122 \pm 1.3$ ps, SC2 reaches 167 ± 1.0 ps and the reference counter contributes 123 ± 1.3 ps.

During the parasitic test beam experiment the main goal was to test every part of the IFES modules under realistic conditions. The board was evaluated with respect to stability of the analogue and digital signals and reproducibility of bias voltage and discriminator threshold settings. It follows that the achieved timing resolution should be considered as easily achievable with the described detectors without tuning the system for high resolution timing.

The correlation between analogue pulse height and ToT signal features two linear regions. After measuring this relation it is possible to use the ToT signal in combination with a multi-hit TDC to measure charge deposit and timing in the same instance. A measurement of this relation is displayed in Fig. 3 on the right side. Furthermore timewalk correction of the leading edge time–stamp is possible with the ToT signal.

4. Summary

A novel front-end module for silicon photodetectors was developed. The IFES module can be tuned to provide bias voltages up to 90 V. It featured differential silicon photodetector readout and a fully differential signal path hence reducing pickup noise even in hostile environments like accelerator facilities. The modules combine the bias voltage, an amplifier and a discriminator on a single board with dimensions 80×32 mm.

The modules were successfully tested under laboratory conditions and in a beam facility. They are in active use at the anti-hydrogen experiment of the ASACUSA collaboration at the CERN AD where 64 boards are operated by a single micro-controller in a daisy-chain.

Furthermore a per channel price of less than 50 Euro was reached while providing accurate timing capabilities, differential analogue signals, a leading edge time over threshold discriminator and remote control for individual channels.

Acknowledgments

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References

- [1] F. Anghinolfi, et al., IEEE Trans. Nucl. Sci. NS-51 (5) (2004) 1974, <http://dx.doi.org/10.1109/TNS.2004.836048>.
- [2] S. Callier, F. Dulucq, R. Fabbri, C. De La Taille, B. Lutz, G. Martin-Chassard, L. Raux, W. Shen, Silicon photomultiplier integrated readout chip (spiroc) for the ilc: measurements and possible further development, in: Nuclear Science Symposium Conference Record (NSS/MIC), 2009, IEEE, Orlando, Florida, USA, 2009, pp. 42–46. <http://dx.doi.org/10.1109/NSSMIC.2009.5401891>.
- [3] S. Blin, P. Barrillon, C. de La Taille, Maroc, a generic photomultiplier readout chip, in: Nuclear Science Symposium Conference Record (NSS/MIC), 2010 IEEE, Knoxville, Tennessee, USA, 2010, pp. 1690–1693. <http://dx.doi.org/10.1109/NSSMIC.2010.5874062>.
- [4] F. Powolny, et al., IEEE Trans. Nucl. Sci. NS-58 (3) (2011) 597, <http://dx.doi.org/10.1109/TNS.2011.2119493>.
- [5] N. Kuroda, et al., Nat. Commun. 5 (2014) 4089. <http://dx.doi.org/10.1038/ncomms4089>.
- [6] Y. Nagata, et al., J. Phys.: Conf. Ser. 635 (2) (2015) 022061, URL (<http://stacks.iop.org/1742-6596/635/i=2/a=022061>).
- [7] S.E. Brunner, et al., J. Instrum. 9 (03) (2014) C03010, URL (<http://stacks.iop.org/1748-0221/9/i=03/a=C03010>).
- [8] L. Gruber, Studies of sipm photosensors for time-of-flight detectors within panda at fair (Ph.D. thesis), Technische Universität Wien, 2014.
- [9] C. Sauerzopf, Waveformlibrary v1.0.0, December 2015, <http://dx.doi.org/10.5281/zenodo.35341>.
- [10] R. Brun, F. Rademakers, Nucl. Instrum. Methods Phys. Res. Sect. A: Accelerat. Spectromet. Detect. Assoc. Equip. 389 (1–2) (1997) 81, [http://dx.doi.org/10.1016/S0168-9002\(97\)00048-X](http://dx.doi.org/10.1016/S0168-9002(97)00048-X), New Computing Techniques in Physics Research V URL (<http://www.sciencedirect.com/science/article/pii/S016890029700048X>).
- [11] N. Dawe, et al., rootpy: 0.8.0, June 2015, <http://dx.doi.org/10.5281/zenodo.18897>.