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PROTOTYPE FLASH ADC SYSTEM FOR CDF VERTEX TIME PROJECTION CHAMBER

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ABSTRACT

A prototype FASTBUS flash ADC system has been developed for readout of the CDF vertex time projection chamber, VTPC. The system has 8-bit flash ADC's and its sampling rate is up to 30 MHz. A cluster finding is made in a hardware module to reduce the data size without loss of the waveform information. We describe the design of the system, and report its performance.

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1. Introduction

Typical 4π detectors for high energy colliding beam experiments today have three-dimensional tracking chambers. Readout of the output waveform from these tracking chambers provides useful information for reconstruction of tracks. Charge coupled devices (CCDs) [1] and flash analog-to-digital converters (FADCs) [2] are powerful devices for the waveform readout. In CCD system, however, a complicated pedestal subtraction is required to eliminate the dark current effect [1]. Furthermore, the dead time of the CCD system is generally large. On the other hand, FADCs are expensive and reasonable cost has been limited for devices with 6 bits or less. Recently, several kinds of 8-bit FADCs become commercially available [3]. They have advantages both in precision and the dynamic range. Cost down in mass production will make them economically accessible for large scale collider experiments.

A serious problem of the FADC system is in its data size. FADC data usually shares a large fraction of the total data size in the colliding beam experiments. Thus, a hardware processing in the data aquisition stage is desirable to reduce the data size. Such a process so far used in experiments is simply the zero suppression [1,2], in which the data format for each non-zero signal consists of the channel number and the sampling time with the pulse height data. In the case of the pad signals of the time projection chamber (TPC) [4], however, this method is inefficient; induced signals are widely extended and the time durations are long, compared with wire signals. The waveform data forms a cluster both in channel and time directions. This implies that the excessive information about the channel number and

the sampling time can be eliminated by findig a signal cluster, or a chain of non-zero signals, and giving a single headder on a the cluster. This is the scheme used in the present system reported in this papaer. The total data size and the dead time incurred in subsequent processing can be substantially reduced by the cluster finding method.

Two modules of the VTPC, the vertex time projection chamber [5] of collider detector at Fermilab (CDF) [6], are shown in fig. 1. Inner and outer field cages and center HV and P.W.C. cathode grids form uniform electric field along the beam direction (z); here, r, ϕ and z represent cylindrical coodinates. Electrons produced by ionization drift towards proportional chambers, consisting of sense wires and cathode pads, placed at both ends of the module. An avalanche occurs around a sense wire when a drift electron arrives. Signals are induced both in the sense wire and the cathode pads. The z and r positions can be measured by the sense wire signals. The ϕ position is obtained from the data of the pad signals; the center of gravity of the pad ϕ corresponds to the ϕ of the avalanche. Total number of channel of the pad signals is 2912, and the prototype system reported here handles about 1/16 of the whole system. Figure 2 is the block diagram of the front end electronics of the pad readout system. Pad signals are amplified by preamplifiers, LeCroy HQV802s. Then the signals are transferred via coaxial cables to a pad amplifier and shaper board named PAS. The shaper consists of a pole zero circuit and a Gaussian integrator [7] which remove the tail of the pad signal and high-frequency noise of the preamplifier. A main amplifier amplifies the signal and a buffer amplifier drives shielded twisted

pair cable. The signals are then transmitted to the flash ADC system. The pulse height of the FADC input signals is up to 2 V, and the width is 300 ns to 3 μs at fwhm (full width at half maximum).

In this paper, the system is described in section 2, the test of the performance is reported in section 3, and the results are summarized in section 4.

2. FADC system

2.1 Overview of the system

This system is designed to be incorporated into the CDF FASTBUS system [8]. Figure 3 shows a crate segment of the FADC system, schematically. The crate segment is connected to a cable segment via a SLAC scanner processor, SSP [9]. The FADC system consists of two kinds of FASTBUS modules, FADC and Compaction modules. Eight FADC modules are connected to one compaction module by external bus lines. The FADC modules have no FASTBUS protocol logic in themselves. They simply receive dc power from the FASTBUS backplane. Each module receives 24 channels of the pad signals and digitizes them by FADCs. The data are recorded in memories. After this process, the data are transferred to the compaction module via external bus lines. The transfer rate in this process is 50 ns/byte, nominally. The compaction module is a FASTBUS slave module which controls eight FADC modules and compacts the data transferred from FADC modules by a hardware logic. The compacted data are stored in memories. After this process, the data are transferred to the SSP. The dead time by the compacting is estimated to be 380 μs, and the total FASTBUS

readout time is estimated to be 600 μs for CDF VTPC. The dead time for readout, however, is negligibly small for CDF level 2 trigger [10], because the FADC module can be restarted right after compacting.

2.2 FADC module

Figure 4 shows a block diagram of the FADC module. The module has 24 input channels, each channel consisting of a differential receiver, an FADC chip and two memory chips. The defferential voltage gain of the receiver is set to be 1. The FADC chips are Fujitsu MB40547-8s which are ECL 8 bit ones. The FADCs have a small linearity error ($\leq$1/2 least significant bits, LSB), and the nominal sampling rate is up to 30 MHz. The power consumption is relatively low (0.9 W, nominally), and the dimension of the package is small (24 pin dual-in-line package, DIP) compared with other high-speed FADCs. The low power consumption and compact package are necessary for high-density assembly. The reference voltage is applied from FASTBUS -15 V line and droped to -2 V by a diode, two stage regulator in order to avoide contamination by noises produced by logic circuits. Two 4-bit 256-word bipolar random access memories record the digitized waveform data of an FADC. Start, stop and clock signals are received from the front panel. A clock control logic controls sampling of the FADCs and writing of data to the RAMs. FADC module control signals (N1-8, Trst, Ctst, Tdec and Cdec) are received from external bus lines. A readout control logic controls the memory address and channel selection flags. The FADC module is assembled on a four-layer FASTBUS board. Figure 5 shows a photograph of the FADC module. The

analog circuit and digital one are separated carefully to pevent the logic induced noises.

During the digitizing process, the memory address is increasing and the data are written on the memories continuously until a stop pulse arrives. After digitizing, FADC module control signals control the readout of the memories. N1-8 are decoded flags of the module number; the module number is defined for each module from 1 to 8. Trst and Crst are the preset pulses of the address and channel, respectively. When a Trst pulse arrives to the module specified by N1-8, the memory address changes to the one at the end of digitizing. At the arrival of the Crst, the channel number changes to 23. The address of the memories is decreased by Tdec, and the channel number is decreased by Cdec. The data of the memories specified by N1-8, the address and the channel number are transferred to the compaction module through the external bus lines. The LSBs of the address and the channel number are transferred to the compaction module in order to check the error of transmission of the commands.

2.3 Compaction module

A compaction logic is the crucial part of the compaction module. In the design stage, three methods of compaction were compared: zero suppression, ϕ-cluster finding and t-cluster finding. The zero suppression is a conventional method; data above a threshold value are written on memory with the channel numbers and the sampling times. In case of the ϕ-cluster finding, data are scanned along the ϕ-direction and the clusters of data above a threshold are written on memory with headers. The header consists of the module number, the leading

channel number of the cluster, the sampling time and the length of the cluster. The t-cluster finding is almost same as ϕ-cluster finding, except that the scanning is now along the sampling time, t. Examples of the data format of the zero suppression, ϕ-cluster finding and t-cluster finding are shown in figs. 6(a)-(c).

The pad signals of the VTPC are extended both in ϕ and the time; the ϕ width corresponds to about five pads and the time duration is about 400 ns for an avalanche. The data format of the zero suppression has excessive information because each data word has information about the channel and sampling time with the pulse-height data. On the other hand, ϕ-cluster finding has a more compacted data format; the channel and the sampling time information is reduced to each ϕ-cluster. Thus the total data size is expected to be small compared with the zero suppression. Furthermore, the ϕ-cluster finding has an advantage in the ϕ-reconstruction; the data format of this method is convenient to the calculation of ϕ of the avalanche. The data format of the t-cluster finding is almost the same as that of ϕ, but the total data size including the headers is expected to be smaller. A VTPC pad covers eight sense wires, and the pulse duration of the pad signal is long because of the successive avalanches. The total number of the header is expected to be small compared with the ϕ-cluster finding method.

The data sizes of the whole system by three compaction methods were estimated on the basis of a Monte Carlo simulation using CDF off-line package. The results for the high-Pt (70 GeV) jet events and minimum bias events are summarized in table 1. The number of readout channels is assumed to be 2912 with a sampling rate of 20 MHz.

The data size by the t-cluster finding is substantially smaller than that of other methods. Therefore, the t-cluster finding method is cosen in the present system.

A block diagram of the compaction module is illustrated in fig. 7. The compaction module is separated into four parts: an FADC module control part, a compaction logic part, memory and its control part and a FASTBUS protocol. The control part generates FADC module control signals (N1-8, Trst, Crst, Tdec and Cdec) and send them to FADC modules. The compaction part receives the data from FADC modules and compacts them by the t-cluster finding method. Figure 8 shows the circuit diagram of the cluster finding logic. The data are compared with the threshold. The flip flop FF2 detects the leading edge of the t cluster and FF3 detects the trailing edge. The signal $\overline{WD}$ is a flag for writting the data to the memory, and $\overline{WH}$ is the one for writting the header. The memory control part controls memory address and switchs the FADC data and header. The memory of the compaction module consists of eight 4-bit 4096-word bipolar RAMs. When a cluster of data above the threshold arrives, the data are written on the RAMs increasing the address for every four FADC data. At the end of the cluster, a header word which consists of the channel number, the sampling time and the cluster length is written on the RAMs. After the compaction process, the data are transferred via FASTBUS to SSP. At this process, the address of the RAMs is kept decrease. Thus we obtain the data arranged as shown in fig. 6(c).

3. Test of the system

3.1 Test of the FADC module

The FADC modules were tested with a CAMAC system and a personal computer. Figure 9 shows the test system of FADC module schematically. Clock signals were applied by a NIM clock generator and NIM to ECL converter. Start and stop were controlled via an output register and a NIM to ECL converter. Then the analog signal produced by a pulse generator was digitized by the FADC module. The data were read out via a CAMAC test module, a crate controller and a CAMAC interface to a personal computer NEC PC-9801VM2.

The method of the resolution test was essentially the same as Ref. 11. A ramp pulse was generated by a pulse generator. Data ware taken at sampling rates of 20 to 30 MHz. Then the peak of the slope distribution was fitted to the Gaussian shape. The mean values and the widths obtained at 20 MHz sampling rate are shown in fig. 10. They represent the slew rate and the resolution, respectively. The closed circles denote the positive slopes, and the open circles denote the negative ones. The agreement between positive and negative slopes was good. The curve in the figure is drawn to guide the eye. The resolution increases with the slew rate, but it was less than 1 LSB below 40 LSB/sampling. The data at higher sampling rate showed the similar behavior to those at 20 MHz.

The power consumptions for the FASTBUS power lines are listed in table 2. Special attentions were given to the large power consumption and the temperature rise. The power consumption of the RAMs shares a large part of that of the logic part (-5.2 V and -2 V). But the temperature rises of RAMs were not so large, and there was no trouble caused by the temperature rises during the test period (a few months).

The most of the dc power of the analog part is dissipated by the voltage regulators. But the operations of the regulators were stable; the drift of the reference voltage was less than 0.3 mV during the 48 hours continuous run.

3.2 Test of the compaction module

The eight FADC modules and one compaction module were constructed and incorporated into the CDF FASTBUS system [8]. The compaction speed so far achieved was 12.5 MHz (80ns/word). The readout via SSP and the FASTBUS system was sccessful. The FASTBUS transfer rate was sufficiently high; the DS-DK delay of the compaction module was 37.4 ns. The rate of the block transfer was 150 ns/word which was restricted mainly by DK-DS delay of SSP. The power consumption of the compaction module was 50 W.

4. Summary

We have developed a prototype FADC system for readout of the VTPC pad signals. The system has two different types of FASTBUS modules: FADC module and compaction module. The FADC module has 24 channels of 8-bit FADCs, and the sampling rate is up to 30 MHz. The resolution of the FADC module was less than 1 LSB for the input slew rate of below 40 LSB/sampling, and the operation was stable in spite of the large power consumption.

The compaction module is a FASTBUS slave module which reads out the data from FADC modules and compacts them by the t-cluster finding method. A Monte Carlo simulation shows that the total data size is reduced about 1/2 or 1/3 times as small as that of the zero

suppression. Eight FADC modules and one compaction module have been constructed, and they were incorporated into the CDF data acquisition system. The readout via SSP was done successfully. The compaction rate so far achieved is 12.5 MHz, and the FASTBUS block transfer rate is 150 ns/word.

Acknowledgements

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Table 1 Data sizes by the zero suppression, ϕ-cluster finding and t-cluster finding methods for the pad readout of the CDF VTPC. The sampling rate is assumed to be 20 MHz. The number of readout channel is assumed to be 2912.

Compaction method	Minimum bias event	High-Pt jet event
Zero suppression	42	84
ϕ-cluster finding	21	43
t-cluster finding	15	31

Unit: Kbytes

Table 2 Power consumption of the FADC module.

Voltage	Current (A)	Power (W)
+15 V	0.25	3.75
-15 V	1.0	15
-5.2V	12.5	65
-2 V	2	4
	Total:	87.75 W

References

[1] R. C. Jared et al., IEEE Trans. Nucl. Sci. NS-29(1) (1982) 282.

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[3] See for example: S. K. Dhawan, IEEE Trans. Nucl. Sci. NS-33(1) (1986) 77.

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[11] S. K. Dhawan et al., IEEE Trans. Nucl. Sci. NS-31(1) (1984) 818.

Figure captions

Fig. 1 : Two modules of VTPC.

Fig. 2 : Block diagram of the front end electronics.

Fig. 3 : Block diagram of the FADC system. FADC and compaction denote FADC module and compaction module, respectively. SSP is a scanner processor module (Ref. 9).

Fig. 4 : Block diagram of the FADC module.

Fig. 5 : Photograph of the FADC module. Differential receivers are placed upper and lower ends followed by FADCs and RAMs. Logic circuits are placed in the center.

Fig. 6 : Examples of the data format of the (a) zero suppression, (b) ϕ-cluster finding and (c) t-cluster finding methods.

Fig. 7 : Block diagram of the compaction module.

Fig. 8 : Circuit diagram of the cluster finding logic.

Fig. 9 : Block diagram of the test of the FADC module.

Fig. 10 : Resolution of the FADC module as a function of the input slew rate.

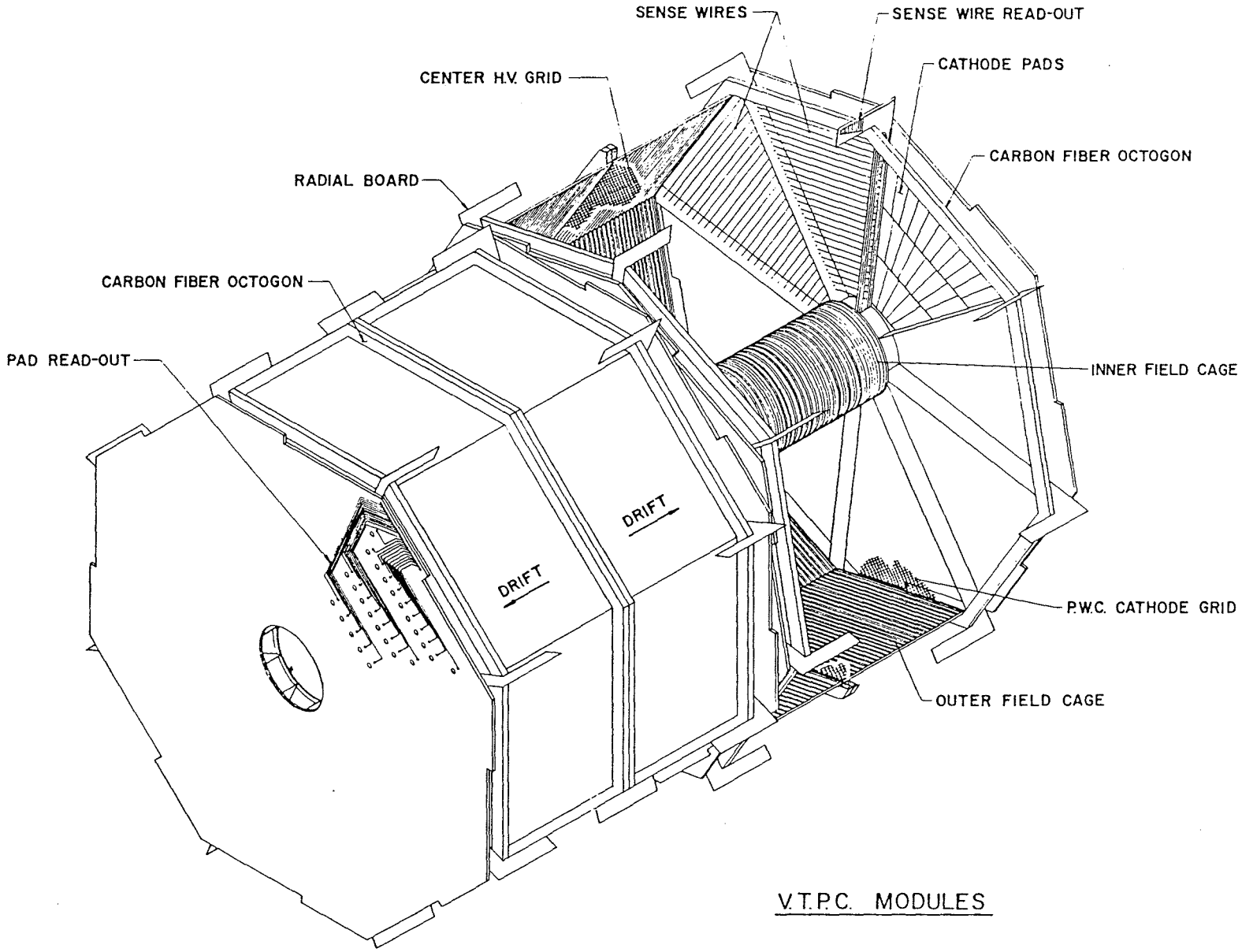

SENSE WIRES
SENSE WIRE READ-OUT
CATHODE PADS
CENTER H.V. GRID
CARBON FIBER OCTOGON
RADIAL BOARD
CARBON FIBER OCTOGON
PAD READ-OUT
INNER FIELD CAGE
DRIFT
DRIFT
P.W.C. CATHODE GRID
OUTER FIELD CAGE
V.T.P.C. MODULES

Fig. 1

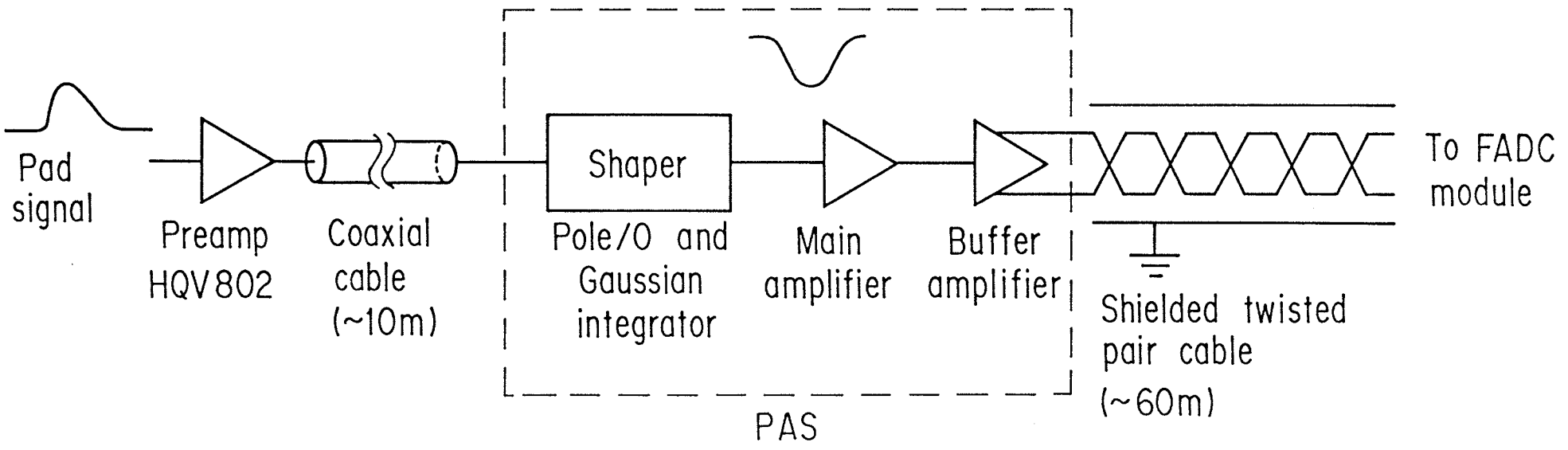

Pad
signal
Preamp
HQV802
Coaxial
cable
(~10m)
Shaper
Pole/0 and
Gaussian
integrator
Main
amplifier
Buffer
amplifier
PAS
Shielded twisted
pair cable
(~60m)
To FADC
module

Fig. 2

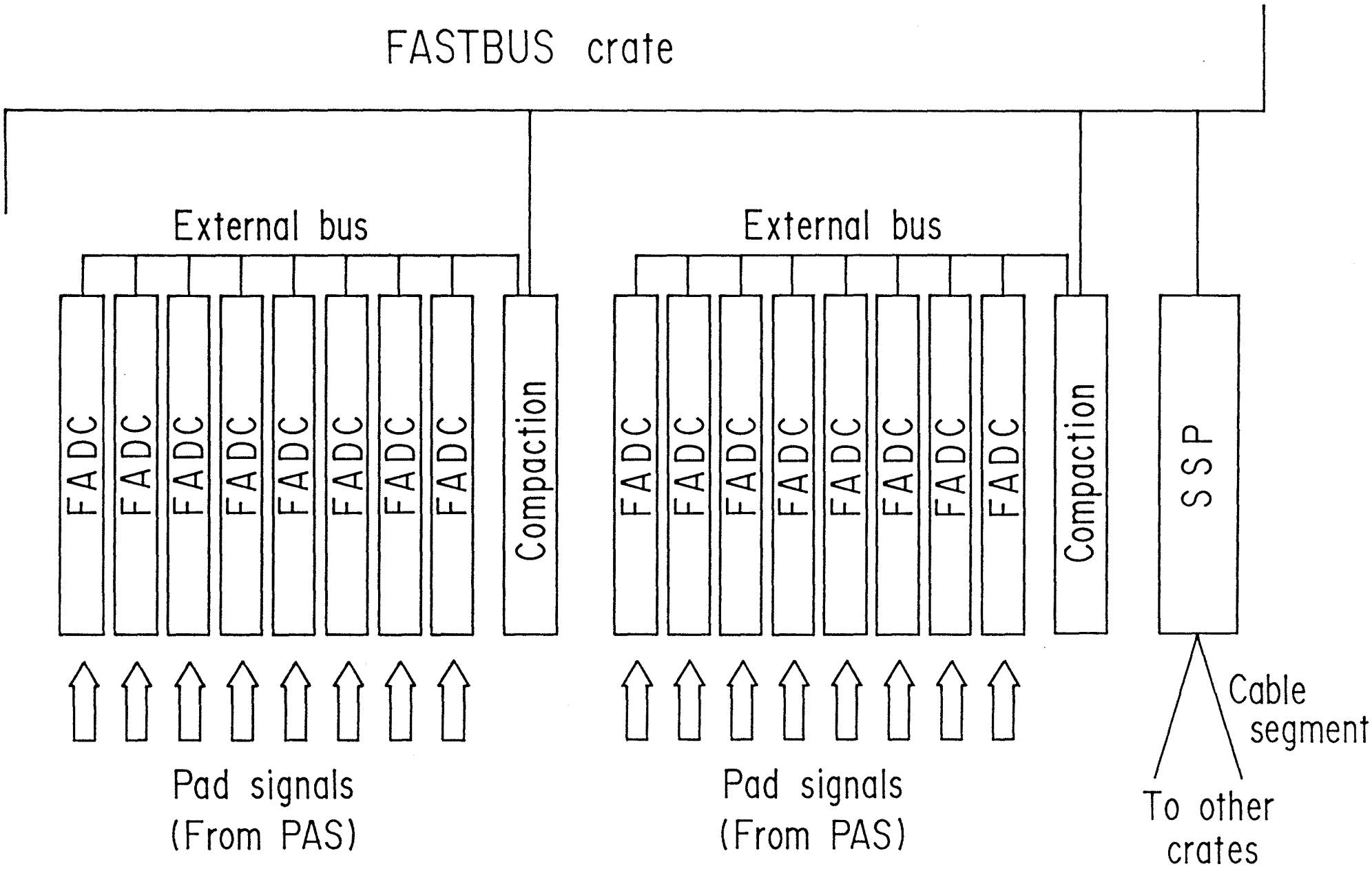

FASTBUS crate
External bus
External bus
FADC
FADC
FADC
FADC
FADC
FADC
FADC
FADC
Compaction
FADC
FADC
FADC
FADC
FADC
FADC
FADC
FADC
Compaction
SSP
Cable segment
To other crates
Pad signals (From PAS)
Pad signals (From PAS)

Fig. 3

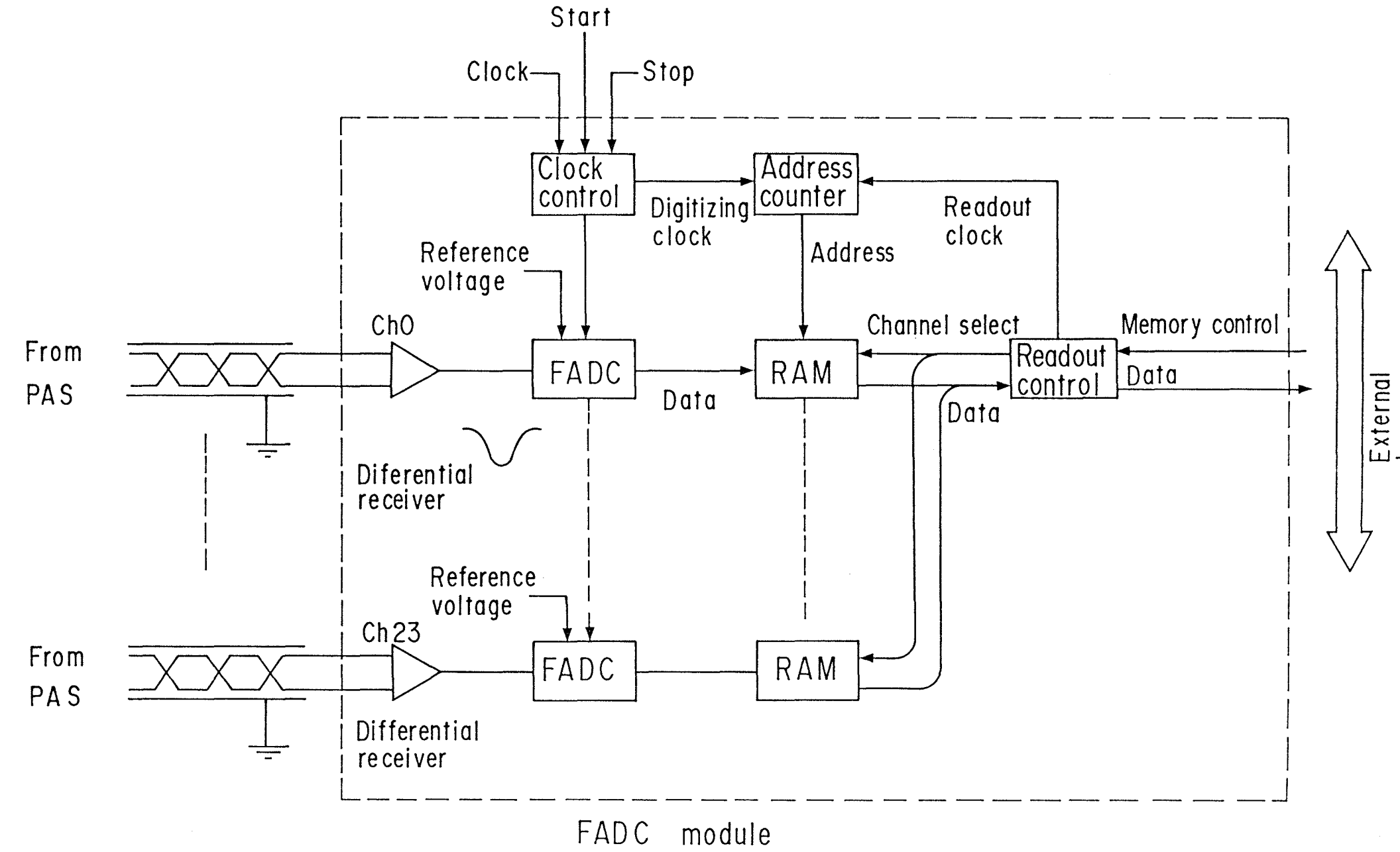

Start
Clock
Stop
Clock control
Address counter
Digitizing clock
Readout clock
Reference voltage
Address
From PAS
Ch0
FADC
Data
RAM
Channel select
Memory control
Readout control
Data
Data
External
Diferential receiver
Reference voltage
Ch23
From PAS
FADC
RAM
Differential receiver
FADC module

Fig. 4

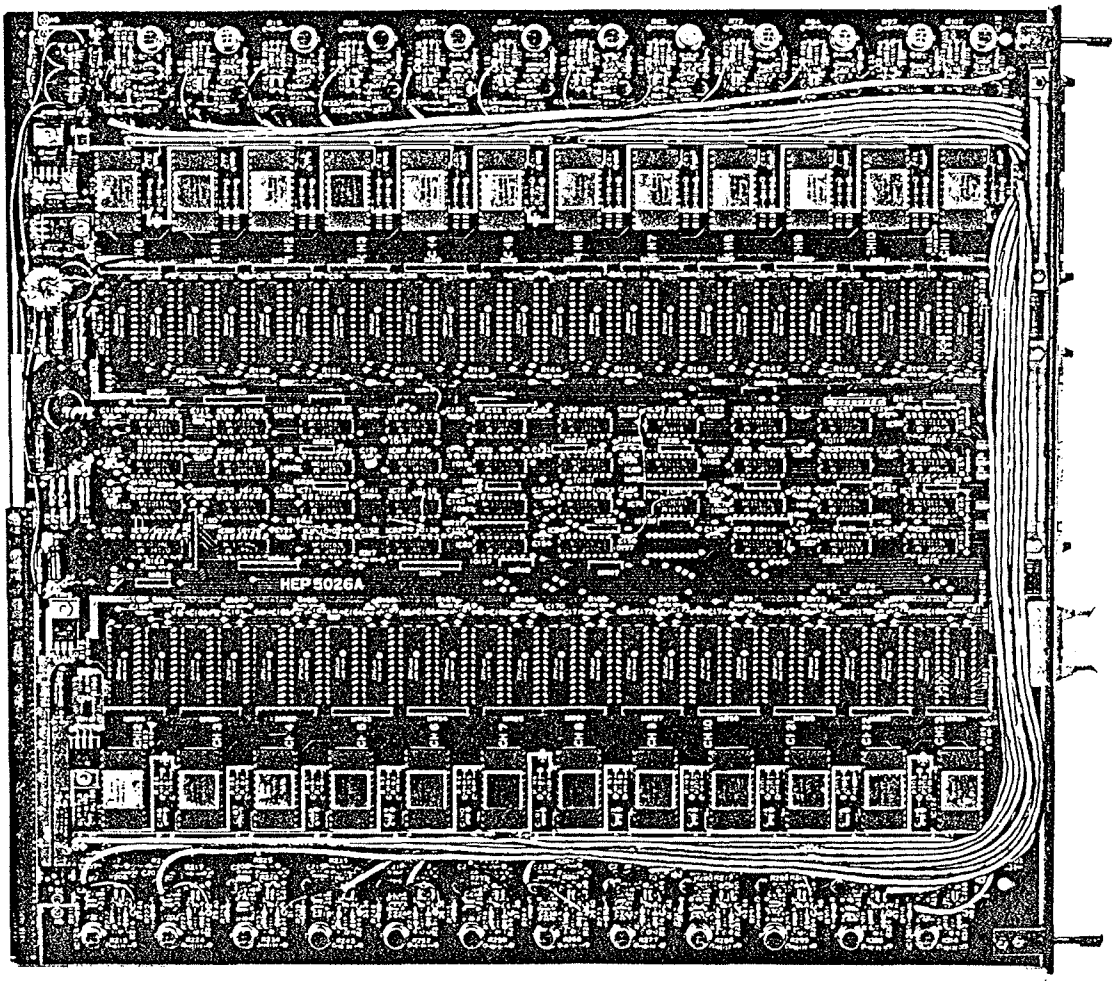
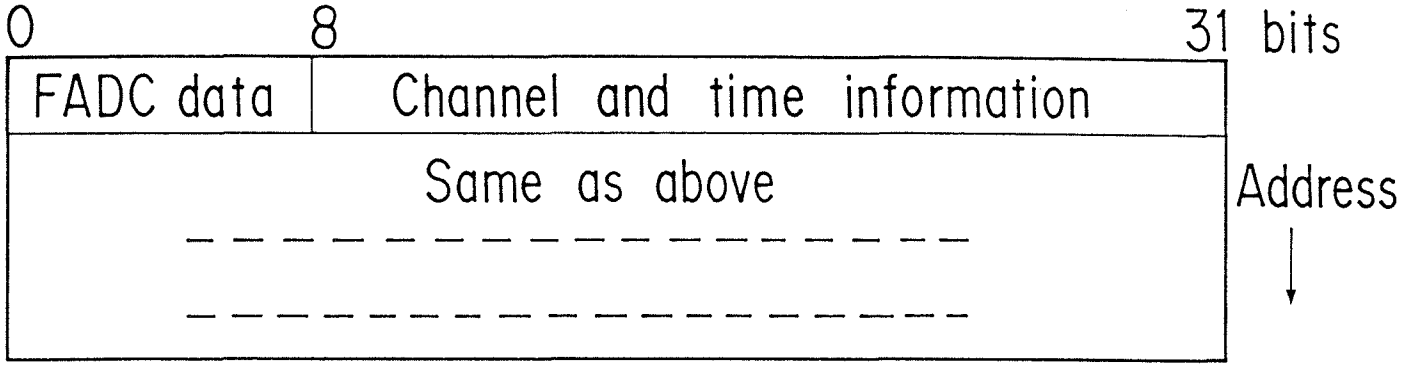
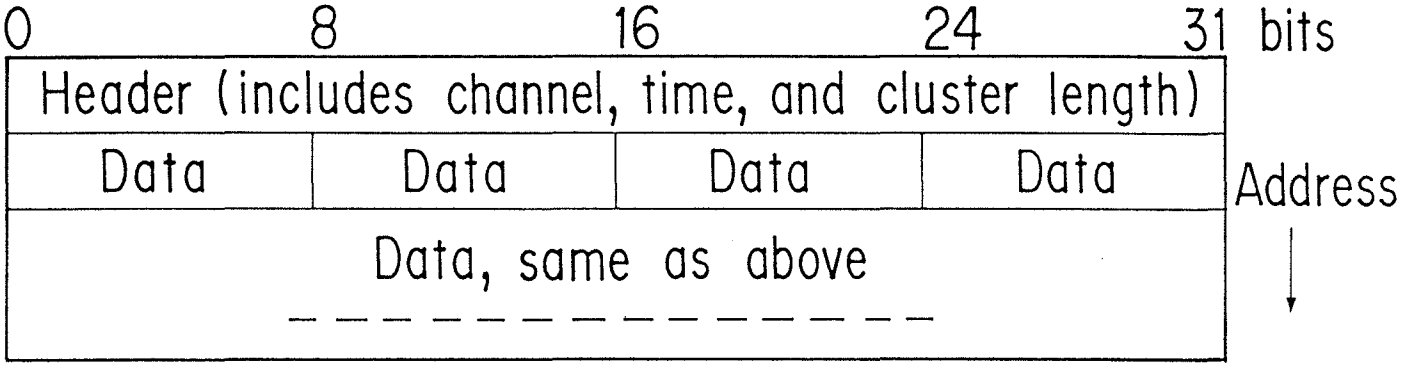


Fig. 5

(a) Zero Suppression



(b) ϕ - cluster finding



(c) t - cluster finding

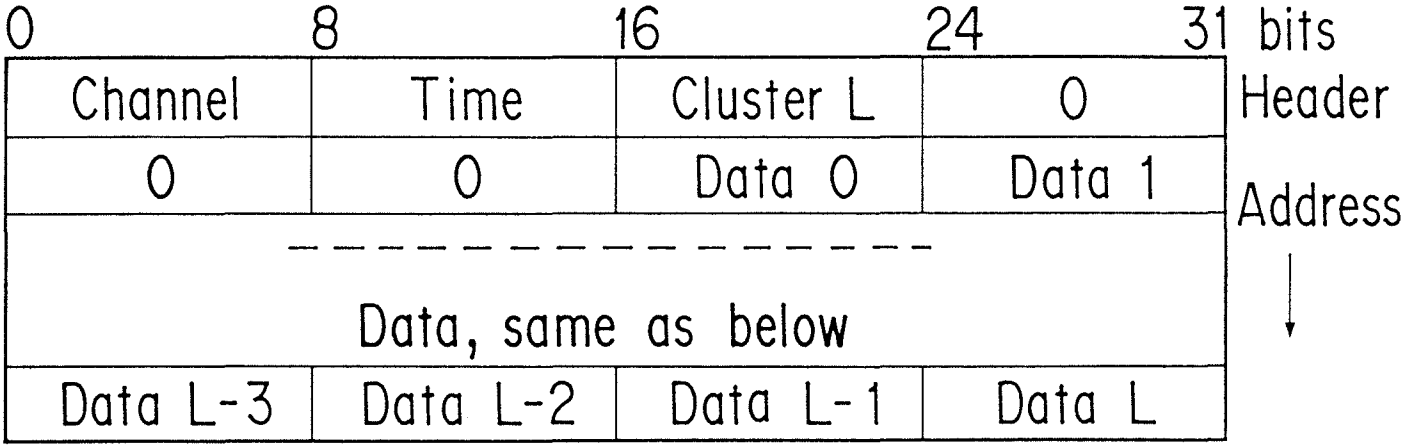


Fig. 6

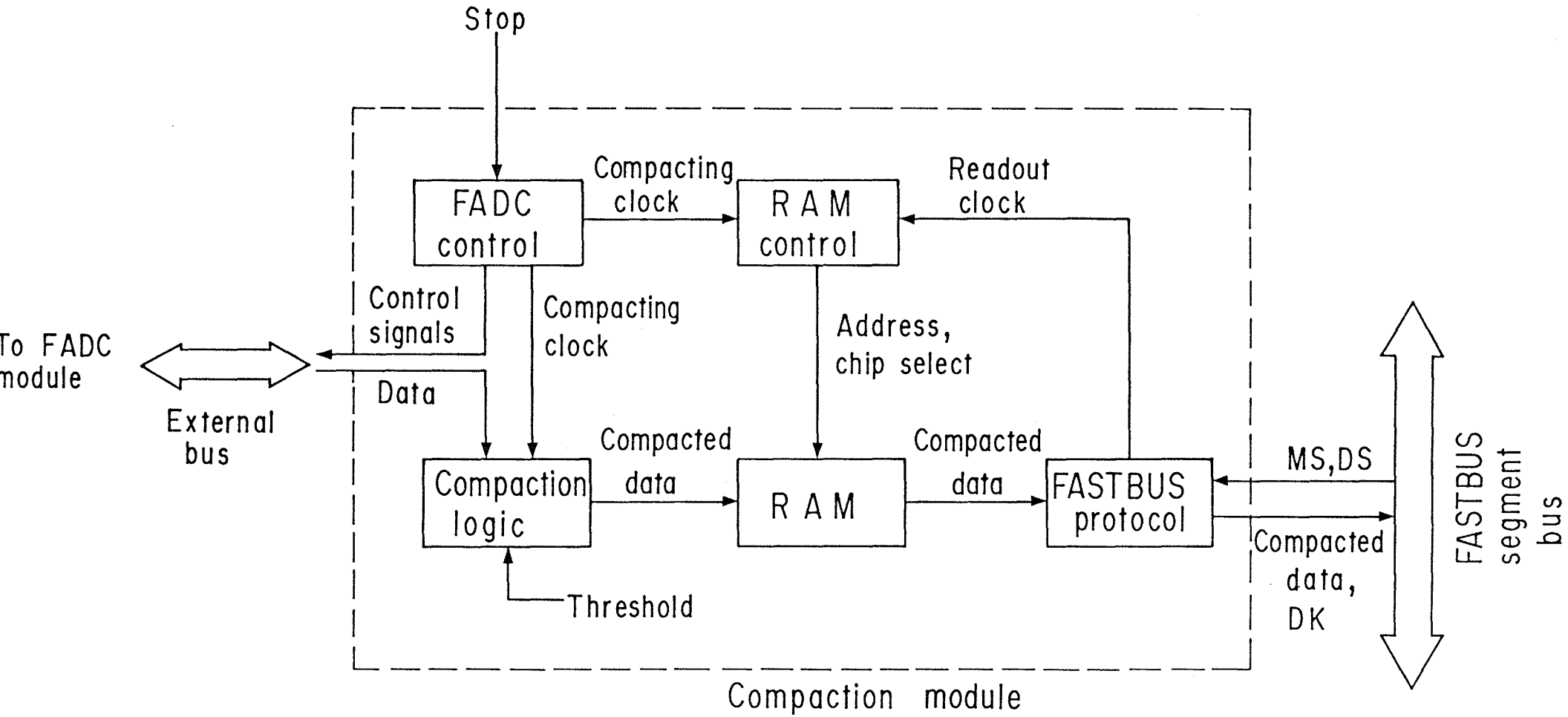

Stop
FADC control
Compacting clock
RAM control
Readout clock
Control signals
Compacting clock
Address, chip select
To FADC module
External bus
Data
Compacted data
Compacted data
Compaction logic
RAM
FASTBUS protocol
MS,DS
Compacted data, DK
FASTBUS segment bus
Threshold
Compaction module

Fig. 7

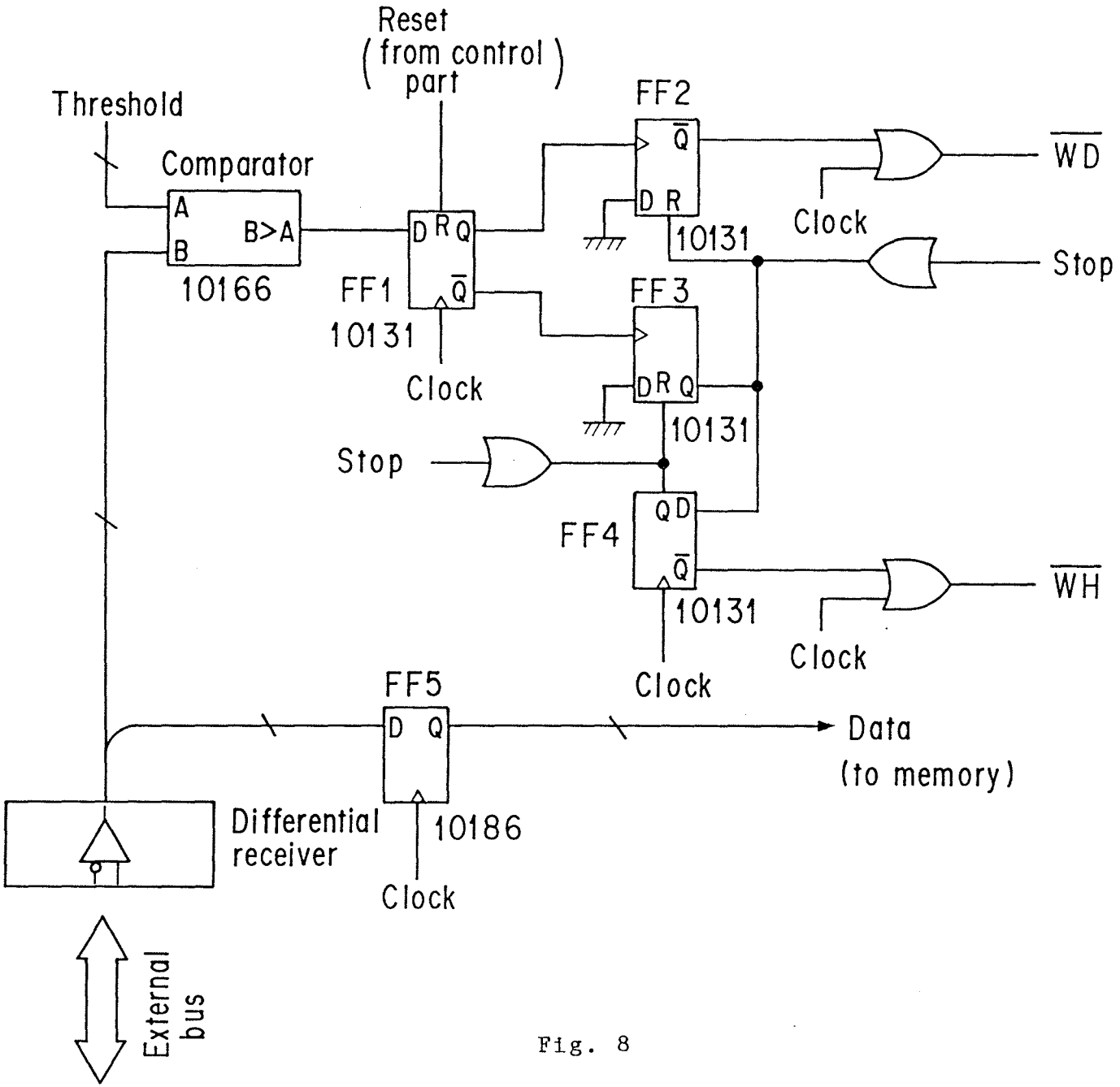

Reset
(from control part)
Threshold
Comparator
A
B
B>A
10166
FF1
D R Q
Q
10131
Clock
FF2
Q
D R
10131
Clock
WD
Stop
FF3
D R Q
10131
Stop
FF4
Q D
Q
10131
Clock
Clock
WH
FF5
D Q
Data
(to memory)
Differential
receiver
10186
Clock
External
bus

Fig. 8

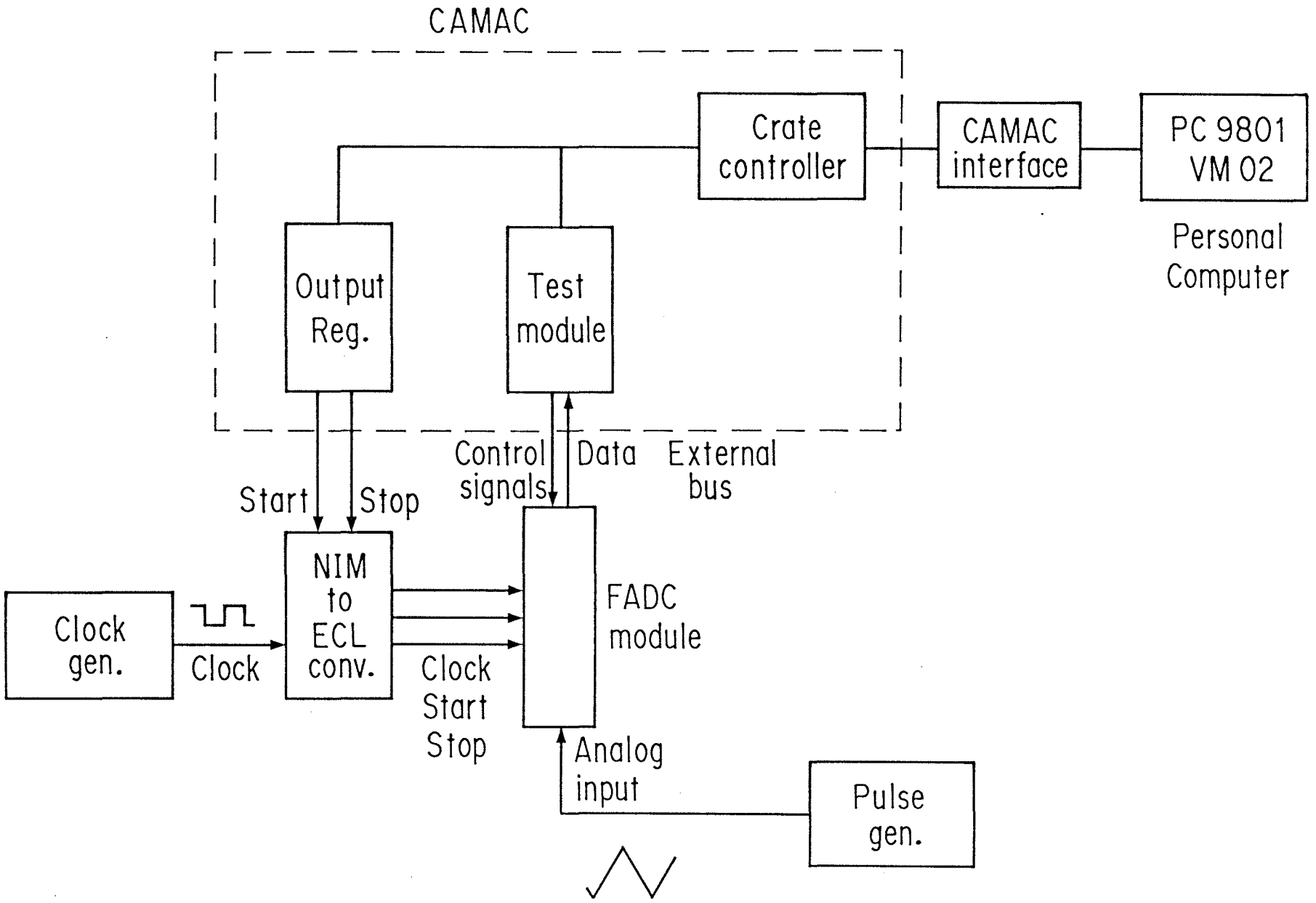

CAMAC
Crate controller
CAMAC interface
PC 9801 VM 02
Personal Computer
Output Reg.
Test module
Control signals
Data
External bus
Start
Stop
NIM to ECL conv.
Clock gen.
Clock
Clock
Start
Stop
FADC module
Analog input
Pulse gen.

Fig. 9

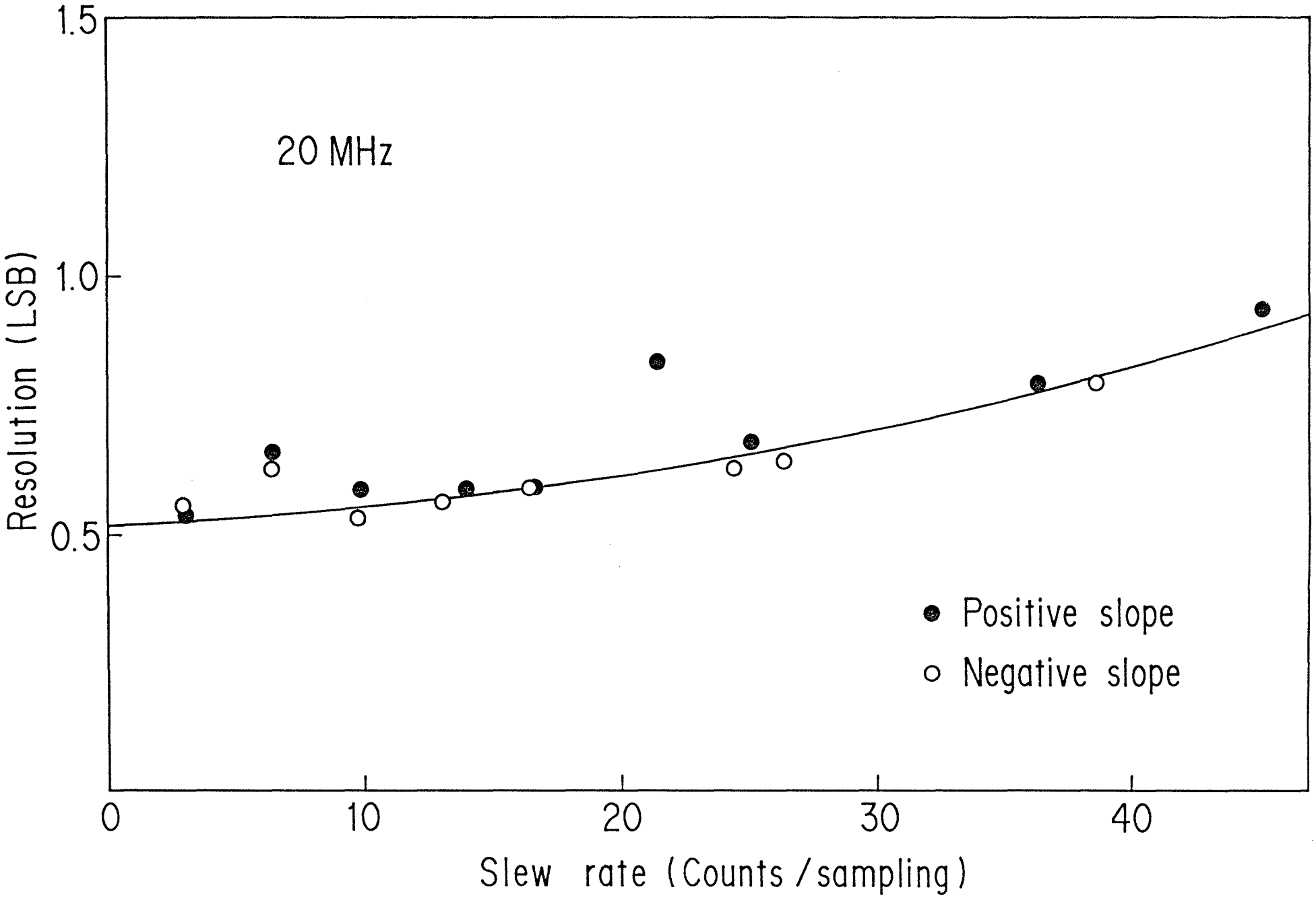

1.5
1.0
0.5
20 MHz
Resolution (LSB)
0
10
20
30
40
Slew rate (Counts / sampling)
Positive slope
Negative slope

Fig. 10