

Development of a high-speed digital signal process system for bunch-by-bunch feedback systems

Makoto Tobiyama* and Eiji Kikutani

Accelerator Laboratory, High Energy Accelerator Research Organization (KEK), 1-1 Oho, Tsukuba, Ibaraki 305-0801, Japan
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High-speed digital filter systems for bunch-by-bunch feedback systems have been developed at KEK. A two-tap finite impulse response filter with simple hardware realizes the functions of a 90° phase shift, suppression of the static component and digital delay of up to a few hundred turns for the KEKB rings. Difficulties in the circuit board, such as the trimming of the timing skews or the problem of long-term reliability, have been solved using custom GaAs large-scale integrated circuits which demultiplex and multiplex fast parallel-digital data coming from the analog-to-digital converter and going to the digital-to-analog converter. Two major applications of the filter board, the bunch current monitor and the bunch oscillation recorder with 20 MB memories for transient-domain analysis of the instabilities, are also described.

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I. INTRODUCTION

In a storage ring which stores many bunches at high beam current, especially in particle-factory machines, such as KEKB, PEP-II, or DAΦNE, it is very likely that many strong coupled-bunch instabilities occur in both the transverse and longitudinal planes. Reduction of the impedances in the ring, of which the strongest ones most likely come from the higher order modes of the accelerating cavities, is essential to suppress the instabilities. In KEKB, we use higher-order-mode-free cavities [1–3] in both low energy ring (LER) and high energy ring (HER), and take special care of the structure of the vacuum components. However, even with these efforts, we have observed strong transverse coupled-bunch instabilities in both rings, the sources of which are presumed to be mainly from the beam-ion effect in the KEKB HER and the photoelectron effect [4] in the KEKB LER. Since there are many bunches with short bunch spacing in the ring and the mechanism of the instabilities is fairly broadband, the frequency spectrum of the instabilities is complicated and spreads over a wide range. How we suppress and analyze the instabilities holds the key to achieving the designed qualities of the accelerators.

To cure these instabilities, we are now operating beam feedback systems with a bunch-by-bunch scheme. In the transverse bunch-by-bunch feedback system, we detect the individual bunch oscillations separately, shift the phase of the signal by 90°, then kick the beam to damp the oscillations. As the signal speed in the feedback circuit and the cables is much slower than that of the beam, feedback signals must wait for rearrival of the bunch at the kicker after about one revolution around the ring. This means that

a signal-processing part of the feedback system must be equipped with a delay mechanism whose length is, at least, the revolution period of the ring. For this delay mechanism we adopted a digital delaying technology. If the size of the ring were not so large, say less than 400 m, we might use analog-type (cable) delays if the loss and deformation of the feedback signal in the delay lines are tolerable. For large rings, such as KEKB, however, analog-type delays are hopeless. Moreover, in the longitudinal plane, we must generate a 90° phase shift amounting to several tens of revolutions in the signal-processing part.

For this purpose, we have developed a digital filter system which realizes the functions of phase shift by any desired value, dc suppression, and an adjustable digital delay without down sampling. Beside this filter, using the same technology, we have also developed a large-scale memory system. In this paper, we describe the filter and

TABLE I. Main parameters of KEKB.

	Ring	
	LER	HER
Energy (E)	3.5 GeV	8.0 GeV
Circumference (C)	3016.26 m	
Design luminosity (\mathcal{L})	$1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$	
Maximum beam current (I)	2.6 A	1.1 A
Bunch current (I_b)	0.5 mA	0.2 mA
Bunch length (σ_z)	4 mm	4 mm
Particles/bunch (N_b)	3.3×10^{10}	1.4×10^{10}
Synchrotron tune (ν_s)	0.01 ~ 0.02	
Betatron tune (ν_x/ν_y)	45.52/45.08	47.52/43.08
rf voltage (V_{rf})	4.5 MV	8.5 MV
rf frequency (f_{rf})	508.887 MHz	
Revolution frequency (f_{rev})	99.39 kHz	
Revolution period (τ_{rev})	10.06 μs	
Minimum bunch spacing (τ_b)	1.97 ns	
Harmonic number (h)	5120	
Longitudinal damping time (τ_s)	22 ms	23 ms
Transverse damping time (τ_x, τ_y)	43/43 ms	46/46 ms

*Email address: makoto.tobiyama@kek.jp
<http://ahfb1.kek.jp/index.html>

memory systems together with the two major applications of the memory system, the bunch current monitor, and the bunch oscillation recorder. Related parameters of the KEKB accelerators are listed in Table I.

II. STRATEGY OF THE DIGITAL FILTER FOR BUNCH-BY-BUNCH FEEDBACK SYSTEMS

The requirements for the digital filter of the longitudinal feedback system is as follows. As the front end detects the longitudinal position of a bunch, the filter should have the function of shifting the phase of the feedback signal by 90° . The static component of the position signal (equilibrium phase), which in some cases is a function of the relative position from the head of a bunch train in the case of high-beam loading, should be eliminated from the feedback signal, because it wastes expensive feedback power. As the period of synchrotron motion is much longer than the revolution period, it is not always necessary to detect the position of a bunch in every revolution. We can digitally *down sample* the signal. On the other hand, for the transverse feedback system, the requirement is simpler; at minimum the filter should have the function of one-turn delay. Unlike the longitudinal case, down sampling the signal is, in general, unacceptable.

There are two approaches to making a digital filter. The first is to use a software-based system using many digital signal processors (DSPs) [5]. Taking advantage of the great progress in digital circuit technology, using DSPs of the fastest execution speed enables us to design a complicated floating-point digital filter with considerable speed. The strong points of a software-based signal process system are as follows:

- (i) Completely programmable. It is easy to change the type of filter by replacing the DSP code.
- (ii) Good filtering characteristics. We can form multi-tap filters easily with good accuracy.
- (iii) Flexibility. It is applicable for both small and large rings by changing the number of DSPs on boards.

However, it also has such weak points as

- (i) Large-scale and complicated design. As the speed of a single DSP is much slower than the given time limit of a calculation, we require many parallel processing cards. For a fixed number of coefficients in the digital filter, the number of DSP cards increases with the number of the bunches times the synchrotron frequency. The difficulty of tuning and maintenance correspondingly increases.
- (ii) It is, in general, necessary to use the down-sampling technique to escape from this complexity. In this case we cannot employ the same system as for the transverse feedback.

The second approach, which we have employed for the KEKB rings, is to make the simplest digital filter which satisfies our minimum requirements with fast hardware logic circuits without the down-sampling technique. The structure of the filter is the hardware two-tap finite impulse

response (FIR) proposed by Pedersen [6]. As shown in Fig. 1, it has only two taps: A(+1) at -90° and B(-1) at -270° of the oscillation.

The frequency response has very wide peaks at $f_s, 3 \times f_s, \dots$, and has zeros at 0 (dc), $2 \times f_s, \dots$, where f_s is the synchrotron frequency in the longitudinal case. Strong points of the hardware two-tap FIR filter are simple and applicable to both longitudinal and transverse feedback systems. The phase shift and time delay are tunable by selection of the tap positions while preserving the time differences between the two taps. For transverse feedback, we can also apply the same two-tap scheme [7]. However, because the optimum tap selection is very sensitive to the betatron tune, this approach is fairly complicated when the optics parameters are not completely known to us. Since adjusting the phase shifts made by vectorially combining signals from locations separated by a betatron phase difference around 90° is easy and not so sensitive to the betatron tunes, the filter should also work as a simple digital delay. Then our filter has two working modes, the two-tap FIR filter mode and the “pass-through” mode. This pass-through mode can be easily realized by simply halting the arithmetic logic unit.

With this simplification, the function of the filter is fairly limited and the following weak points arise:

- (i) Very limited flexibility. To reduce the complexity, the structure of the filter needs to be strongly geared towards a particular ring. Application to other rings is, in general, very difficult.
- (ii) No sharp filtering effect around the center frequency. This is, in practice, not a serious problem. Experiments with beams show that the measured S/N of the detection signal is good enough, typically better than 40 dB.

The greatest difficulty with the filter lies in the complication of the high-frequency digital circuits. It is necessary to access memories three times (one *write* and two *reads*) within one data period, in our case 2 ns. This access speed is completely unattainable without

$$\text{Kick} = \alpha(A - B)$$

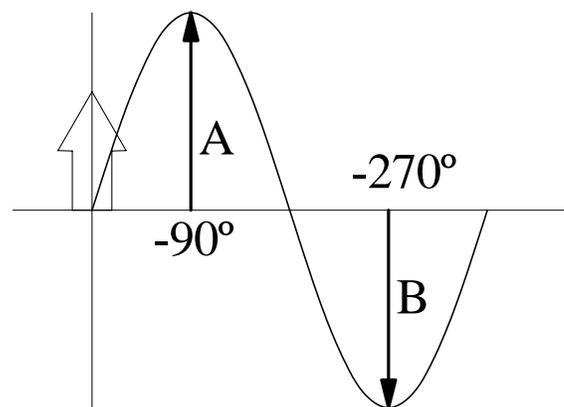


FIG. 1. Tap positions for the two-tap FIR filter.

TABLE II. Main specifications for FDMUX and FMUX.

	FDMUX	FMUX
Technology	0.5 μ gated GaAs direct coupled FET logic	
Function	1:16 \times 4 bits	16:1 \times 4 bits
Integration	1.5 k gates	1.7 k gates
Maximum operation frequency	600 MHz	600 MHz
Supply voltage	3.3 and 2.0 V	
Consumption current (2 V)	570 mA	814 mA
Consumption current (3.3 V)	400 mA	12 mA
Power dissipation	2.5 W	1.7 W
I/O (fast)	Pseudo-ECL (1 and 0 V with load of 50 Ω)	
I/O (slow)	LvTTL (3 and 0 V)	
Packaging	136 pins ceramic quad flat package	

demultiplexing the digital data into many parallel lines. The demultiplexer by separated logics commercially available would be a fairly complicated circuit needing great care in the design and tuning of the time skews of many lines. In addition, we must prepare chips with the same characteristics. The design of the final multiplexing process would also be a severe problem.

These difficulties have been overcome by developing custom large-scale integrated circuits (LSIs) to multiplex and demultiplex fast digital data. Small chips contain a high-speed circuit which would occupy a large area on the circuit board. These maintenance-free chips enable us to use dense complementary metal-oxide semiconductor (CMOS) memories and ensure high reliability of the board.

III. CUSTOM LSIS

The circuit design and fabrication of the custom LSIs for the fast data demultiplexer (FDMUX) and the fast data multiplexer (FMUX) were carried out by Oki Electric Industry Co. Ltd. Table II gives the main specifications of the LSIs.

The bottom views of the FDMUX (GHDK4211) and FMUX (GHDK4212) are shown in Fig. 2.

A. Fast data demultiplexer

The FDMUX demultiplexes four bits of pseudo-emitter-coupled logic (PECL) signal into 16 channels \times 4 bits of low-voltage transistor-transistor logic (LvTTL)

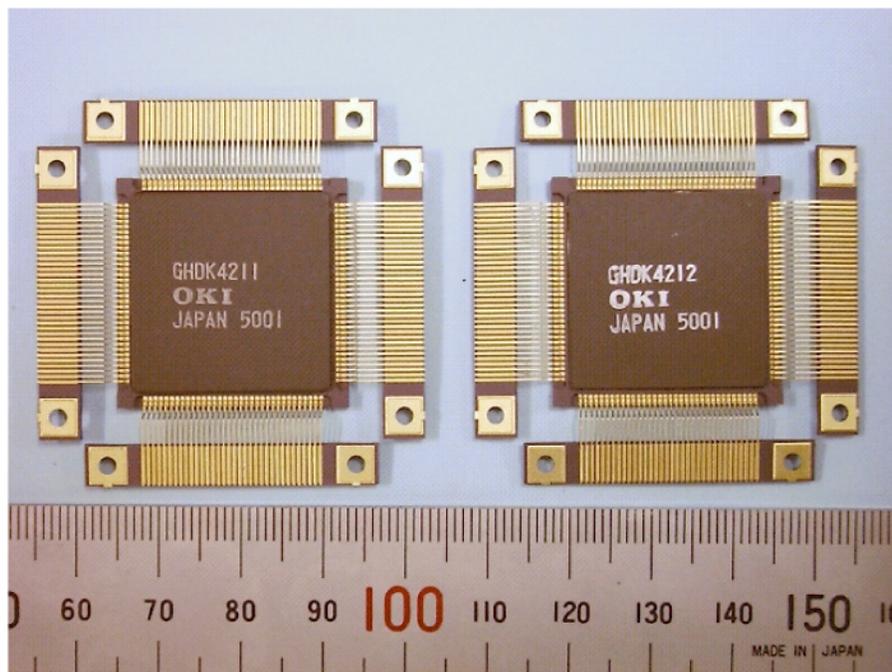


FIG. 2. (Color) Bottom views of FDMUX (GHDK4211) and FMUX (GHDK4212).

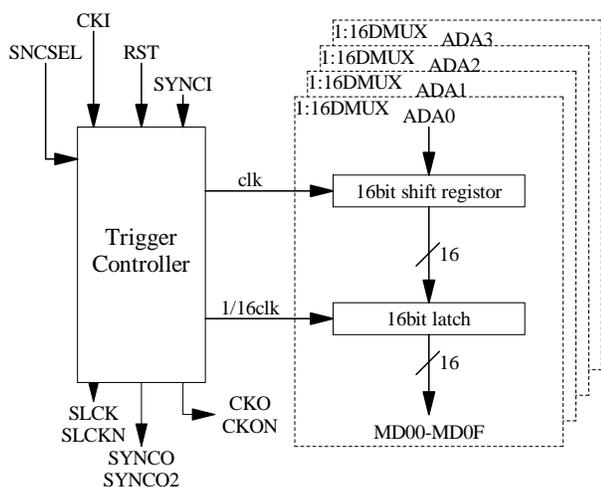


FIG. 3. Block diagram of the FDMUX LSI. CKI: clock input (PECL); RST: reset input (LvTTL); SYNCI: synchronization timing input (PECL); SNCSSEL: synchronization timing selection (LvTTL); SLCK and SLCKN: synchronization timing output (LvTTL); SYNCO and SYNCON: synchronization timing output (PECL); CKO and CKON: clock output (PECL); ADA0–ADA3: fast data input (PECL); MD00–MD3F: demultiplexed data output (LvTTL).

signal at up to 600 MHz. As shown in Fig. 3, this LSI consists of four 1:16 DMUX blocks and one trigger controller. In one 1:16 DMUX block there is one 16-bit shift register and one 16-bit latch. Fast-serial data of up to 600 MBPS are input to the 16-bit shift register and aligned to the same clock, then latched by the 16-bit latch working with a 1/16 clock. The output of the latch makes a 1:16 demultiplexed signal.

The trigger controller consists mainly of an 8-bit ring counter and several decoders. It supplies trigger signals to the 1:16 DMUX blocks, the synchronization timing signals (SYNCO and SYNCON) which are used to synchronize between multiple FDMUXs and FMUXs, and the slow timing signals used in the LvTTL circuit (SLCK and SLCKN). By combining the two FDMUXs (four bits), we can easily create a 1:16 demultiplexer for eight bits, because of limitations of available package pins, we could not prepare many timing signals that would have been useful for the memory circuits.

B. Fast data multiplexer

The FMUX multiplexes 16 channels \times 4 bits of LvTTL signals to a 4-bit PECL signal. Figure 4 shows a block diagram of the FMUX LSI. As shown in the figure, it consists of four 16:1 MUX blocks and a trigger controller. The trigger-controller block has the same function as that in FDMUX.

A slow parallel signal is at first held by a 16-bit latch in the 1:16 DMUX block. Between the 2:1 selector and the 16-bit register, the latched data advance bit by bit,

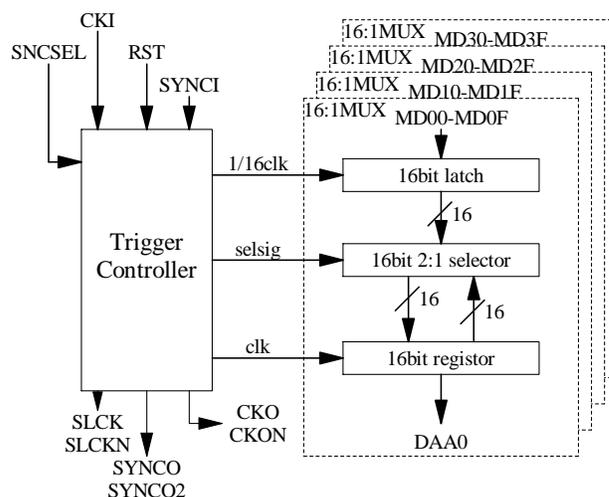


FIG. 4. Block diagram of the FMUX LSI. MD00–MD3F: slow data input (LvTTL); DAA0–ADD3: multiplexed data output (PECL).

synchronized to the clock signal. This procedure performs the function of a 16-bit shift register, and the output of the register becomes the multiplexed data. As with the FDMUX, we can generate a 16:1 multiplexer with 8 bits combining two FMUXs.

IV. THE FILTER BOARD

Figures 5 and 6 show a block diagram and a photograph of the filter board.

The size of the motherboard is 366.7 mm \times 460 mm. On the board there are FDMUXs, FMUXs, a digital-to-analog converter (DAC), field programmable gate array (FPGA) chips for address, and versa module Europe (VME) control. There are 16 slots of connectors on the board for the memory/arithmetic logic unit daughterboards, and four slots of connectors for the data shift logic daughterboards. An analog-to-digital converter (ADC) daughtercard and a precise-timing-generator daughtercard are also mounted on the board.

The filter system can use a large-scale memory board by replacing the memory/subtractor daughtercard with a dense memory card and by replacing the address-control FPGA of the filter addressing with that of the memory addressing. In this case, each memory daughtercard has 1.3 Mbytes of memory, and the total memory capacity amounts to 20 Mbytes, which corresponds to recording 4096 turns of 5120 bunches. In KEKB, this memory size corresponds to 41 ms, comparable to the transverse radiation damping time. In this application, we can omit the precise timing controller for the memory-write and memory-read control because the timing is not severe at all. Also, the downstream section of the filter, such as the FMUXs and the DAC, is omitted.

The practical design and fabrication of the boards are performed at the Digitex Laboratory Co., Ltd.

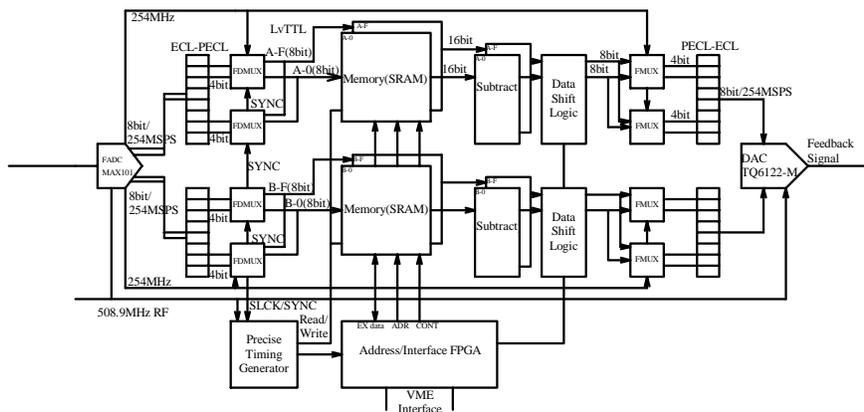


FIG. 5. Block diagram of the filter board.

A. ADC and DAC

When we started designing the system, we had few candidates for an ADC which works at a clock rate of 509 MHz and has a sufficient analog bandwidth, typically around 1 GHz. We adopted a MAX101 from MAXIM, which works at 500 MSPS with 8-bit resolution and has 1.1 GHz of analog bandwidth. It has a 1:2 demultiplexer within the chip, so there are two channels of emitter-coupled logic level outputs. To more easily handle possible problems with ADC, we have separated the ADC from the motherboard.

Since the output of the MAX101 is already 1:2 demultiplexed, we have used four chips of FDMUXs and FMUXs on the board. The ADC outputs are therefore demultiplexed into 32 channels. The system clock (255 MHz) for the upper 16 channels (channel A) and the lower 16 channels (channel B) are supplied from the ADC. Each set of 16 channels works simultaneously.

For the DAC we have chosen the TQ6122-M from TriQuint which works at up to 1 GHz with 8-bit resolution and has a 2:1 multiplexer in the chip. The DAC is directly mounted on the motherboard.

B. Memory/arithmetic logic units

The actual filtering function is performed by the memory/arithmetic logic unit, two of which are mounted on one daughtercard. Each channel handles 160 (= 5120/32) bunches in the case of the KEKB rings. We use two sets of ring memories (M-1 and M-2) per channel to reduce the memory accesses from three (one write and two reads) to two (one write to M-1 and M-2, one read from M-1 and one read from M-2). Data from FDMUXs are written into both memories in the same address simultaneously. At the next step, we read the -90° data from memory M-1 and the -270° data from memory M-2 at the same timing with different memory addresses. Since the time period of the data output from the FDMUXs is 64 ns, the use of CMOS static random access memory with an access speed of 12 ns is enough for the two accesses. Practically, as is commonly said, we need roughly a treble margin for fast memories; otherwise, very fine tuning of all the signals would be necessary. We therefore have prepared a separate timing circuit (a precise timing generator daughtercard) to change the timings and widths of the write enable (\overline{WE}) and output enable (\overline{OE}). The tuning step of the board is 16 ps.

As it is necessary to store data for at least 100 turns per bunch, that is $5120 \times 100 \times 2$ bytes, we mounted 2 Mbytes of memory in total. To debug the system, all the memory can be accessed (read and write) through the VME bus.

For each memory/arithmetic logic unit daughtercard, we use two FPGAs (ALTERA EPM7064LC68-15) with the function of a subtractor, that is full-adder logic. About 82% of the 2500 available gates are used. It also contains a bit-shift mechanism which shifts the output of the subtractor from 0 to 3 bit upward. It enables us to change the gain of the filter up to 20 dB dynamically.

In the pass-through mode, we do not change any timing on the memory board but only change the function of the FPGA from [(contents of M1)–(contents of M2)] to [M1–0]. It is also possible to change the gain with the bit shifter.



FIG. 6. (Color) Photograph of the filter board.

C. Address and synchronization controllers

In order to realize the function of the digital filter, we must manipulate three address pointers for accessing the ring memory under a 15-bit address space. One is the write address that runs $508.9 \text{ MHz}/32 = 16 \text{ MHz}$. The other two addresses are used to point at the -90° and -270° previous data for the bunch feedback. We have used the very fast and dense ALTERA EPM7128ELC84-7 FPGA for the controller. About 99% of the 5000 available gates are used. In the FPGA, these two addresses are calculated from the main address and the shift values supplied through I/O (VME). The shift value must be a multiple of 160 in our case to synchronize the data with the ring. For the large-scale memory board and the bunch current monitor, we use the ALTERA EPM7218LC84-10, at 44% of capacity.

By changing the first tap position while keeping the interval of two-tap positions constant, we can adjust the one-turn delay of the feedback system with 64 ns steps. In addition to this rough delay, we have prepared data shift logic that changes the order of the data from the memory daughtercards. It has 8 FPGAs (ALTERA EPM7064LC44-12) that latch and switch the data. About 82% of the 2500 available gates are used. The delay step here is 8 ns and is controlled through the VME bus.

Synchronization between the ring and the filter board is not necessary in our case, because the harmonic number of 5120 is a multiple of 160, so synchronization is realized automatically in free running. For the case of the large-scale memory board, in order to fix the relationship between the bucket ID number and the memory address, synchronization between the ring revolution and address 0 of the memory is necessary. The system accepts the nuclear instrument module level synchronization signal, which resets the addressing of the memory and generates the SYNCI signal to the master of the FDMUX. As the ADC has a demultiplexer whose timing we do not control, we can change the relation between bucket 0 and memory address 0 in 2-bucket steps. The residual difference of 2 ns is adjusted by trial and error by switching on and off the clock to the memory board.

D. VME interface

For external I/O, we have mounted a VME interface on the board. The required address space is A24 (AM code of 3D) or A32 (0D) with a data size of D16 or D32. The interface also has an interrupt function with the release on acknowledge mode that is used to send the stop request to the VME bus. The decoding and encoding of the VME command is performed with an FPGA (ALTERA EPM7096LC84-15). About 46% of the 3600 available gates are used.

As it is impossible to connect the filter/memory system directly to the VME bus, we are using a bus expander

which connects between the VME subrack and the filter system. It consists of buffer transistor-transistor logic integrated circuits and bus selectors so as not to interfere with other cards on the bus.

V. APPLICATION TO THE KEKB BUNCH-BY-BUNCH FEEDBACK SYSTEMS

A. Transverse bunch feedback systems

We have prepared transverse feedback systems for both the KEKB HER and the KEKB LER for both horizontal and vertical planes and a longitudinal feedback system for the KEKB LER. As we need one filter system for each transverse plane for each ring, four filter systems are necessary for transverse feedback in total. In addition, one is necessary for LER longitudinal feedback. The filter functions are controlled through the EPICS R.313 system. The VME-CPU (IOC: I/O controller) which we have used is a Force Power PC 6750s with 64 MB of memory.

An example of the frequency response of the filter is shown in Fig. 7, where the input power is -5 dBm and the tap positions are (1, 401), which correspond to a passing frequency of 19.9 kHz.

Commissioning of the KEKB rings started at the end of 1998 [8]. We have successfully stored over 500 mA in each ring and have begun physics running. During the commissioning, we encountered strong coupled-bunch instabilities in the transverse planes in both rings. They limited the total storable currents, shortened the beam lifetimes, and reduced the beam qualities. With the progress of the operation of the transverse bunch-by-bunch systems, we have successfully suppressed the instabilities. At present we are operating the filters for the transverse feedback system, not as a two-tap FIR filter, but as a simple digital delay (the pass-through mode). The size of the digital delay was about $9.29 \mu\text{s}$ for the KEKB LER and $9.03 \mu\text{s}$ for the KEKB HER. The

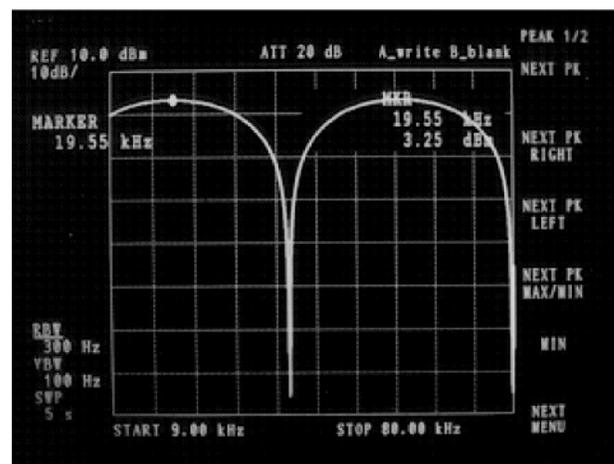


FIG. 7. Frequency response of the two-tap filter with the tap position of (1, 401).

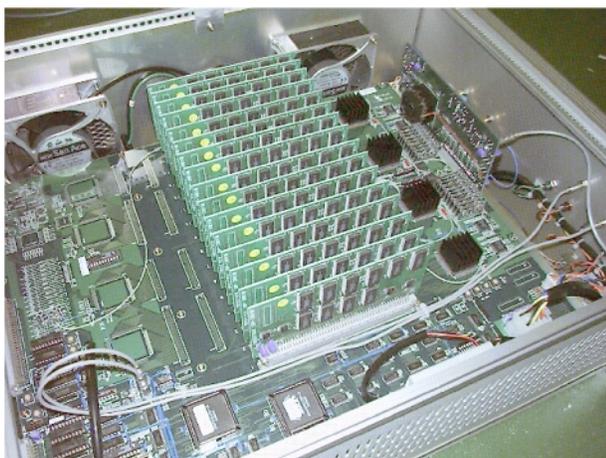


FIG. 8. (Color) Photograph of the bunch current monitor/large-scale memory board.

typical damping time of the transverse feedback system was about 0.5 ms for both KEKB HER and KEKB LER. Up to this point, we have been able to completely suppress all transverse instabilities with a gain greater than 40 dB for all planes in both rings.

B. Bunch-current monitor

In KEKB, the equalization of the bunch current is very important not only to suppress the instabilities, but also to maintain high luminosity with long beam lifetimes. To control the bunch current during the injection process, it

is necessary to measure the bunch currents of all 5120 buckets and decide which bucket should be injected by the next pulse within the injection interval, which is 20 ms at the maximum injection rate. As one special application of the filter board as a memory board, we have prepared two bunch-current monitors for KEKB. The structure of the bunch-current monitor is the same as that of the large-scale memory board, but the address space is limited to 1 Mbyte. Figure 8 shows a photograph of the bunch current/large-scale memory board.

During injection, the bunch-current monitor transfers the bunch-current data triggered by the interrupt from the injection kicker timing signal. Under the VxWorks operating system with EPICS R313 and the IOC of Power PC 6750, the interrupt response time was typically 21 μ s, and the data transfer of 5120 bunches data required about 1.4 ms, at about 1.2 μ s per four bunches data transferred in D32 mode. An example of the filling pattern of the KEKB LER during a physics run is shown in Fig. 9, where the total current was 265 mA.

C. Transient-domain analysis of instabilities

The transient behavior of the beam just after closing/opening of the feedback loop reveals many important characteristics of the coupled-bunch motions as well as the performance of the feedback systems. This powerful method of analyzing instabilities is known as transient-domain analysis [5,9]. Six large-scale memory boards for all planes of both rings with a capacity of 20 MB have

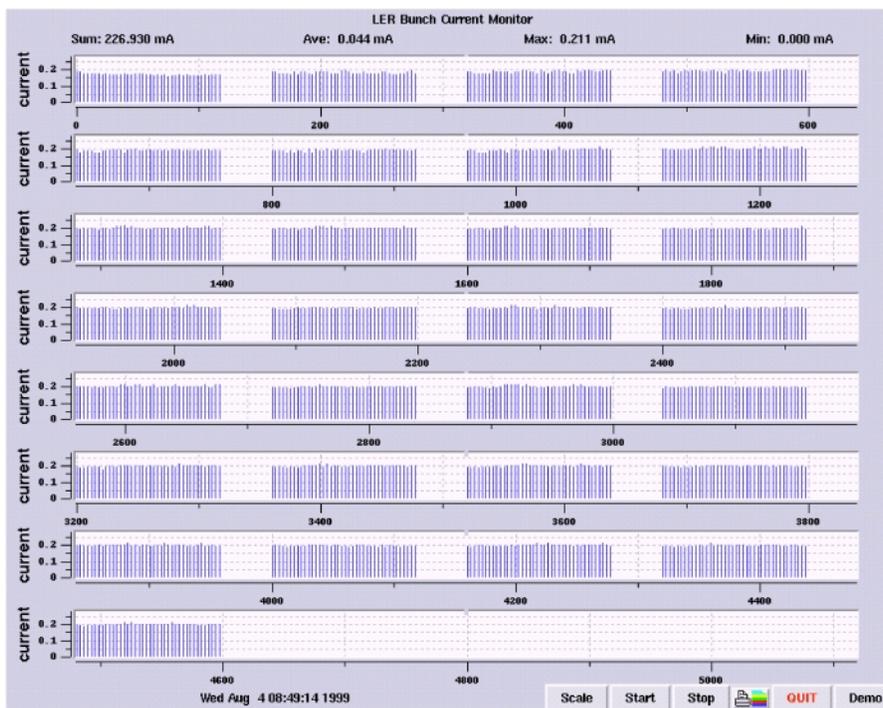


FIG. 9. (Color) Example of the filling pattern during a physics run. The bunch spacing was 6 ns.

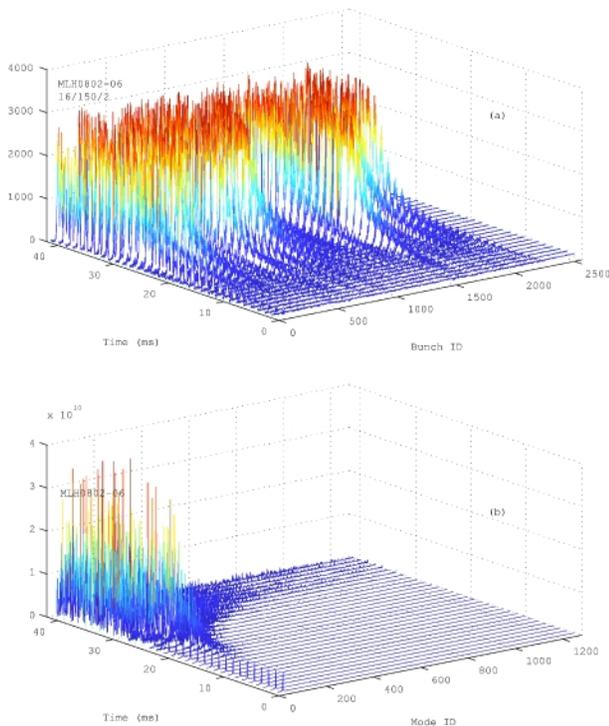


FIG. 10. (Color) Example of a growing transient due to horizontal instability in the KEKB LER: (a) time evolution of the betatron amplitude for each bunch, (b) time evolution of the modes of the instability.

been prepared for analysis as bunch oscillation recorders. To transfer the data from the memory board to the memory on the IOC, it takes about 16 sec in the D16 access mode. In practical use, the data transfer of 20 MB from an IOC to a network file system mounted disk on a host workstation takes about one to a few minutes, depending on the traffic on the network system.

Figure 10 shows an example of the growth of horizontal instability in the KEKB LER from just after turning off the horizontal feedback up to 41 ms later. The total current was 120 mA with a filling pattern of 16 bunch trains equally spaced in the ring, each train containing 150 bunches with a bunch spacing of 4 ns. Figure 10(a) shows the time evolution of the betatron-oscillation components for each bunch. By taking the Fourier transform of bunch amplitude at each time, taking into account the betatron phase advances, we calculate the evolution of the modes of the instability over time, as shown in Fig. 10(b). The net growth time of the instability was about 5 ms in this case. We have acquired many transient-domain data with changing filling pattern and betatron tunes for both rings in both planes. Figure 11 shows the vertical feedback switch-on transient in the KEKB HER.

The large-scale memory board was also used to observe the instabilities at Beijing Electron Positron Collider in the electron-filling mode and the positron-filling mode [10].

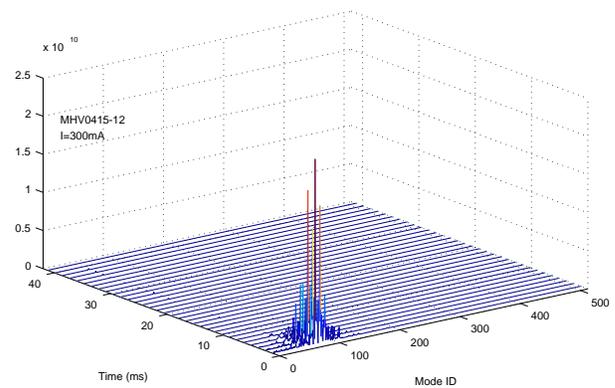


FIG. 11. (Color) Example of a damped transient due to a vertical instability in the KEKB HER.

VI. CONCLUSION

We have developed high-speed digital filter systems for the bunch-by-bunch feedback systems. The difficulties of high-speed electronics were overcome by developing custom LSIs that demultiplex and multiplex the parallel data. Based on the same technology, we have also developed a bunch current monitor and a large-scale memory board. All of the systems are working very well at KEKB and are contributing to improvements in ring operation and physics runs.

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