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Woodpile Structure Fabrication for Photonic Crystal Laser Acceleration

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Abstract. We describe initial steps at fabricating a dielectric photonic bandgap accelerator structure designed to operate at near IR frequencies. Such a structure operating at these frequencies requires extremely small, sub-micron sized features, forcing one to use lithographic means for fabrication. A process based upon lithographic equipment at the Stanford Nanofabrication Facility has been developed and a four layer test structure has been fabricated. Unexpected problems with the final etch step, and corresponding modifications to the process flow addressing these problems, are described. Spectroscopic measurements of the structure have been taken and are compared to simulations.

Keywords: woodpile, photonic crystal, PBG, laser acceleration, nanofabrication
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INTRODUCTION

Laser driven dielectric accelerator structures have recently become of interest due to the potential GeV/m accelerating gradients [1, 2], widespread availability of high power lasers, low costs associated with large scale fabrication of such structures, and interesting beam parameters resulting from such accelerating schemes [2, 3, 4]. High loss in metals at optical frequencies prompt exploration of alternate means to confine and manipulate the EM fields used for acceleration. Photonic crystals offer an attractive way to confine laser radiation over a range of frequencies to within a defect region, allowing the manipulation of the EM fields without the use of metallic boundaries. One structure in particular that has been explored in some detail, but only theoretically for particle accelerator applications, is the woodpile structure, shown in Figure 1. This structure is attractive because it has a fully 3 dimensional bandgap, is amenable to common lithographic procedures, and allows much flexibility in structure refinement and modification.

The critical parameters for the design of a woodpile accelerator structure have been explored through simulations by Cowan [2]. These simulations provide the framework needed for the initial steps of fabrication. Target structure parameters such as the rod thickness, w, lattice constant or rod spacing, a, and layer thickness, h, were determined by optimizing the bandgap using these simulations. A process based on nanofabrication technology used in the semiconductor industry has been developed using equipment at the Stanford Nanofabrication Facility (SNF). This process has been used to build a four layer test structure, exploring the details and ramifications of the methods used

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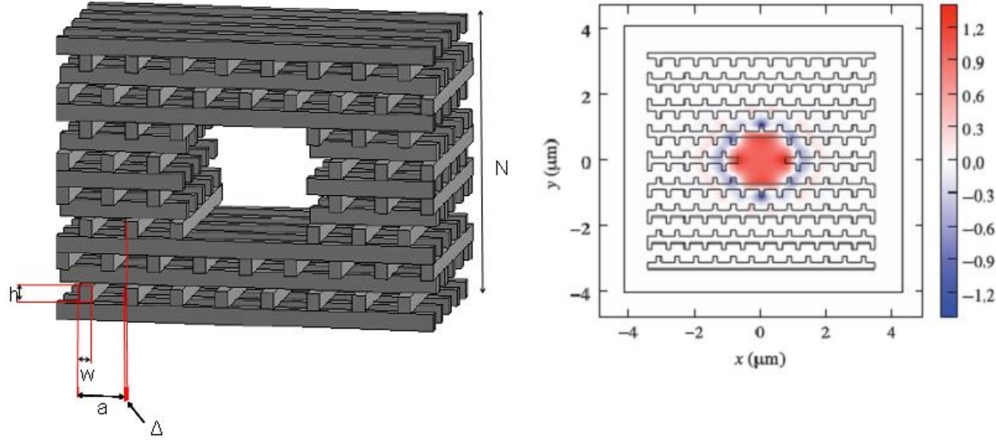

FIGURE 1. Left: The woodpile structure with a defect and critical lattice parameters denoted. Right: Axial electric field profile derived from FDTD simulations.

for each step in the fabrication. This paper will discuss the design parameters of a woodpile accelerator structure, the details of the current fabrication process, the results of the second attempt at fabricating a four layer test structure, and some spectroscopy measurements taken on the resulting four layer test structure.

CRITICAL STRUCTURE PARAMETERS

The woodpile structure, shown in Figure 1, is a photonic crystal with a periodically varying index of refraction in a face centered cubic lattice orientation. This index variation is achieved by stacking rows of rods of two different materials, silicon and vacuum in this case, on top of another in an orthogonal fashion, with every other layer offset by half a lattice constant. The parameters of the entire structure are scalable, determining the center bandgap wavelength. By scaling the structure down in size this center wavelength can be scaled down to near IR wavelengths, where high power lasers are commercially available. The corresponding feature sizes for such a structure are at the limit of current optical lithography tools, however. SNF currently operates an ASML PAS 5500, a lithography tool capable of resolving minimum features of 450nm, setting the lower limit for the scale of a structure fabricated at this facility. A minimum feature size of 500nm was chosen for the purposes of the test structure, thus determining the rod width, lattice constant, and layer thickness to be 500nm, 1.814μm, and 632nm respectively. This structure has a corresponding center bandgap wavelength of 4.9μm.

FABRICATION PROCESS

Fabrication of photonic crystals at optical frequencies is an entire field itself, based heavily on nanofabrication procedures and equipment used in the semiconductor industry [6].

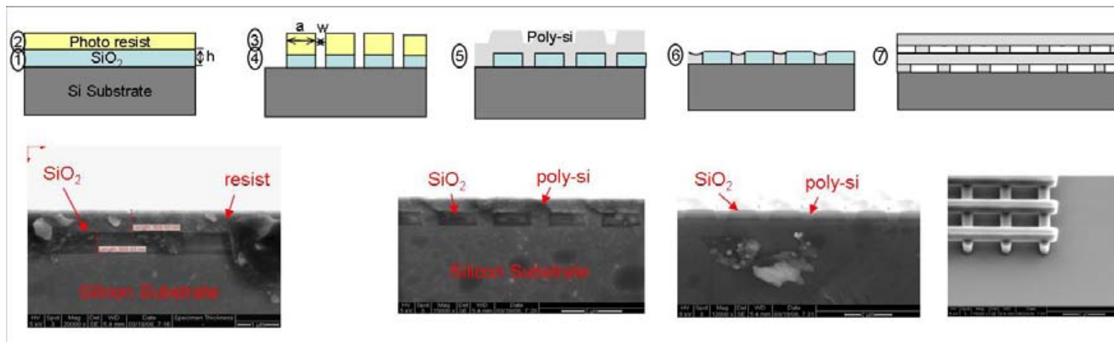

FIGURE 2. This is a visual outline of the fabrication process. The details of each step are described in the Fabrication Section. SEM images are included to supplement the outline and demonstrate the feasibility of the process.

The fabrication process developed for the woodpile structure described here was based upon previous work described by Lin and Flemming at Sandia National Lab [5]. Limits imposed by the tools available at the SNF forced some of the steps to be altered in order to achieve the desired structure parameters described above. Some of the steps are still being refined, so this outline describes a work in progress method I will refer to as version 2.0. The general process involves building up the structure layer by layer, using silicon dioxide as a matrix in which silicon feature are embedded. When all the layers are complete, a selective etch is done to remove the silicon dioxide, resulting in a free standing structure of silicon and vacuum. Figure 2 shows a visual outline of the process, supplemented with SEM images of the developing structure.

The first, or zeroth step, in the fabrication is to etch alignment features into the bare silicon wafer. The ASML tool interferes two slightly different frequency lasers over the alignment pattern achieving alignment accuracy of 3σ=60nm. The next step, step one, is to deposit of a layer of silicon dioxide using TEOS gas (tetraethyl orthosilicate) in a LPCVD process. At high temperatures, >600°C, TEOS breaks down into silicon dioxide, which is deposited on the samples in the deposition chamber, and diethylether, which is collected as waste gas. This step is critical in determining the layer thickness of the final structure, and hence a well controlled and highly uniform deposition is desired. Uniformity between wafers in the tube used for the deposition initially varied by 10%, and across a given wafer by 5%. By rotating the wafers, and inverting their positions within the tube half way through a given run, the uniformity improved to 2% between wafers and across a given wafer. The controllability, defined here as the difference between the desired layer thickness and that actually deposited was 5%.

The second and third steps are to pattern the wafer with the given layer features. This is done by first coating the wafer with a layer of resist and then exposing the resist with an image of the desired pattern from the mask. The ASML PAS 5500 i-line stepper is used to resolve the 500nm wide rods desired for this structure. After this the wafer is developed, UV cured, and baked at 110°C for 30 minutes.

Step four uses an AMT 8100 hexode plasma etcher to etch the features patterned into the resist into the oxide layer below. Etch rates are remeasured for each run using blank test wafers. Small features have a slower etch rate than global features, so a 13%

overetch is included when etching the desired sub-micron sized features. Problems with layer to layer bonding have led to even further overetching for the version 3.0 process.

The fifth step is the deposition of a layer of poly-crystalline silicon using LPCVD run at 620°C. This deposition isotropically coats the patterned surface of the silicon dioxide, effectively filling in the etched features with poly-silicon, as can be seen in the second SEM image in Figure 2.

The sixth step is to chemical mechanical polish (CMP) the surface of the deposited silicon down to the surface of the oxide. The CMP tool used for this step is equipped with an end-point detector which measures the friction in the polishing head allowing one to detect a change in friction when the surface of the oxide is reached. The friction drop occurs gradually over the period of 20sec, which corresponds to a potential polishing depth of 24nm in oxide, or 3.7% of the layer thickness.

Once the wafers have been planarized the entire process is repeated for the next layer. This continues for the number of layers desired, currently four, but structures of up to twenty layers will be fabricated once the process flow is finalized. When all the layers are complete, a selective oxide etch is done using buffered oxide etch, consisting of 59% water, 34% ammonium fluoride (NH_4F), and 7% hydrofluoric acid (HF). This selectively etches the oxide leaving the stack of silicon rods free standing surrounded by vacuum.

RESULTS

Four Layer Test Structure. A four layer test structure was fabricated using the process flow described. The intent was to measure the bandgap of the structure using an FTIR (Fourier Transform InfraRed) Spectrometer. Unfortunately there were problems with bonding between successive layers when the oxide matrix was etched away. The third and fourth layers on the majority of structures fabricated washed away during the final etch process. This was eventually attributed to two causes. First, the dry etch in step four did not penetrate down to the layer below, leaving a thin film of oxide between successive layers. Figure 3 shows an SEM profile of a final four layer structure prior to the final etch. It is clear there is a distinct gap between layers 3 and 4. The bond between layers 2 and 3 looks to be intact however. The second potential cause was stress mismatch between the silicon dioxide and poly silicon. A stress mismatch would lead to a strain across the wafer when the oxide was removed, potentially fracturing the bonds between the silicon rods. A 20 hour anneal at 1100°C was done to relieve some of the stress built up from each successive deposition and polishing process. The yield of structures with three layers successfully bonded together after the oxide etch was greatly improved after this anneal. These two causes are addressed in version 3.0 of the process flow by increasing the overetch in step four to 20%, and annealing the wafers after every four layers.

Spectroscopy of Four Layer Test Structure. Due to the problems with the final etch process, FTIR measurements were taken on samples that had not been etched. The only difference between the two samples is that in one case there is a periodic index modulation difference between poly-silicon (n=3.5) and air (n=1.0003), or vacuum, and the other it is between poly-silicon and silicon dioxide (n=1.46). Figure 4 shows the trans-

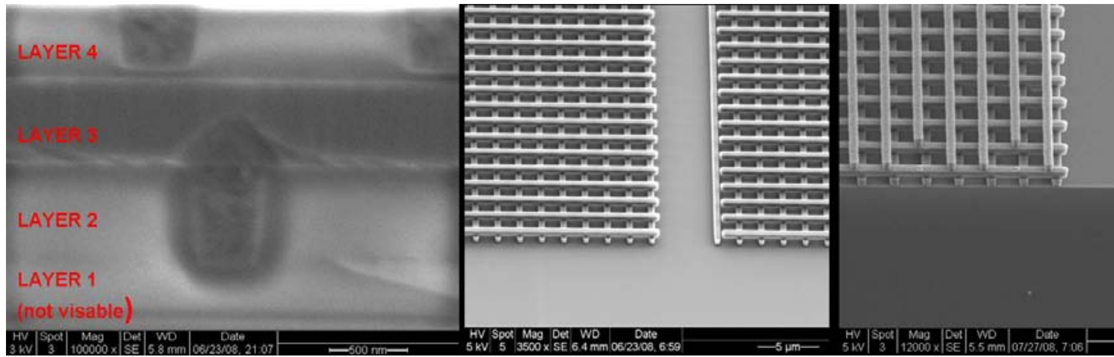

FIGURE 3. Left: A profile image of the four layer test structure prior to the final oxide etch. A clear gap can be seen between layer 3 and 4, which is likely to blame for the poor bond between these layers. There appears to be good contact between layer 2 and 3 however, which would suggest other factors may be responsible for the failure of this bond. Middle: The remaining two layers after the final oxide etch. Right: A structure that has been annealed prior to the final etch. This seems to have improved the bond between layers 2 and 3.

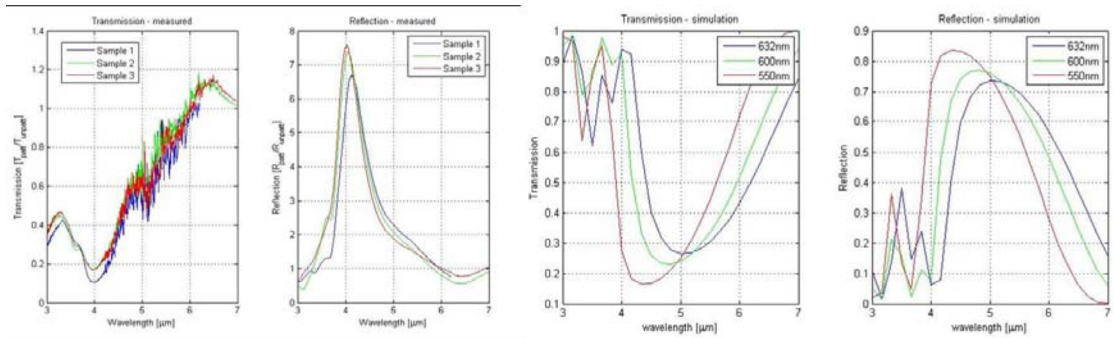

FIGURE 4. Left: Reflection and transmission spectrum for a four layer silicon-silicon dioxide woodpile structure, measured using FTIR. The data has been normalized to the transmission and reflection of an unpatterened region of the wafer adjacent to the patterned region. Right: Simulation of four layer silicon-silicon dioxide woodpile structures with varying layer thickness. Notice how the bandgap shifts to lower wavelength as the layer thickness decreases. SEM images show the layer thickness for the actual structure is generally closer to 600nm, rather than the target 632nm, which may partially explain the discrepancy in center bandgap wavelength between the measured data and simulations.

mission and reflection spectra for the silicon-silicon dioxide four layer woodpile structure. The data has been normalized to the transmission and reflection of an unpatterened region of the wafer adjacent to the patterned region. Simulations were performed using a scattering matrix code in which a 2D plane wave eigenmode solver was used to calculate the modes in each individual layer, assuming an infinite plane of periodically modulated index of refraction, and propagated from layer to layer using the scattering matrix method [7]. This code was uniquely situated to simulating this problem because it does not assume and infinite 3D lattice, bur rather a series of infinite 2D planes stacked on top of one another. Results from the simulation of three structures with varying layer thicknesses are shown in Figure 4.

There are two significant discrepancies between the simulation and the measured data.

First, the resulting bandgap, seen as the region with high reflection, or low transmission, is much broader in the simulation. Defining the bandgap to be the FWHM of the reflection peak, the bandgap for the measured structure is $.772\mu m$, or 18.6% of the center bandgap frequency, while that for the simulation is $3.2\mu m$, or 63%. This discrepancy may be attributed to imperfections in the fabrication process. Variations in layer thickness and rod shape are the most difficult parameters to control precisely during fabrication, which may be to blame for the narrow bandgap. The second discrepancy is the center bandgap wavelength for the measured structure is $4.15\mu m$, while that for the simulation is $4.9\mu m$. Suspecting the layer thickness deviations were to blame for this as well, the simulation was run while adjusting the layer thickness. A center bandgap wavelength of $4.83\mu m$ results for a structure with layer thickness of 600nm in each layer, and $4.33\mu m$ for a structure with 550nm thick layers, as seen in Figure 4. SEM images of the final structure confirm that the layer thickness for each of the layers was less than the target 632nm, generally closer to 600nm. The smaller layer thickness is likely due to the CMP step polishing off a fraction of the oxide layer. Version 3.0 has been updated to increase the target layer thickness to account for this loss of oxide in the CMP step, and will hopefully improve the agreement between measurements and simulation.

CONCLUSION

Despite some challenges encountered, a four layer test structure has been fabricated and initial spectroscopic measurements have been taken. Discrepancies between simulations and measurements are likely due to imperfections in the fabricated structure. Future improvements to the process flow will address the layer to layer bonding issue, as well as the layer thickness deviation. Once the process flow is finalized a full structure with up to 20 layers, including a defect channel will be fabricated and tested at the E163 laser acceleration facility at SLAC.

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