Published by IOP Publishing for Sissa Medialab

Received: *November 6, 2025*
Accepted: *March 4, 2026*
Published: *April 14, 2026*

Topical Workshop on Electronics for Particle Physics
Rethymno, Crete, Greece
6–10 October 2025

First prototype of a low-power timing chip for strip LGAD readout: LATRIC0

C. Wang[a,b] **X. Li**[b,c] **Y. Bai**[b,d] **H. Chen**[b,a] **J. Chen**[b] **Y. Deng**[b,e] **W. Huang**[b,f] **H. Jiang**[b,g] **H. Li**[b,c] **Z. Liang**[b,e] **L. Liu**[b,e] **X. Wang**[b,f] **Z. Wang**[b] **Q. Wu**[b,a] **Q. Yan**[b,c] **X. Yan**[b,c,g,*] **J. Ye**[b,c] **L. Zhang**[a] **G. Zhang**[b,f] **and Q. Zhu**[b,d]

[a] *Department of Physics, Nanjing University, Nanjing, 210093, China*
[b] *Institute of High Energy Physics, Chinese Academy of Sciences, Beijing, 100049, China*
[c] *High Energy Physics Research Center, Henan Academy of Sciences, Zhengzhou, 450046, China*
[d] *School of Physics and Electronic Information, Gannan Normal University, Ganzhou, 341000, China*
[e] *PLAC, Key Laboratory of Quark and Lepton Physics, Central China Normal University, Wuhan, 430070, China*
[f] *School of Nuclear Science and Technology, University of Chinese Academy of Sciences, Beijing, 100049, China*
[g] *School of Physical Sciences, University of Chinese Academy of Sciences, Beijing, 100049, China*

E-mail: yanxb@ihep.ac.cn

Abstract: LATRIC0 is a single-channel readout chip designed for the Outer Tracker (OTK) of the reference detector on the Circular Electron Positron Collider (CEPC). The OTK employs AC-coupled Low-Gain Avalanche Detector (AC-LGAD) microstrip sensors to achieve high-precision spatial (10 µm) and timing (50 ps) measurements. Fabricated using a 55 nm CMOS process, LATRIC0 integrates an analog front-end amplifier and an event-driven ring-oscillator-based Time-to-Digital Converter (TDC) in a compact architecture. Measurements show that the prototype achieves a Least Significant Bit (LSB) of approximately 30 ps from both Time-over-Threshold (TOT) and Time-of-Arrival (TOA). The TDC core consumes less than 1.0 mW, while the total power of the front-end and TDC together is below 7.0 mW. The measured Integral Nonlinearity (INL) and Differential Nonlinearity (DNL) are within 1 LSB. LATRIC0 not only validates the proposed timing architecture but also establishes a foundation for the development of a future fully functional version with 128 channels and 100-µm channel pitch.

Keywords: Analogue electronic circuits; Front-end electronics for detector readout; Timing detectors

*Corresponding author.

https://doi.org/10.1088/1748-0221/21/04/C04028

Contents

2026 JINST 21 C04028

1 Introduction

The Outer Tracker (OTK) is the outermost detector of the tracking system in the Circular Electron Positron Collider (CEPC) experiment [1]. It is designed to provide precise spatial measurement to improve momentum resolution, and precise timing measurement for Time-of-Flight (TOF) based particle identification. The OTK employs AC-coupled Low-Gain Avalanche Detector (AC-LGAD) microstrip sensor technology, which will be the first application where a microstrip sensor simultaneously measures position (10 µm) and time (50 ps) [2]. With an expected input capacitance of 8 pF and a collected charge of 16 fC, the microstrip sensor poses a significant challenge to the power consumption of the readout electronics.

The key technologies are essential in the OTK: the AC-LGAD sensor and its dedicated readout ASIC LATRIC (LGAD Timing Readout Integrated Chip). The AC-LGAD sensor features an internal multiplication layer for charge amplification and an AC-coupled structure that improves spatial resolution while minimizing dead area. The AC coupling design within the sensor [3] isolates the circuit from large leakage currents and protects the ASIC from potential damage caused by bias voltage in case of an LGAD failure. Preliminary tests conducted by the Institute of High Energy Physics (IHEP) demonstrate that both the charge collection efficiency and time resolution meet CEPC specifications, including after irradiation [4, 5]. The final LATRIC ASIC will integrate 128 readout-channels, a clock fanout circuit, a configuration block, and framing and serial output circuits. Each readout channel has a transimpedance amplifier [6], a discriminator, and a Time-to-Digital Converter (TDC). The main requirements for LATRIC include a 30-ps time resolution, low power consumption for thermal management, and a 100-µm channel pitch to match the silicon microstrip pitch. LATRIC0 is an initial single-channel prototype. The second iteration, named LATRIC1, was submitted in October, 2025. It incorporates 8 channels to study high-density layouts, cross-talk, power supply, bonding inductance, and related issues.

This paper focuses on the design and test results of LATRIC0, which includes a analog Front-End (FE), a TDC core, a 128-bit serializer for thermal-code output, and a 40-bit serializer for encoded data output. Both serializers utilize a shift-register-chain structure [7]. The FE exhibits a root mean square jitter of 8 ps under a 2 mV pulse input, while consuming only 6 mW. Section 2 details the circuit design, and section 3 presents preliminary test results.

2 Circuit design

2.1 Overall architecture

Figure 1 shows the architecture of the LATRIC0 chip. The Front-End (FE) stage receives, amplifies, and converts analog negative pulses into digital positive pulses. These digital pulses, along with external test pulses, can be selectively delivered to the TDC core. The TDC core consists of three blocks: a timing controller, an event-driven ring oscillator (RO) with quantization logic, and an encoder. When an event occurs, the timing controller generates an enable signal (RO_key) to start the RO, along with two latch signals for TOA and TOT measurements, respectively. An additional clock cycle and second-stage shift registers are added for calibration (CAL) [8]. All three measurements share a single RO delay line containing 15 delay cells.

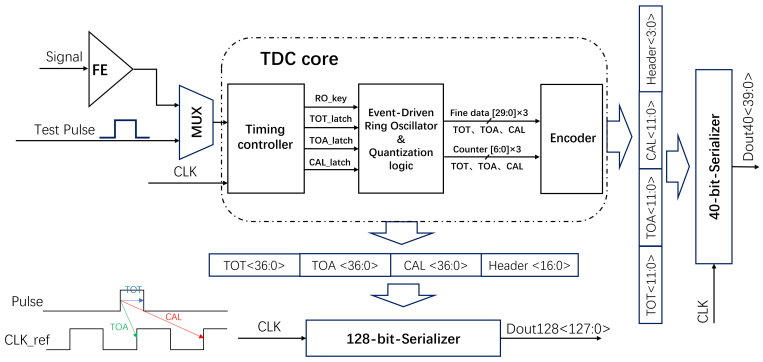

Figure 1. The architecture of the LATRIC0 chip.

Each measurement (TOT, TOA, and CAL) produces 30-bit fine-time thermometer codes and 7-bit coarse-time binary codes. The 111-bit raw data, along with a 17-bit header, are output through a 128-bit serializer. Simultaneously, the encoder converts the thermometer codes into a 5-bit binary code. The resulting 36-bit encoded data, along with a 4-bit header, are output through a 40-bit serializer. The clock (CLK) for the two serializers and TDC core is provided externally.

2.2 Event-driven ring oscillator and quantization logic

Figure 2(a) presents the schematic of the event-driven RO delay line with quantization logic. It comprises an RO core and three latch groups for capturing fine-time information of TOT, TOA and CAL measurements. Compared to single-ended ones, analog differential ROs consume more power. Enabling via a switch at the tail current bias results in long bias settling time and ns-range start-up, making the analog differential ROs unsuitable for event-driven operation. Considering power consumption, the design employs a RO comprising 15 NAND-based delay cells, each providing an average delay of approximately 30 ps. The RO is controlled by an enable signal (RO_key) which is only applied to the first stage. Fine-time quantization is performed using Single-to-Differential (S2D) converters and gated Set-Reset (SR) latches. The S2D converter transforms both the rising and falling edges of the fine-time phases into aligned complementary signals for the SR latch. The latch is symmetric which ensures consistent response to both rising and falling edges, minimizing edge dependent variation.

The quantization timing is illustrated in figure 2(b). The clock used for TOA and CAL measurements is an event-gated clock (CLK_ref). When the leading edge of the PULSE signal arrives, the RO is

2026 JINST 21 C04028

enabled, and the CLK_ref starts, activating the RO and initiating the coarse counting. The first rising edge (R1) of CLK_ref after the pulse arrival generates the CLK_latch1 signal, which captures the TOA information in the latch group1. The falling edge (F1) triggers CLK_latch2, transferring the TOA codes to the latch group2. The rising edge (R2) of CLK_ref generates the second CLK_latch1 pulse, which latches the CAL value into the latch group1, overwriting the previous TOA codes. For the TOT measurement, the trailing edge of the PULSE signal generates the TOT_latch signal, capturing the TOT information in the latch group3. Once all three measurements are completed, RO_key is pulled low, stopping and resetting the RO, clearing the coarse counter, and disabling the gated clock, returning it to a static high state.

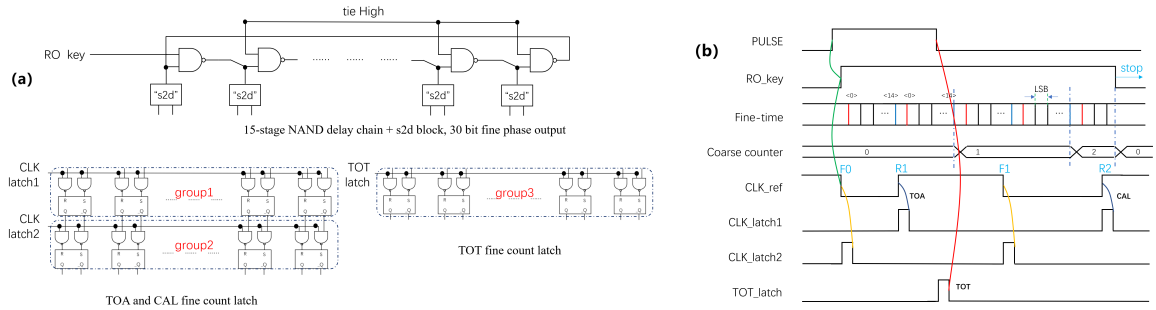

Figure 2. (a): TDC event-driven ring oscillator and quantization logics; (b): Quantization timing.

3 Measurement and performance

3.1 Test setup

Figure 3 shows the test setup for characterization of the LATRIC0 chip. Two operational modes are employed: the FE mode and the test-pulse mode. The 720-MHz clock is provided by a Si5347 board, which also generates a 2-MHz synchronous clock for an oscilloscope. In test-pulse mode, the test pulse is generated using an Agilent 81130A pulse/pattern generator which receives the 2-MHz clock from the Si5347. Both the pulse width and relative delay can be independently adjustable, enabling detailed scans of TOT and TOA transfer curves, respectively. To characterize the pulse generated by the 81130A and Si5347, we used an oscilloscope to measure the standard deviation (σ) of both the pulse width and the relative delay of the pulse with respect to its synchronized clock. The measured σ is 15.8 ps for the pulse width and 14.2 ps for the relative delay. In FE mode, a passive RC differential circuit generates the analog pulse that simulates the sensor signal. Power consumption is measured through a 1-Ω resistor in series with each supply line.

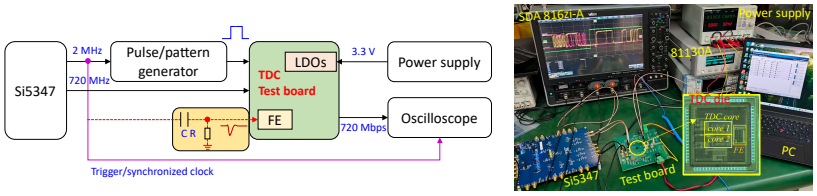

Figure 3. Test setup for characterization of the LATRIC0 chip.

2026 JINST 21 C04028

3.2 Measurement results

Figures 4(a) and 4(b) show the measured TOA and TOT transfer curves in test-pulse mode, respectively. The coarse transfer curve for TOA is obtained by scanning the delay between the pulse and the synchronized clock over a 25-ns range with 1-ns step. The fine transfer curve for TOA spans a one-coarse-count range of about 1 ns with 6-ps step. The coarse transfer curve for TOT is measured by scanning the pulse width over the same 25-ns range with 1-ns step, while the fine transfer curve spans a range of 5 to 6 ns with 10-ps step. The transfer fitting results show average Least Significant Bit (LSB) values of 31.1 ps for TOA and 31.0 ps for TOT measurements, with the calibrated LSB derived from CAL values of 31.1 ps. These three values are very close, indicating the effectiveness of the self-calibration capability of the design.

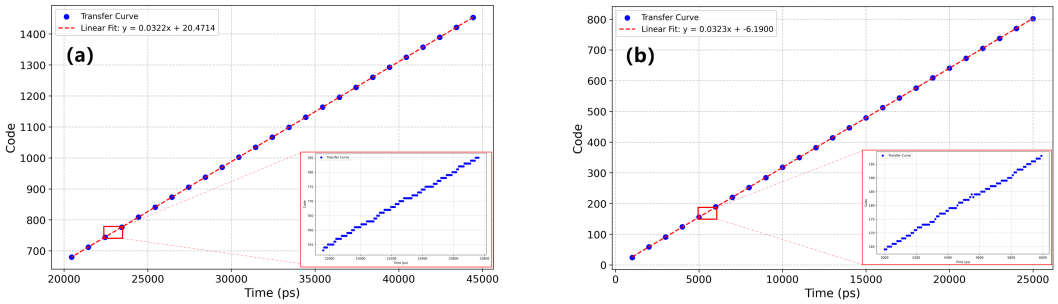

Figure 4. Measured transfer curves: (a) TOA; (b) TOT.

Figures 5(a) and 5(b) show the measured differential nonlinearity (DNL), integral nonlinearity (INL) of TOA and TOT. The results indicate that the DNL and INL for both TOT and TOA remain within ±1 LSB. Figures 6(a) and 6(b) show the time precision (sdev) for TOA and TOT under test-pulse mode. Each data point is based on at least 300 samples. The associated statistical standard deviation of these samples is utilized to characterize the time precision of the respective data point. The time precision achieves better than 0.51 LSB for TOT and 0.92 LSB for TOA, corresponding to 15.8 ps and 28.6 ps for TOT and TOA, respectively, based on the fitted LSB values.

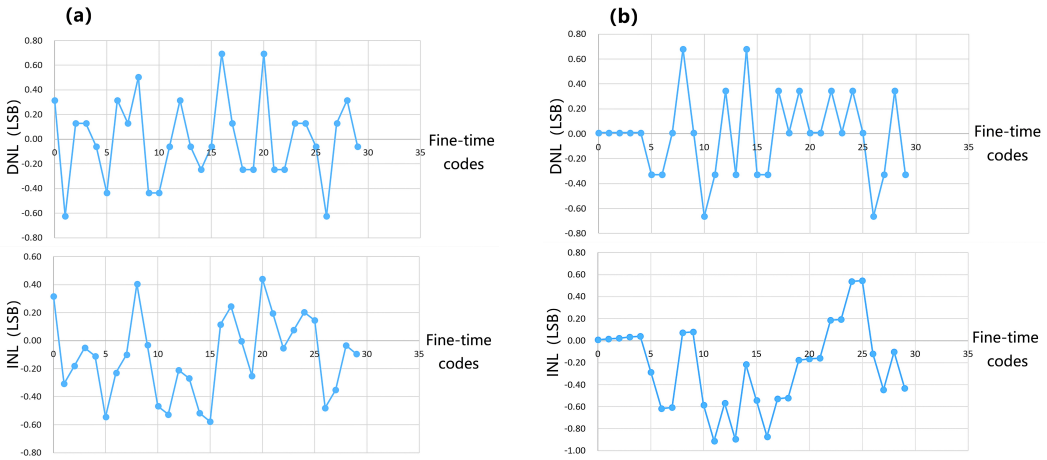

Figure 5. (a): Nonlinearity of TOA; (b): Nonlinearity of TOT.

2026 JINST 21 C04028

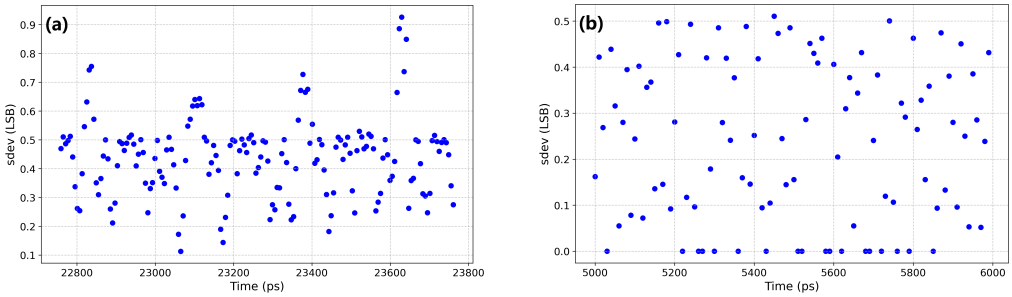

Figure 6. (a): Timing precision for TOA; (b): Timing precision for TOT.

In FE mode, which represents a complete readout channel, the amplitude of the simulated input pulse is about 16.8 mV, with the discriminator threshold held constant at an appropriate value. The preliminary results indicate a timing precision of 1.1 LSB (34.1 ps) for FE-TOT and 0.91 LSB (28.3 ps) for FE-TOA, thus validating the functionality of the full readout chain. Figure 7 presents the measured TOT distribution of the leading-out signal after amplification of the FE. Additionally, the minimum detectable input pulse width is characterized to be less than 210 ps.

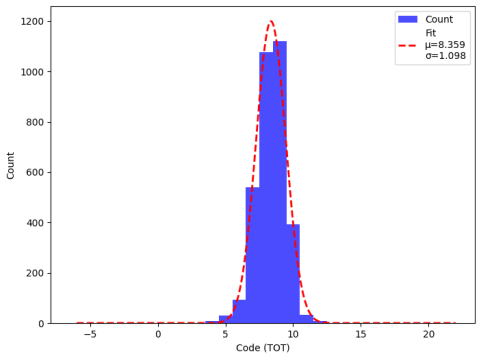

Figure 7. The measured TOT distribution of the leading-out signal after amplification of the FE.

The TDC core employs an event-driven design, resulting in power consumption proportional to the event rate. When an event arrives, the ring oscillator and S2D circuitry oscillate for up to two clock cycles, which constitutes the primary source of dynamic power consumption. The static power consumption of the TDC core is less than 60 µW. The measured power consumption of a single TDC core channel as follows: 0.60 mW at 2 MHz, 0.36 mW at 1 MHz, and 0.12 mW at 500 kHz. The FE maintains a constant power consumption of 5.88 mW. The total measured power per channel at an event rate of 1 MHz is 6.24 mW.

In the OTK application scenario, the total event rate across 128 channels is below 1 MHz. With a static power consumption of less than 60 µW per TDC channel, the total power consumption for the 128 TDC cores is expected to be below 8 mW. For the FE, a pad pitch of 60 µm is used in the layout, with a single-channel height of 100 µm. On average, every four channels are allocated six pads: four for input signals and two for power supply. This configuration helps mitigate significant IR drop issues when scaling the channel count. Crosstalk effects and the power consumption of the data output digital block will be further validated in testing of the eight-channel version, latric1. The OTK cooling system requires the average power per channel to be below 20 mW, a specification met by the current design.

2026 JINST 21 C04028

4 Conclusions

Measurement results confirm that the LATRIC0 prototype achieves a LSB of approximately 30 ps for both Time-over-Threshold and Time-of-Arrival measurements. The TDC core maintains both DNL and INL within ±1 LSB across the measurement range. In test-pulse mode, the timing precision reaches 15.8 ps for TOT and 28.6 ps for TOA. Power consumption remains below 6.24 mW per channel at 1 MHz event rate, with the TDC core consuming 0.36 mW. The prototype demonstrates a minimum detectable pulse width below 210 ps. These results validate the integration of the FE with the TDC core and confirm the feasibility of the proposed architecture for high-precision timing measurements. LATRIC0 thus provides a foundation for developing the future 128-channel LATRIC chip.

Acknowledgments

This work was supported by the High Energy Physics Research Center, Henan Academy of Sciences, and by the Independent Deployment Project of the Institute of High Energy Physics, Chinese Academy of Sciences (No. 2023000134).

References

[1] CEPC Study Group collaboration, *CEPC Technical Design Report — Reference Detector*, arXiv:2510.05260.

[2] G. Giacomini, *LGAD-Based Silicon Sensors for 4D Detectors*, *Sensors* **23** (2023) 2132.

[3] M. Li et al., *The Performance of Large-Pitch AC-LGAD With Different N+ Dose*, *IEEE Trans. Nucl. Sci.* **70** (2023) 2134 [arXiv:2212.03754].

[4] L.A. Beresford et al., *Destructive breakdown studies of irradiated LGADs at beam tests for the ATLAS HGTD*, 2023 *JINST* **18** P07030 [arXiv:2306.12269].

[5] S. Ali et al., *Performance in beam tests of carbon-enriched irradiated Low Gain Avalanche Detectors for the ATLAS High Granularity Timing Detector*, 2023 *JINST* **18** P05005 [arXiv:2303.07728].

[6] C. Agapopoulou et al., *Performance of a Front End prototype ASIC for picosecond precision time measurements with LGAD sensors*, 2020 *JINST* **15** P07007 [arXiv:2002.06089].

[7] X. Li et al., *4 Gbps serializer circuits in a 180 nm technology for monolithic pixel sensor prototypes developed for the CEPC vertex detector*, *Nucl. Instrum. Meth. A* **1063** (2024) 169282.

[8] W. Zhang et al., *An ASIC for ToF-PET application with MCP-PMTs*, 2025 *JINST* **20** C04024.

2026 JINST 21 C04028