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The H1 Central Silicon Tracker

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Abstract

Since 1997, the H1 detector at the HERA collider at DESY, Hamburg has been equipped with a two layer silicon vertex detector (CST). The CST uses double sided, double metal layer sensors; it is read out with a specifically designed analog pipeline chip (APC), the signals are transmitted optically. The whole detector has a thickness of only 0.40 g/cm, corresponding to 1.4 $\%X_0$. An asymptotic impact parameter resolution of 57 μm has been achieved.

In 2001, the detector was redesigned for the HERA luminosity upgrade. It has been equipped with a new version of the readout chip APC that has been produced in radiation hard DMILL technology.

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Key words: Silicon vertex detector
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1 Introduction

After almost nine years of operation the ep collider HERA in Hamburg was shut down in August 2000 for one year for an extensive luminosity upgrade. In the course of this upgrade, the H1 detector was equipped with a beryllium–aluminum beam pipe of elliptical cross section. This made a redesign of the central silicon tracker of the H1 detector necessary.

The first part of this contribution will describe the performance of the CST that was achieved during the first years of its operation. After a discussion of the mechanical redesign, the development of new front end readout chips in radiation hard DMILL technology is presented. Finally, some aspects of the separation of readout hybrids from the sensors are discussed.

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2 The H1 Central Silicon Tracker

The Central Silicon Tracker (CST) of the H1 detector is a joint project of the Swiss Federal Institute of Technology (ETH) Zurich, the University of Zurich, and the Paul Scherrer Institute in Villigen, Switzerland [1]. It consists of two barrel layers of double–sided silicon detectors.

As installed in 1996, it comprises 12 ladders in the inner layer at a radius of 6 cm, and 20 ladders in the outer layer at 10 cm radius. Each ladder consists of six sensors of size $5.9 \times 3.4\,\mathrm{cm}^2$ and 300 μm thickness that are read out by two hybrids at either end of the ladder. The sensors are made out of high–resistivity silicon ($> 6\,\mathrm{k}\Omega\mathrm{cm}$) produced by Wacker [2]. The 640 p–side strips run parallel to the sensor's axis and measure the $r\phi$ coordinate; the strip pitch is 25 μm, and every second strip is read out. The n–side has 640 strips with 88 μm pitch and no intermediate strips; these strips run perpendicular to the sensor's axis and are read out via a second metal layer. The readout capacitance is 9 pF on the p–side and 19 pF on the n side for one sensor. Three sensors are bonded together to form a half ladder which is read out by one hybrid at the end. The sensors are DC coupled.

The readout hybrid [3] is made of 0.6 mm thick AlN, a ceramic with high thermal conductivity. The bias voltage is applied across both sides of the hybrid, which float at different voltages. The steering signals are transmitted through small 15 pF coupling capacitors.

Each side of the hybrid contains five APC128 chips [4], which accomodate 128 preamplifiers and 32 stage analog pipelines; all five chips are read out serially. A second ASIC chip developed at PSI, the decoder chip, uses four differential input signals to generate all steering signals necessary for the operation of the APC128. The two output signals per hybrid are amplified by a discrete amplifier and transmitted via a capton cable to the end ring print. Two adjacent hybrids are read out sequentially via one readout line for each side; the signals are transmitted optically by LEDs on the end ring prints. The four steering signals for the decoder chip are also transmitted optically to receivers that are located on these prints [3].

This design allows to have a very thin detector; particles that pass through the sensitive region of the detector see only 0.40 g/cm of material (including mechanical and electrical shielding and thermal insulation), corresponding to $1.4\,\%\,X_0$, of which 0.16 g/cm ($0.7\,\%\,X_0$) are due to the sensors themselves.

However, on the n–side three sensors with double metal layer have to be bonded together, which leads to a total input capacitance of 57 pF for the preamplifiers; in conjunction with the short shaping time of about 300 ns this results in a signal over noise ratio of $S/N = 7$ in units of single strip noise.

This S/N ratio is only marginally sufficient for reliable hit detection. The short shaping time is necessitated by the HERA bunch crossing frequency of 10.4 MHz. On the p–side, the S/N ratio is 19.

After the occurence of a trigger signal, the analog pipeline is stopped. The APCs allow to add and subtract the signals of several pipeline stages in parallel: three stages are added to collect as much signal charge as possible, then three empty stages are subtracted to reduce the pedestal. Subsequently, the 1280 signals of two adjacent hybrids are transmitted serially with one of the 64 LEDs over a distance of about 30 m, which takes approximately 1.2 ms. The readout speed is limited by the capacitive load of the output amplifier of the APCs; their output signal travels only about 7 cm to the input of the amplifier transistor, but due to the high susceptibility of the AlN ceramic, this corresponds to a considerable capacitance.

In the counting house the signals are processed by eight Power PC 604 processor boards operating at 96 MHz [1]. Each processor board is equipped with a custom made mezzanine board designed by Rutherford Appleton Laboratories, containing eight 12bit flash ADCs and a FIFO logic to buffer the incoming data.

These processor boards perform pedestal subtraction, common mode correction, zero suppression, and hit finding, so that the raw data information of 1 Mbyte is reduced to a manageable amount of about 20 kbyte per event.

3 Performance of the CST in 1997 to 2000

In building the CST, a mechanical accuracy of about 0.1 mm in three dimensions has been aimed at and achieved. This accuracy is sufficient to prevent mechanic stress of the sensors; the final accuracy as needed for the vertex reconstruction is obtained by an alignment procedure based on cosmic ray muons and high momentum tracks from ep interactions. The internal alignment determines the relative positions of all 64 half ladders with respect to each other, while the location of the three sensors that form one half ladder are known from optical laboratory measurements. The result of this internal alignment is valid for the whole run period, i. e. as long as the CST is not touched.

The external alignment determines the position and orientation of the whole CST with respect to the surrounding tracking chambers. The CST has a three point support that determines its position relative to the carbon fiber tube, which is the inner wall of the surrounding tracking chamber. Movements of the CST on the micrometer scale have been observed on a time scale of hours,

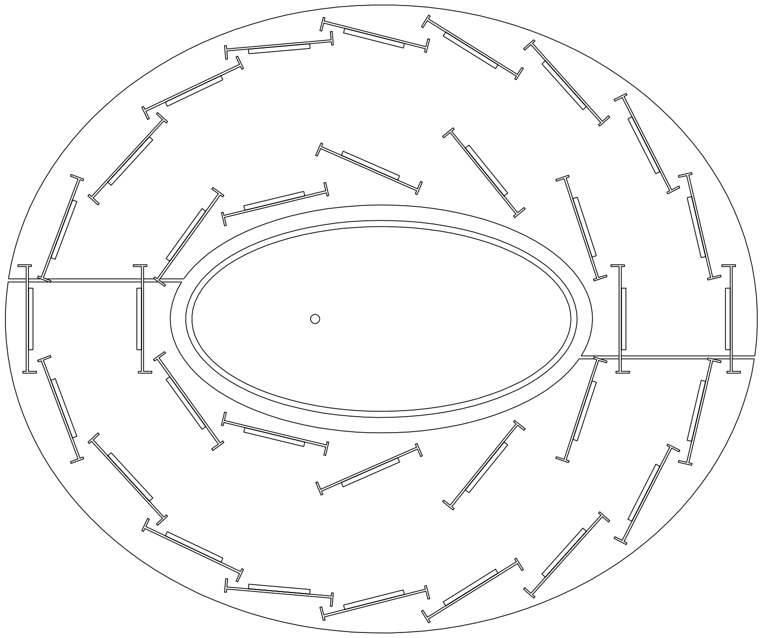

Fig. 1. Arrangement of the 32 ladders of the upgraded H1 Central Silicon Tracker. The small circle in the middle denotes the interaction point.

i. e. during a single luminosity fill. This is most likely due to temperature variations, which cause thermal expansion of the support legs and may lead to sagging of the surrounding carbon fiber tube.

A single hit resolution of 12 μm on the p–side and 22 μm on the n–side has been achieved. After complete alignment, this results in an impact parameter resolution of 37 μm for high momentum tracks [1]. The average hit efficiency is 97 % and 92 % on the p–side and n–side, respectively. The hit definition demands a signal that is 5 times bigger than the single strip noise for the p–side (4 times for the n–side). Inefficiencies on the p–side are mainly due to dead or noisy readout channels, whereas on the n–side the lower signal to noise ratio leads to a reduced hit finding efficiency.

4 Mechanical Design of the CST Upgrade

The mechanical layout of the upgraded CST followed largely the original design. Due to the elliptical shape and non–concentric position of the new beam-pipe, a new and highly irregular arrangement of the silicon ladders had to be found. Since it was not foreseen to install additional sensors, the ladders were again arranged in two layers with 12 and 20 ladders. The inner layer was placed as closely as possible to the beam-pipe, the outer layer as far away as possible. Care was taken to have sufficient overlap between adjacent ladders (at least 450 μm) to facilitate internal alignment with high momentum tracks.

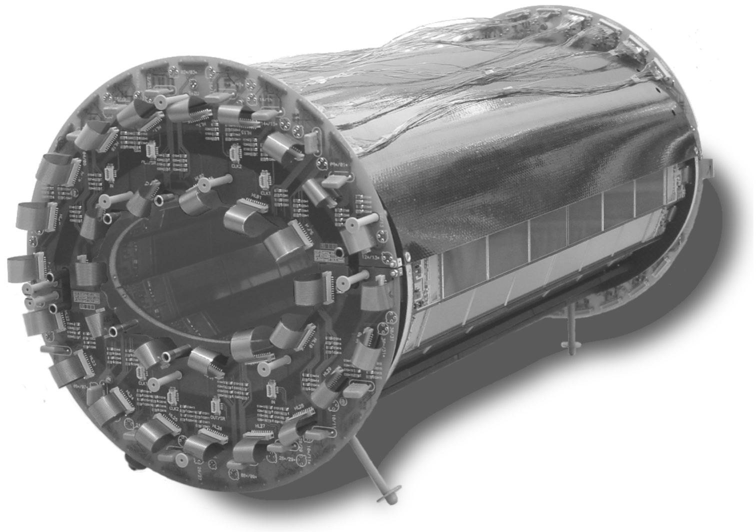

Fig. 2. A picture of the upgraded H1 Central Silicon Tracker. The end ring prints for electrical power and signal distribution are visible, with the capton cables that lead to the readout hybrids. At the upper half the capton foil shielding and the power cables that connect the front and backside prints are already installed. In the lower part, the sensors are still visible.

The ladders were placed such that straight tracks coming from the interaction point pass them at normal incidence to ensure the best possible position resolution. The resulting ladder arrangement is shown in Fig. 1.

Similar to the old design, the ladders are mounted on carbon fiber balconies protruding from the two carbon fiber end flanges. No additional mechanical frame exists, the whole structure is held by the sensor ladders, which are reinforced by carbon rails of $5 \times 0.6\,\mathrm{mm}^2$ cross section at their edges; this design minimizes the total amount of dead material.

The end flanges provide the necessary mechanical stability and cooling. The mechanical stability is provided by two carbon fiber plates of 1.2 and 0.7 mm thickness. Sandwiched between these is a roughly half–moon shaped copper cooling box which is cooled by water. A Rohacell spacer provides additional stability. The carbon fiber balconies are laminated in one piece such that the fibers run along the direction of the heat flow, because the thermal conductivity of carbon is about eight times higher along the fiber direction than transverse to it.

The endring prints that distribute the electrical power and hold the LEDs for signal transmission to and from the CST are mounted onto the end flanges (Fig. 2).

Most of the electrical power is dissipated in the APC chips. This heat, about 4 W per hybrid, is conducted through the AlN hybrid and the carbon fiber balcony (which has a cross section of $20 \times 1.5\,\mathrm{mm}^2$) to the copper cooling box. The cooling box has a wall thickness of about 0.5 mm. In spite of the material budget penalty, copper was chosen for the box because aluminum corrodes electrochemically, since the external pipework is made out of copper, as well as parts of the water pumps; stainless steel proved too difficult to weld. Unfortunately, first operating experience indicates that the box design is not optimal because it has a tendency to develop air pockets; also the high flow rate necessary for turbulent flow, which would improve the heat conductance between water and walls, is not easily achieved.

5 Design of New Frontend Readout Chips

After three years of operation, in April 1999 the CST had received an integrated dose of about 300 Gy, mostly due to synchrotron radiation; most of this dose was received in a short time at the beginning of 1999. Considerably lower than the projected radiation tolerance of the CST of about 1000 to 2000 Gy, this dose lead to an unexpected degradation of the signals in the APC128 chips, which is most likely due to increased leakage currents on the chips.

Therefore a project was launched to develop new, radiation hard versions of the two ASIC chips, the decoder and the APC128 [5]. The original chips were fabricated in SACMOS–1 μ technology. The new chips were designed in DMILL (*Durci Mixte sur Isolant Logico–Linéaire*), a radiation hard silicon–on–insulator technology with $0.8\,\mu$m feature size developed by CEA, Saclay, and now available as commercial process from ATMEL. DMILL chips are designed to withstand a dose of at least 10 kGy, if they are specially tested the manufacturer guarantees a radiation tolerance of 100 kGy. DMILL components have about the same footprint as SACMOS components; this greatly facilitated the transfer of the design, which was achieved in only two months.

The main challenge of the project was the preamplifier design of the APC128; a circuit working well in one technology does not necessarily achieve the same performance in another technology. Therefore the prototype chips contained different preamplifier designs: additionally to the one stage push–pull amplifier employed in the SACMOS chip, a two–stage version was implemented. Both basic designs were implemented in several variations with differing channel lengths of the FETs; in total, five variations were tested.

The main stumbling stone turned out to be the design of the feedback resistor of the preamplifier; in the prototypes, this was implemented as a chain of five n–MOS transistors with a $W/L = 2.2\,\mu\mathrm{m}/90\,\mu\mathrm{m}$ each. This design had an intolerable tendency to oscillate and was therefore replaced by a riding feedback in the final design, which works fine.

As discussed earlier, for a successful operation of the n–side of the CST, a low amplifier noise at high (57 pF) input capacitance is mandatory. Laboratory measurements show that the new DMILL design has a somewhat higher noise than the SACMOS chip at low input capacities, but is superior above 40 pF.

The final chip design was submitted for fabrication in August 2000, and the wafers were received early March 2001. The yield of usable chips, which include chips with up to one malfunctioning preamplifier or several malfunctioning storage cells, varied between 37 % and 69 % between the wafers received; on average, it was 56 %. Wafers from a second batch delivered later show an improved yield.

6 Fabrication and Installation

With the APC chips that were available, 28 out of 32 ladders of the CST could be equipped with new readout hybrids; careful design of the new chips allows the operation of ladders with old and new chips in a single system. Since the radiation dose received by the CST during HERA–1 operation was significantly below the projected tolerance of the sensors, no new silicon sensors were produced. Therefore, for 28 ladders the readout hybrids had to be cut away from the sensors.

Sensors and hybrids are mechanically held together by a carbon rail at the side, which can be milled away relatively easily. After that, sensor and hybrid are only connected by the 1280 bond. No problems e. g. due to carbon fiber dust were observed after this procedure. Prior to the removal of the hybrid, the bond wires were glued with epoxy to the readout chips; then, the hybrids were slowly pulled away from the sensors. With this procedure, about 99 % of the bond wires were severed on the sensor side when the hybrid was removed. The remaining bonds were removed by hand. Afterwards the bond pads were not usable anymore, mostly due to remains of the bond wire on the pad. Therefore, the sensors were rotated by 180° and the spare set of bond pads was used.

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