

Readout system and testbeam results of the RD50-MPW2 HV-CMOS pixel chip

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Abstract. The RD50-CMOS group aims to design and study High Voltage CMOS (HV-CMOS) chips for use in a high radiation environment. Currently, measurements are performed on RD50-MPW2 chip, the second prototype developed by this group. The active matrix of the prototype consists of 8x8 pixels with analog front end. Details of the analog front end and simulations have been already published earlier. This contribution focuses on the Caribou based readout system of the active matrix. Each pixel of the active matrix can be readout one after the other. Relevant aspects of hardware, firmware and software are introduced. As a first stage, firmware for a standalone setup is introduced and details on data flow are given. Afterwards, a second stage of the firmware capable of synchronizing with other detectors and accepting triggers is presented, focusing on operation of the chip in combination with a tracking telescope to measure efficiency and residuals.

1. Introduction

Depleted monolithic active pixel sensors (DMAPS) are a promising option for future tracking detectors in high energy physics. The availability of high-resistivity Si substrates and High Voltage (HV) capable structures in commercial CMOS processing makes them suitable as detectors in high-luminosity environments. DMAP sensors integrate the sensing diode into the bulk silicon of commercial CMOS chips. It also allows to use very small transistors which results in high granularity pixels with sophisticated in-pixel logic. Thus, amplification, sampling and digitization of signals as well as timing measurement and data reduction can be done on-chip.

The RD50 HV-CMOS group is studying radiation-hard DMAP sensors in the course of the CERN RD50 collaboration. This includes not only sensor development itself, but also characterization, electronics for data acquisition (DAQ) and readout software. This contribution focuses on the DAQ system and data flow of the RD50-MPW2 chip.

2. RD50 HV-CMOS Road Map

The first chip developed by the RD50 HV-CMOS group was manufactured in a multi project wafer (MPW) run and called RD50-MPW1. The chip was fabricated in the LFoundry 150nm process with a wafer thickness of 280 μ m. Measurements have shown, that the analog behavior of RD50-MPW1 was suffering from high leakage current and low breakdown voltage [1]. Moreover the chip showed some shortcomings in the digital readout. In order to tackle one issue after the other, the group decided to focus on improvements of the analog behavior of the pixel cell



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and designed a second iteration of the chip, the RD50-MPW2. The chip only has an analog front end in the pixels and no digital readout. As a result of these improvements, the pixel in the active matrix have been enlarged from $50\mu\text{m} \times 50\mu\text{m}$ in RD50-MPW1 to $60\mu\text{m} \times 60\mu\text{m}$ in RD50-MPW2, still focusing on the minimal possible size to achieve a highly granular matrix. An enlarged distance between the collection electrode and the biasing implant lead to a decrease of leakage current by four orders of magnitude. This massive improvement is suitable to be used in future tracking devices, where power dissipation is one of the big challenges. The analog characteristics and performance have been presented for example in [2].

In the course of characterizing and testing of RD50-MPW1 and later the RD50-MPW2 chips, a readout chain to be used in laboratory measurements as well as for beam tests has been implemented. In addition to the standalone data acquisition, this readout system provides techniques to synchronize with other detectors by an AIDA trigger logic unit (TLU) [3].

3. Overview RD50-MPW2

RD50-MPW2 consist of different test structures for studying the analog behavior of the chip [4]. One main part is the active pixel matrix, which is depicted in figure 1. It includes a bias block, configuration registers (implemented as shift register) and the pixel matrix itself with 8 by 8 pixels and a size of $60\mu\text{m} \times 60\mu\text{m}$ each. Each pixel has a charge sensitive amplifier (CSA), an analog output after a source follower, called SFOUT, and a digital output after a comparator, called COMPOUT, as shown in Figure 2. The matrix provides pixels of two different flavors of readout: columns 0-3 are continuous reset pixels, while columns 4-7 are switched reset pixels. They differ in their feedback loop of the CSA. The feedback capacitor of the continuous reset pixel is continuously discharged by a fixed current I_{FB_CONT} source, leading to an amplitude dependent output signal length. For the switched reset pixel, the feedback capacitor is discharged by a comparably high current I_{FB_SW} source, which is switched on as soon as the signal is above a threshold and COMPOUT is high, resulting in a charge independent pulse length. A pixel from the latter type is chosen for all measurements in this contribution.

It is important to mention that the matrix is analog only and moreover only one pixel at a time can be read out. The output of each pixel is tri-stated and ORed together for each column and all columns are again ORed together and routed to a bonding pad. This is done for both SFOUT and COMPOUT, respectively.

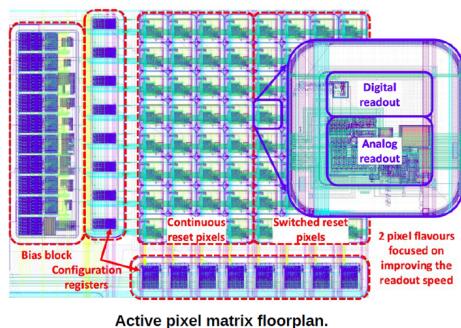


Figure 1. The analog pixel matrix of RD50-MPW2 [4].

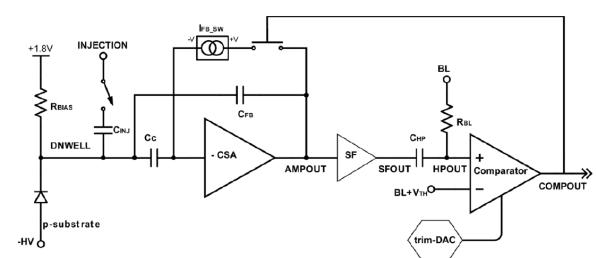


Figure 2. Schematic of a switched reset pixel [4].

4. Standalone DAQ for laboratory tests

The DAQ system is based on the Caribou framework [5], which includes hardware, firmware and software packages for configuring, powering and reading out pixels sensors. A detailed

description of the setup used for RD50-MPW2 can be found in [6]. This contribution focuses on firmware developments.

Figure 3 shows a schematic of the standalone firmware, which can be used for laboratory measurements such as charge injection by the integrated injection circuit and charge generation by a radioactive source. The COMPOUT is buffered and connected to the FPGA (located at the Xilinx SoC ZC706 Evaluation Board, which is part of Caribou). This simple implementation includes a counter with a 200MHz clock input which is set and reset at the two edges of the pulse. It provides the 16-bit time over threshold (ToT) value at the output. Furthermore, one edge is shaped and counted in an asynchronous counter, which provides another 16-bit as output for counting particles. Those two times 16 bits are feed into the AXI FIFO, which is part of the standard AXI-bus from Xilinx [7].

The functions to access these FIFOs with the CPU are already implemented in the Caribou framework. The readout software just polls the AXI FIFOs every 100 μ s and writes the values into an ASCII file. The integrated peary command-line interface (peary_cli) is used for this purpose.

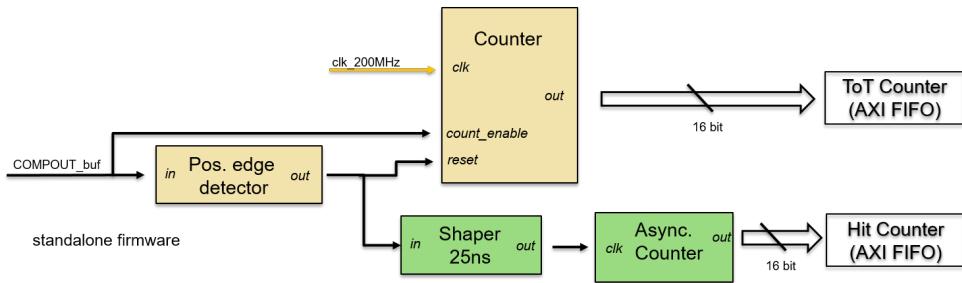


Figure 3. Standalone firmware of RD50-MPW2.

5. Testbeam setup and DAQ

5.1. Synchronizing with other detectors

Synchronization with other detectors and the capability of accepting trigger signals is a crucial need of a detector in order to work in a tracking setup during testbeams. Thus, the standalone firmware was modified to implement this functionality. The extended firmware is called testbeam-firmware and a schematic is depicted in figure 4. The main component is another FIFO which has a delayed input.

The FIFO captures the ToT value, calculated in the same way as in the standalone-firmware, whenever a particle hits the collection electrode. The second input of the FIFO is an internal counter. The FIFO is read out whenever the value of the counter matches with another counter working at the same speed, but delayed by a certain amount of time Δt . The blocks implementing this behavior are enclosed by the red-dashed rectangle in figure 4.

The whole circuit has another input, the trigger signal, which is generated by the TLU. It is issued by the coincidence of two scintillators placed behind the detector and only forwarded to all sub-detectors if none of them is vetoing triggers. This is needed, in order to record data only when every detector is ready. Other data is thrown away, which is done in RD50-MPW2 with a simple AND gate which enables the writing of the AXI FIFO. If a trigger is issued, the (delayed) value of ToT is written into the AXI FIFO along with a trigger number from the TLU in order to synchronize events with other detectors. The important parameter of this setup is the time of the delay Δt , which needs to match exactly with the trigger delay. This was determined before the testbeam by directly measuring Δt with an oscilloscope.

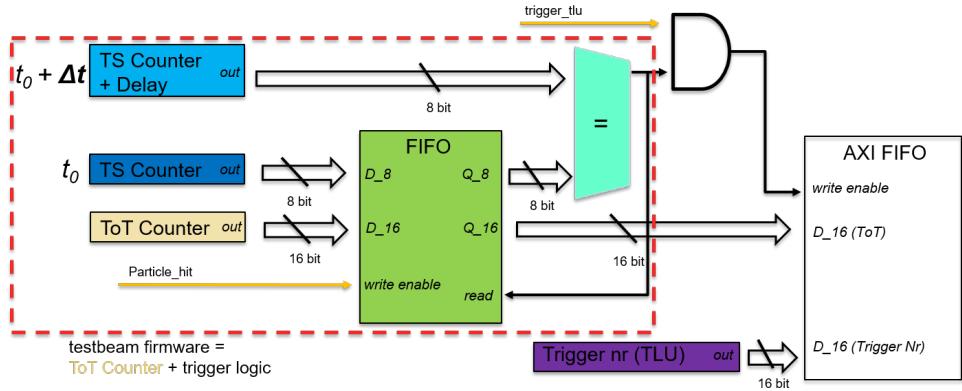


Figure 4. Testbeam firmware of RD50-MPW2.

5.2. Testbeam setup and beam parameters

Both setups were tested with a proton beam at MedAustron [8]. Since this is a medical facility for cancer treatment with a high nominal particle rate in the GHz region, so-called low-flux parameters have been determined in order to provide a more suitable beam for tracking devices [9]. For testing RD50-MPW2, setting "high (MED)" at an energy of 252.7 MeV and a proton rate of 3.73 - 5.21MHz was used. Due to restrictions by the telescope, the overall event rate was at around 30 kHz.

6. Testbeam results

In order to test the standalone firmware RD50-MPW2 serves as device under test (DUT) and is put directly into the beam. As one can see in figure 5, the ToT value is independent from deposited energy for switched reset pixels, since the CSA is resetting nearly instantaneous after the switch is closed. The standalone firmware of RD50-MPW2 roughly measures this value as well, but with a bin size of 5 ns, which is needed for measuring longer pulses from the other pixel flavour. Calibration to get charge in units of electrons has not been performed yet.

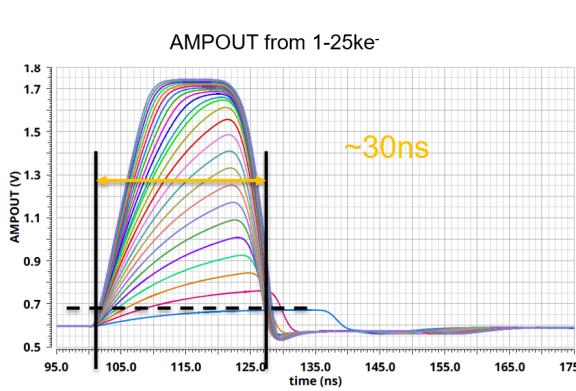


Figure 5. Simulation of the analog output gives a ToT of about 30ns [4].

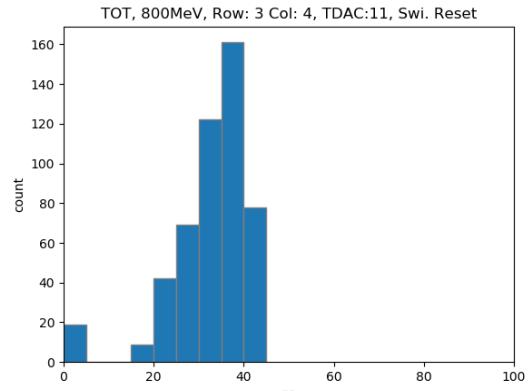


Figure 6. ToT measurements using the testbeam-firmware show a distribution peaking at 35ns.

In order to test the testbeam-firmware, RD50-MPW2 is put in the middle of a beam

telescope, which uses two double sided silicon strip detectors (DSSDs) upstream and two DSSDs downstream of the DUT. The telescope is triggered by the coincidence of two scintillators, which are located at the very back of the setup. Analysis of the tracking capability of RD50-MPW2 is ongoing. Due to small geometric acceptance (just one single pixel is recorded at the same time) very high statistics is needed to get reliable results for tracking studies. This is in contradiction to the maximum rate of the telescope of 30 kHz. Thus the goal of this setup is to measure pixel efficiency, which can be done with a single pixel.

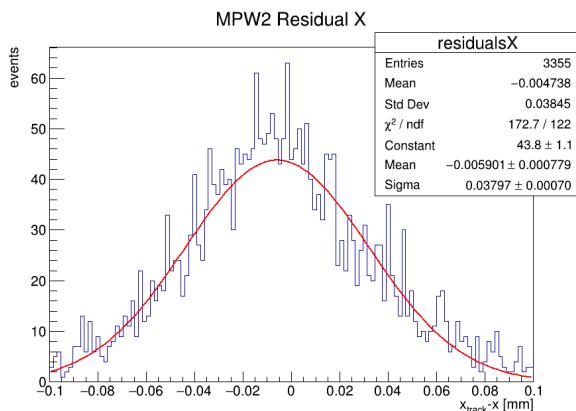


Figure 7. The depicted distribution of residuals for the DUT are centered around 0 and have a distribution very similar to the planes of the telescope. This is expected, since only a constant value, the position of the pixel, is subtracted from the uncertainty of the beam position, which has no influence on the distribution of residuals. The rather low beam energy causes multiple scattering of beam particles in air, which widens the distribution of residuals for all detectors. It is only in the order of half of a pitch for the telescope planes, instead of the theoretically expected value $\text{pitch} / \sqrt{12}$.

7. Conclusion and outlook

In this paper we report the first data taking with the RD50-MPW2 DMAPS chip in a testbeam environment. It has been shown that both readout firmware versions work very well and demonstrate a good agreement of the analog performance of the chip with simulation results. Also the synchronization of the chip with other detectors is working and analysis of tracking data shows consistent results. The main goal of this measurement was to familiarize with the special high-rate, but low-energy environment at MedAustron and prepare the DAQ system and analysis software for the successor chip of RD50-MPW2, which has been achieved.

Currently, RD50-MPW3 is being developed which will have a digital front end and the capability of reading out the full matrix. Knowledge gained for RD50-MPW2 in DAQ and analysis will be a valuable input for the study of this successor sensor.

Acknowledgments

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References

- [1] Franks M and et al 2020 Initial I-V and e-TCT measurements of a depleted CMOS sensor within the CERN-RD50 collaboration 36th RD50 Workshop (Monolithic Sensor session)
- [2] Marco Hernández R and et al 2020 Latest Depleted CMOS Sensor Developments in the CERN RD50 collaboration (to be published in JPS Conference Proceedings)
- [3] Baesso P, Cussans D and Goldstein J 2019 *JINST* **14** P09019
- [4] Zhang C 2019 *RD50-MPW2 Documentation* RD50-HVCMOS-group version 1.2 29/04/2019 ed
- [5] Vanat T 2020 *PoS TWEPP2019* **370** 100
- [6] Irmler C and et al 2020 Data acquisition system for characterization of RD50 HV-CMOS active pixel matrix prototypes 36th RD50 Workshop (Monolithic Sensor session)
- [7] Xilinx 2011 *AXI Reference Guide* ug761 (v13.1) ed
- [8] Benedikt M (ed) 2009 *Physics opportunities at MedAustron : white book*; 1. ed. Schriftenreihe der Technischen Universität Wien (Vienna: Univ. of Technology) ISBN 978-3-901167-14-0 Literaturverz. S. 83 - 100
- [9] Ulrich-Pur F and et al 2021 *Nucl. Instr. and Meth. A* 165570 ISSN 0168-9002