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Monolithic CMOS Sensors for high energy physics — Challenges and perspectives

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ABSTRACT

CMOS cameras revolutionized the visible imaging world, and now also move into other fields. After years of intensive research with significant progress and introduction in a few experiments, monolithic active pixel sensors integrating sensor matrix and readout in one piece of silicon are considered for wider application in high energy physics. Detailed requirements and implementation of CMOS sensors in high energy physics differ from those for visible light. This paper tries to give an overview.

1. Requirements of CMOS sensors for High Energy Physics

CMOS monolithic active pixel sensors (MAPS) revolutionized visible imaging with several Mpixels, even in mobile phones, reaching sub-electron noise. Hybrid pixel sensors with sensor and readout fabricated on separate wafers are still in the majority in installed pixel detector systems in high energy physics experiments (HEP) today. Monolithic pixel sensors integrating sensor and readout on the same silicon substrate are now used in some experiments. They are likely to be adopted more widely as they offer lower material budget, easier assembly and lower cost as they avoid the assembly between sensor and readout. Stitching enabling wafer scale integration and 3D wafer stacking [1] open new perspectives for detector construction further discussed below. This section gives an overview of the requirements of CMOS MAPS for high energy physics (HEP), and the main differences with CMOS cameras for visible light.

Fig. 1 [2] indicates that commercial CMOS imaging technology nodes for visible light are approximately 10 years behind most advanced CMOS technologies (e.g. DRAMs). Pixel pitches of imaging sensors are typically about a factor 20 larger than the minimum line width of the technology with only very few (1–4) transistors per pixel. Pixels in CMOS sensors for HEP usually contain several hundred transistors for a pixel pitch about 200 times larger than the minimum line width of the technology. This is because they need to satisfy the following requirements:

- Single particle hits need to be detected rather than continuously collecting the signals in visible imaging. The images are sparse with only 1% or (much) less of the pixels hit per readout frame.
- Time stamping of hits at the Large Hadron Collider (LHC) at CERN usually happens in 25 ns bins corresponding to the bunch-crossing period, but there is a strong interest for time of flight, 4D tracking (space & time) with timing requirements in the tens of picosecond range.
- Particles need to be detected with a position resolution of a few microns.
- Pixels have to be near 100% efficient over their full area, but particle traversals generate signal charge also deep into the silicon under the circuitry from where it still must be collected. Readout circuitry in the pixel is usually (much) more complex and requires full CMOS (PMOS and NMOS) within the pixel.
- Low power consumption is the key for low mass in the detectors of HEP experiments as electric power is provided through cables and removed through cooling. Together with the cables to transmit the data off-detector, these services often dominate the material budget, as well as the tracking performance and the momentum resolution, especially for low momentum particles. In practice this limits power densities to a few hundred mW/cm^2 near the interaction point where particle collisions are intended to take place and a few tens of mW/cm^2 further away, despite enhanced performance and functionality introduced from one generation to the next.
- With increased hit rate densities, and the tendency to read out all the data, required data bandwidths are ever increasing.
- Depending on the type of particles colliding and the collision rates, CMOS MAPS for HEP are often subject to very stringent radiation tolerance requirements, up to or even beyond 10 MGy of ionizing dose and 10^{16-17} 1 MeV neutron equivalent per cm^2 of non-ionizing energy loss for the most aggressive applications, see Table 1. Submicron CMOS technologies proved to be extremely radiation tolerant with special design techniques [3], and are widely used for circuits in the present Large Hadron Collider

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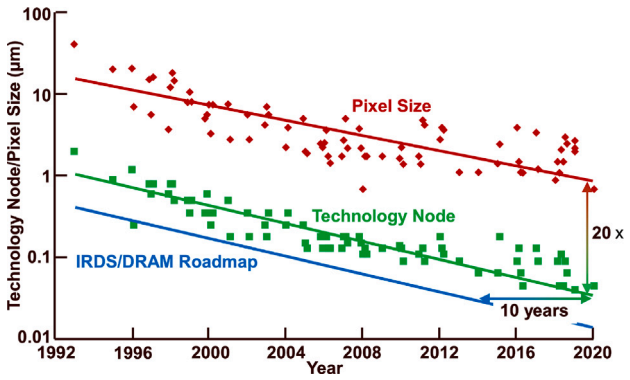

Fig. 1. Pixel size and line width of CMOS imaging technologies and DRAM technologies. Pixel imaging technologies are about 10 years behind DRAM technologies with pixels containing only few transistors at a pitch of about 20 times the minimum technology linewidth [2].
Source: Courtesy A. Theuwissen.

Table 1
Radiation tolerance requirements for CMOS MAPS in HEP, at the ALICE Inner Tracker System (ITS) with proton–proton and heavy ion collisions, at the Large Hadron Collider (LHC), the High-Luminosity LHC (HL-LHC), and at the Future Circular Collider (FCChh) with hadron–hadron collisions. Note that for the FCC colliding electrons and positrons (FCC-ee) the radiation tolerance requirements are much less stringent.

	Dose (MGy)	Fluence (10^{16} 1 MeV n_{eq}/cm^2)
ALICE ITS	0.01	10^{-3}
LHC	1	0.1–0.3
HL-LHC 3 ab^{-1}	5	1.5
FCChh	10–350	3–100

(LHC). Special transistor layouts, used in the beginning to mitigate radiation induced leakage, are often no longer needed in very deep submicron technologies, for instance in [4]. More subtle effects, for instance related to narrow or short channels [5], can still be important, but usually these technologies are extremely tolerant to total ionizing dose due to their very thin dielectrics. Special design techniques now primarily aim to mitigate single event effects, for instance redundancy by triplication and majority voting to reduce or eliminate Single Event Upsets (SEU). Radiation damage due to non-ionizing energy loss (NIEL), primarily a bulk effect, does not significantly affect MOS transistors, generally governed by the silicon–silicon-dioxide interface. However, NIEL can significantly degrade silicon sensors, and its mitigation, discussed below, is very relevant for CMOS sensors in HEP. CMOS transistor and circuit tolerance are treated elsewhere in this special issue.

- One of the main motivations for MAPS in HEP is the reduced cost. After the ALICE ITS2 10 m^2 tracker, there is interest to cover even larger areas with MAPS with discussions addressing hundreds or even thousands square meters in calorimeters. To take advantage of volume production also very versatile sensors, programmable for different applications, are considered [6].

2. Early developments

The first success of silicon sensors with strip detectors and corresponding readout circuitry, for instance with the amplex [7] and microplex [8] chips, is at the origin of the interest in pixel sensors for HEP. At the time silicon sensors were manufactured on high resistivity float-zone silicon, more expensive than Czochralski material, with much higher minority-carrier lifetimes and resistivities allowing depletion layers of several hundred micron thick with low leakage currents. Several developments started on hybrid pixels, at CERN with the RD19 project [9,10], but also elsewhere, for instance [11], and also on monolithic sensors, discussed further below.

2.1. Depleted field effect transistor

Sometimes non-conventional devices were considered. A successful example is the Depleted Field Effect Transistor or DEPFET [12], where signal charge is guided towards a potential well directly under the channel of a MOS transistor of which it affects the conduction. The low capacitance of the potential well results in very high signal-to-noise ratios [13]: 120 to 1 for a 32 μm × 24 μm pixel and 200 to 1 for a 20 μm by 20 μm pixel. This resulted in a position resolution of respectively 1.6 μm in X and 1.2 μm in Y for the larger pitch and 1 μm for the smallest pixel pitch in a 120 GeV pion beam. Pursued by the Max Planck Semiconductor Laboratory in Munich and collaborating institutes for a long time, the CMOS readout was implemented on a separate chip, and adopted much later for the vertex detector of the BELLE experiment at KEK, the Japanese High Energy Accelerator Research Organization [14].

2.2. Charge coupled devices

After their invention by W. Boyle and G. Smith at Bell labs about 50 years ago [17], Charge Coupled Devices or CCDs have been widely used as imaging devices, but CMOS active pixel sensors now dominate [18]. Chris Damerell and co-workers started investigating CCDs for tracking purposes in HEP early on [19], measuring a position resolution of about 5 μm at full efficiency in 1983. A few years later 2 planes in the ACCMOR spectrometer at the Super Proton Synchrotron (SPS) at CERN demonstrated the capability of CCDs to help observe short-lived particles. This finally led to the development and installation in the SLD detector at SLAC of VXD2 (see Fig. 2a), a 120 Mpixel vertex detector composed of 480 CCDs, each with about 400 × 600 pixels on a 22 μm pitch [15]. Large area stitched CCD's (see Fig. 2b), each with 3.2 million pixels on a 20 μm pitch, were used to upgrade to VXD3 [16] and provide a breakthrough in terms of sensitivity to short-lived particles decaying inside the beam pipe. Power consumption per pixel was only 100 nW with a 160 ms readout time for the full detector. These long readout times imposed by the charge transfer inside the CCD sensor disfavors its use for higher interaction rates, and contributed to the emergence of MAPS with more in-pixel circuitry.

CCDs also have been applied in precise timing applications and extreme frame rates as a serial signal buffer written at very high speed to store the signal as a function of time at high rate during the acquisition, followed by the readout at a lower rate [20]. With this technique the authors have been capable of capturing light in flight [21].

2.3. Integration of MOS transistors with sensors on high resistivity wafers

MOS transistors are typically fabricated on Czochralski material with a <100> crystal orientation to minimize interface states at the silicon–silicon-oxide interface. Silicon sensors traditionally use high-resistivity float-zone <111> wafers. Regardless of the orientation, float-zone wafers are much more fragile due to the reduced presence of impurities which otherwise pin the dislocations in the crystal and decrease the risk of wafer breakage. To this day many silicon foundries are reluctant to adapt standard processing steps to reduce thermal and mechanical shocks and stresses necessary to process float-zone wafers. In addition, high temperature process steps can introduce impurities and defects and degrade these wafers decreasing minority carrier lifetime and increasing leakage current. Sensor fabrication processes limited the processing temperature after the initial oxidation, as for instance the Kemmer process [22,23] (600 °C or below), and yielded high sheet resistance of the implanted layers.

The 9 mask HRCMOS process at IMEC integrated transistors and detecting diodes on high-resistivity float-zone silicon [24]. It minimized the thermal budget and avoided plasma etching and the usage of

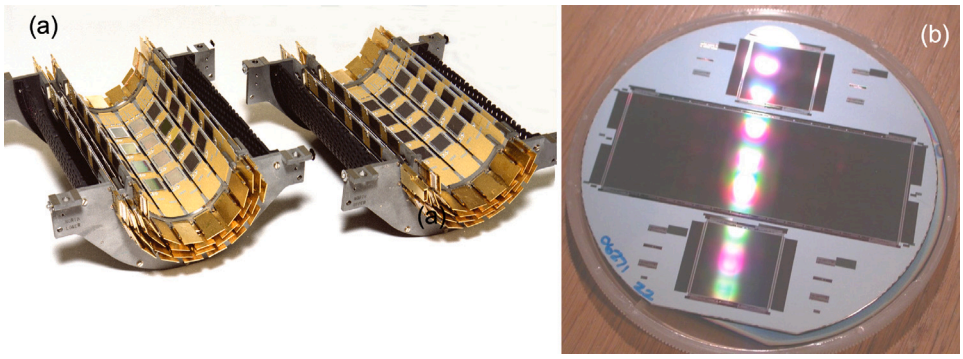

Fig. 2. (a) Picture of the VXD2 upper and lower barrel [15] about 100 mm long with an inner radius of 29.5 mm with 480 CCDs for a total of 120 Mpixels. (b) Photograph of a wafer with a large stitched CCD on the 100 mm wafer with 3.2 million pixels on a 20 μm pitch, used for the upgrade to the VXD3 [16].
Source: Courtesy C. Damerell.

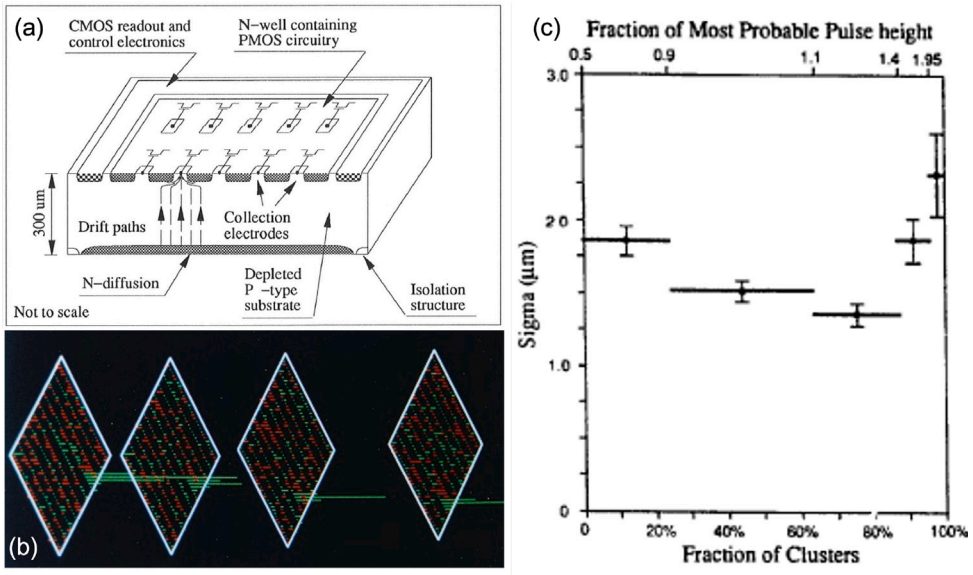

Fig. 3. (a) Schematic overview of the sensor developed in [26,27], see text, (b) event display of a particle traversal through a 4 plane telescope in a high-momentum muon beam, illustrating that charge is always shared in the direction of smallest pixel pitch, (c) position resolution as a function of the signal size, the fraction of the total number of clusters within a certain signal range is indicated with the horizontal bars.

stress-inducing layers. The p-well implant and subsequent long, high-temperature drive-in were replaced by a high energy (700 keV) implant and short anneal. The traditional field oxidation with nitride mask was substituted with an oxide deposition at low temperature and subsequent etching of the active regions. Minority carrier generation lifetimes were measured in excess of 20 ms.

A gettering technique introduced at Lawrence Berkeley Laboratory [25] opened the way to higher temperature processing for more traditional MOS transistor fabrication. Similarly effective for <100> and <111> material, it evacuates harmful impurities from the silicon bulk and traps them near the wafer's back side where they cannot become electrically active. MOS transistors were directly implemented in the high resistivity material.

A collaboration between Stanford University and the University of Hawaii, used a similar gettering technique in combination with a 16 h, 1150 °C well drive-in [26,27]. Fig. 3a shows a schematic drawing of the sensor containing a matrix of 10 by 30 pixels, each 125 μm by 34 μm. On the front side of a 300 μm thick high resistivity p-type (12 kOhm.cm) wafer, an array of p-type collection electrodes contact the substrate through holes in an n-well which contains the readout circuitry. The full substrate is depleted by reverse bias on a planar junction on the back side of the wafer. Separating this junction from the collection electrode allowed this full depletion, but created a low lateral field near the pixel edges. This enhanced charge sharing eliminated single pixel clusters for minimum ionizing particles as illustrated in Fig. 3b, and yielded a 2 μm position resolution in the direction of the smallest pixel pitch (34 μm). Fig. 3c illustrates a position resolution better than 2 μm for signals around the most probable value, degrading at lower signals due to the reduced signal to noise, and at higher signals as delta electrons generate charge away from the particle traversal. Both sides of the wafer required processing, typically not compatible with standard foundry CMOS processes. A trench etch reduced the processing on the back side of the wafer to a single masking step [28], and triggered the idea of 3D silicon sensors [29].

Separating the junction from the collection electrode was also done in the ARCADIA project [30,31], in CCDs [20], and also by growing an epitaxial layer of opposite type as the substrate [32], and in the TowerJazz 180 nm and TPSCo 65 nm with a low dose deep implant, see below, to mitigate the low lateral field and obtain better NIEL sensor tolerance.

A pixel sensor with a 13.75 μm pixel pitch In [33,34] reached a position resolution of about 1 μm with analog interpolation. Larger reverse bias extended depletion, increased signal-to-noise ratio and enhanced charge sharing due to the increase in signal from the extended depletion. Capacitive coupling further enhanced charge sharing so that also there practically no single pixel clusters were observed. A pixel

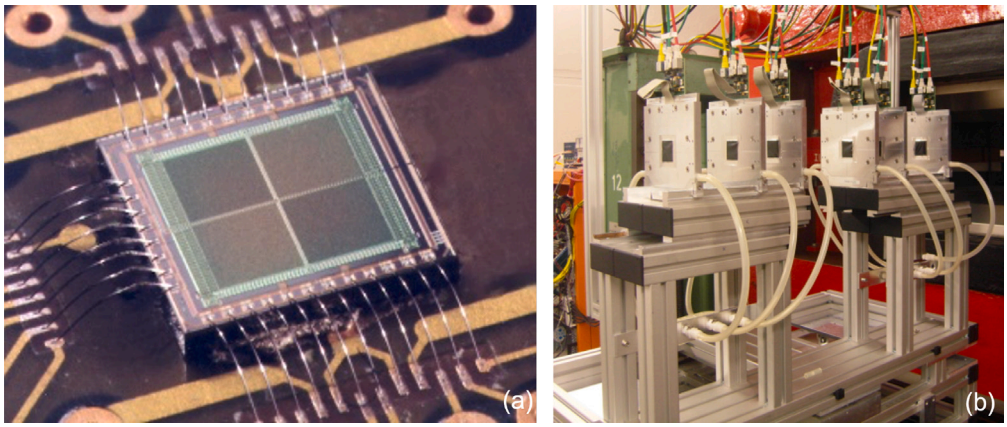

Fig. 4. (a) Photograph of MIMOSA 1 [36], the first MAPS for HEP in a standard technology, (b) photograph of the EUDET telescope using the MIMOSA26 [37]. *Source:* Courtesy IPHC.

Table 2
Overview of some of the chips developed by IPHC.
Source: Courtesy IPHC.

Sensors	Year	Tech	Metal layer	Epi μm	Matrix	Pixel pitch μm	Chip size mm^2	Output	Purpose
Mimosa 1	1999	AMS 0.6	3M	14	16k pixels 4 × 64 × 64 3T pixel	20	3.75 × 4.06	4 analog 10 MHz	Proof of concept prototype
Mimosa 5	2001 2003	AMS 0.6	3M	14	1M pixels 4 × 512 × 512 3T pixel	17	19.4 × 17.4	4 analog 10 MHz	1st reticle prototype sensor
Mimosa 20	2006 2007 2008	AMS 0.35	4M	14 & 20	204k pixels 2 × 320 × 320	30	10.5 × 19.25	2 analog	STAR PXL half reticle prototype
Mimosa 26	2008 2009	AMS 0.35	4M	14 & 10-15-20 high res	660k pixels 1152 × 512	18.4	13.7 × 21.5	digital zero supp	EUDET telescope sensors
Mimosa 28 ULTIMATE 1 & 2	2010 2012	AMS 0.35	4M	14 & 10-15-20 high res	890k pixels 960 × 928	20.7	20.2 × 22.7	digital zero supp	STAR PXL final sensors
Monolithic Imager 2 versions	2020 2021	Tower 0.18	6M	18-25-50 high resist.	125k pixels 256 × 512	20	6.2 × 10.6	analog	Soft X Ray applic.
Mimosis 1&2	2020 2023	Tower 0.18	6M	18-25-50 high resist.	500k pixels 504 × 1024	26.88 & 30.24	17.2 × 31	digital	CBM MVD prototype sensors

sensor with 8 μm pixel pitch achieved a sub-micron point resolution of 0.59–0.83 μm by significant charge sharing and a very large 340 to 1 signal-to-single-channel-noise ratio for a 400 μm thick depletion layer [35]. These examples illustrate how a large signal-to-noise ratio contributes to an excellent position resolution.

2.4. Evolution to standard processes

Gradually the focus shifted towards standard CMOS technologies as starting materials more compatible with particle detection became available due to a demand for other applications, for instance for RF to minimize losses. A first sensor for HEP in a standard technology, the MIMOSA or Minimum Ionizing particle MOS Active pixel Sensor was developed by IPHC in a 0.6 μm technology [36], see Fig. 4a. The pixel matrix itself with a 20 μm pitch contained only NMOS transistors, a few per pixel, for a rolling shutter readout at maximum 10 MHz. This was the first of a series of many chips designed at IPHC, Table 2 gives an overview. The MIMOSA26 [37] is used to this day in the EUDET reference telescope in test beams to characterize the performance of new sensor prototypes, see Fig. 4b. The MIMOSA28, alias the ULTIMATE chip [38], with rolling shutter and an integration time of 185.6 μs, was used for the vertex detector of the STAR experiment, see below. AC coupling and reverse biasing of the sensor from the front side was also introduced on some sensors [39,40]. Sensor capacitance increases due to the parasitics related to the AC coupling, but the circuit design greatly simplifies without reverse substrate bias. The MIMOSIS sensor chip [41], derived from the ALPIDE chip, see below, is a further development for the Compressed Baryonic Matter (CBM) experiment at GSI.

2.5. The InMAPS process and full CMOS circuitry in the pixel

A further important step forward, achieved by the Rutherford Appleton Laboratory (RAL) in collaboration with TowerJazz semiconductor, was the integration of full CMOS circuitry in the pixel, essential for more advanced readout schemes, while maintaining a 100% fill factor or full detection efficiency over the whole pixel area. The inMAPS process [42] provides a deep p-well, in addition to a p-well, n-well and deep n-well (see Fig. 5). In the pixel matrix this deep p-well shields in-pixel n-wells containing PMOS transistors from the epitaxial layer, preventing them from collecting any signal charge generated in the p-type epitaxial layer. It also provides better shielding of the

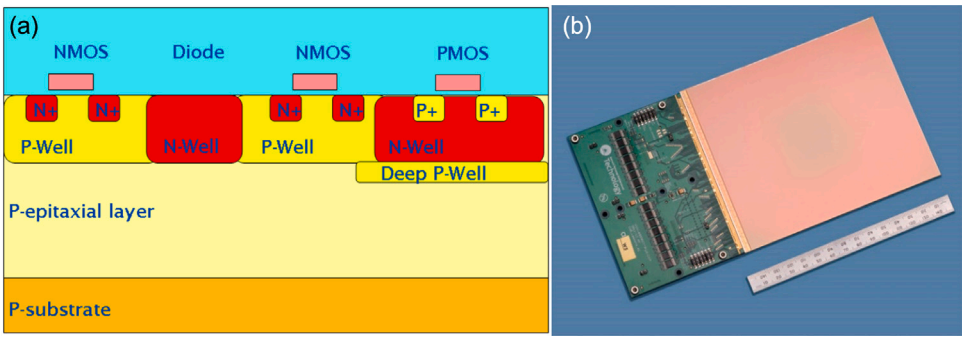

Fig. 5. (a) Schematic cross-section of the INMAPS process [38][38] with an additional deep p-well implant in the pixel to prevent the n-wells with PMOS transistors from collecting signal charge so that only the n-well collection electrode collects the signal charge, and (b) real die photograph of the stitched wafer-scale LASSENA sensor just barely fitting in a 200 mm wafer.
Source: Courtesy STFC.

epitaxial layer from transient signals in the circuitry. This process was extensively used by the RAL group for a number of prototypes listed hereafter, the pixel size in μm being indicated between brackets: TPAC developed for ILC ECAL (50) [43], DECAL a chip for calorimetry (50) [44], PIMMS for Time of Flight mass spectroscopy (70) [45], CHERWELL for tracking and calorimetry (48 × 96) [46], PERCIVAL for soft X-rays [47,48], and LASSENA, a wafer-scale stitched sensor just barely fitting in a 200 mm wafer [49]. Fig. 5 shows a schematic die cross-section representing major features of the process as well as a die photograph of the stitched LASSENA sensor (courtesy STFC).

The inMAPS process was used for many further developments discussed below, including the ALPIDE sensor, the first MAPS sensor with sparse readout similar to hybrid sensors, for RD50 prototypes, for the MALTA and MONOPIX developments for the ATLAS Inner Tracker (ITk) upgrade, as well as for vertexing and tracking devices in experiments envisaged at future electron–positron colliders (The International Linear Collider (ILC), the Compact Linear Collider (CLIC), FCCee, the Circular Electron Positron Collider (CEPC)), and the MIMOSIS mentioned earlier.

2.6. Silicon on insulator

Another approach to integrate readout circuitry with a sensor is to use Silicon on Insulator technology or SOI, where a thin oxide layer separates the layer with transistors and readout circuitry from the high resistivity sensor substrate below, see Fig. 6a. The SOIPIX development in Japan [51], supported by Japan MEXT KAKENHI Grant-in-Aid for Scientific Research on Innovative Areas 25109001, allowed the SOIPIX collaboration to closely work together with a foundry to develop a fully depleted 0.15 μm and 0.2 μm SOI process [52,53]. More than 20 Multi-Project Wafer (MPW) runs were organized for a significant user community targeting a wide variety of different applications, not counting the user specific runs. This led to a very productive development of sensor prototypes, circuits and sensor device structures, as for instance the SOIPIX-PDD, a pinned depleted diode structure [54], as well as work on steep-slope transistors [55] (see Fig. 6b), and also the monolithic sensor with submicron position resolution already mentioned [35]. A weak point is the relatively low tolerance to ionizing radiation due to the buried oxide layer being prone to accumulate charge under irradiation. Mitigation techniques including a double buried oxide with a thin silicon layer in between acting as a shield between the sensor and the transistors brought some improvement [50], see Fig. 6c.

2.7. Wafer stacking

Monolithic sensors normally integrate the sensor and the readout electronics on a single wafer. The demand for more functionality in the pixel pushes to smaller line width technologies to maintain an acceptable pixel size, but the cost of very small line width technologies significantly increases. A possible alternative is wafer stacking to assemble the monolithic sensor wafer including some electronics and an additional wafer with the rest of the electronics. This is technologically challenging, but also in terms of design and verification, especially with wafers from different sources, as then design kits are not set up to include the connections between the parts of the circuit on other wafers. An early development at Fermilab [56] faced significant technological challenges with different vendors, but in the end functional devices were produced [57].

Also the commercial CMOS imaging industry pursued wafer stacking as an interesting alternative to finer linewidth technology, stacking even more than two wafers [1]. Foundries now offer wafer stacking in house, delivering fully finished assemblies to the customer. This actually makes the distinction between hybrid and monolithic less clear, but represents an opportunity for further integration also for our community.

3. MAPS installed in HEP experiments

3.1. First application of MAPS in HEP in the STAR experiment

Most installed pixel tracking systems in HEP are still based on hybrid sensors. The STAR experiment at Brookhaven National Laboratory was the first to implement a MAPS based upgrade of its vertex tracker [58], see Fig. 7, motivated by a lower material budget. It consisted of two cylindrical layers at 2.8 cm and 8 cm radius. A value of 0.39% of a radiation length (X_0) was achieved for the innermost layer, based on 50 μm thin sensors mounted on a two layer kapton flex with aluminum traces. The ULTIMATE chip [38] was already discussed under 2.4. The absence of reverse bias yields a moderate NIEL tolerance of several 10^{12} 1 MeV n_{eq}/cm^2 at room temperature. The ULTIMATE chip was designed in 2011, the full detector was completed and installed in 2014, and operated for physics runs until 2016.

3.2. The ALICE Inner Tracking System 2

For its upgrade of the Inner Tracking System (ITS), the ALICE experiment installed a new tracker [59] consisting of 7 barrel layers fully constructed with MAPS, covering a 10 m^2 area with about 12.5 billion pixels. It is a significant improvement over its first version, based on hybrid pixel sensors. In particular, the material budget of the inner layers was reduced from 1.14% of a radiation length to 0.3%, the pixel size from 425 × 50 μm^2 to about 27 × 29 μm^2, and the radius of the first layer from 39 to 22 mm. Fig. 8 shows a schematic view of the ITS2 detector, outer half barrels during construction and an event display.

The ALPIDE sensor [60,61] developed in the INMAPS process for ITS2, contains full CMOS readout circuitry in the pixel, a pixel front

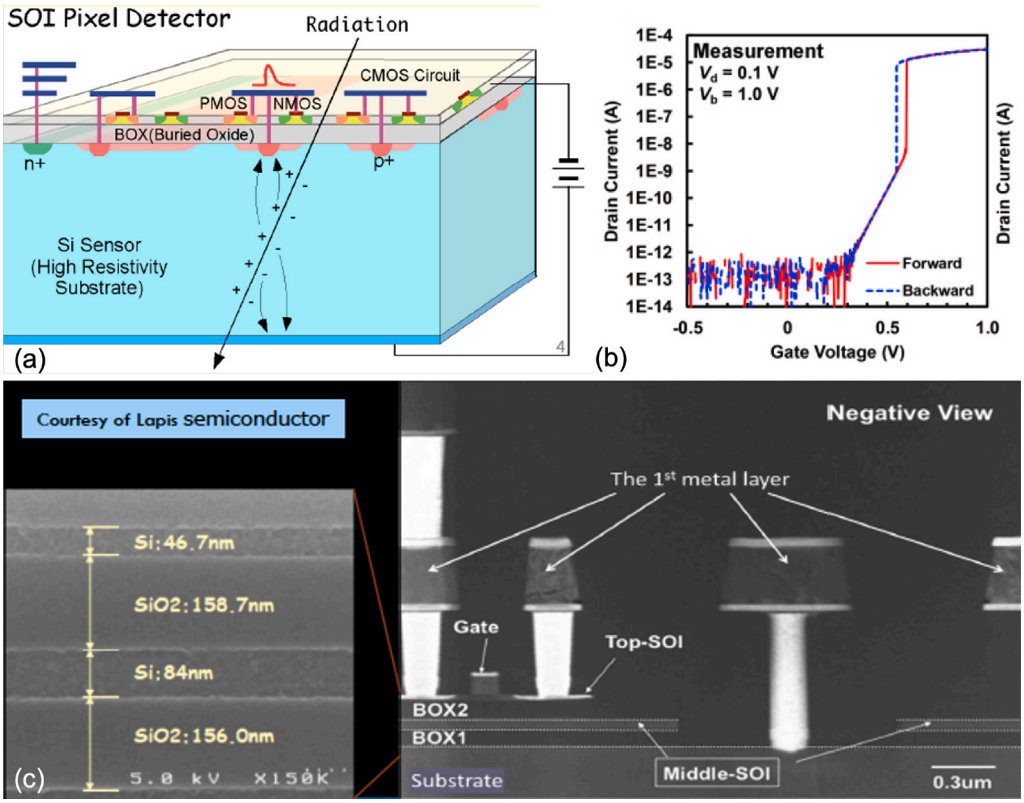

Fig. 6. The SOIPIX development in Japan: (a) Schematic cross-section of the Silicon-on-Insulator sensor illustrating the buried oxide layer separating the thin silicon layer containing the circuitry and the high resistivity substrate, (b) the drain current vs gate voltage of a steep-slope transistor, and (c) cross-section of the double SOI structure developed to mitigate the lower tolerance to ionizing radiation [50].
Source: Courtesy Y. Arai.

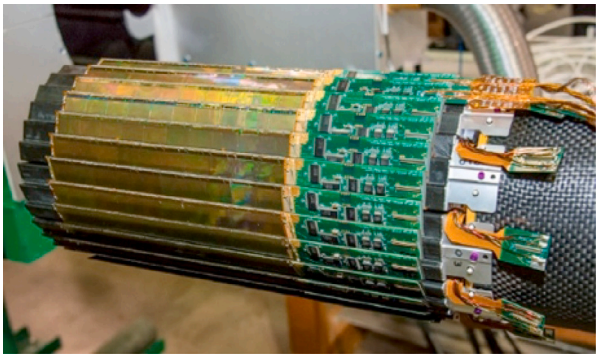

Fig. 7. Photograph of the vertex detector of the STAR experiment [58], the first to use CMOS MAPS.
Source: Courtesy G. Contin.

end (amplifier and discriminator) and a sparse readout similar to hybrid pixel detectors. The low capacitance of the small collection electrode (about 2x2 μm^2) helped reducing the front end power to 40 nW [62], combined with a zero suppressed readout for low overall power consumption. Outside of the pixel matrix, the deep n-well provides the possibility of a standard triple well structure. The ALPIDE measures 15×30 mm^2 and contains a 512×1024 pixel matrix. The matrix power density is only about 5 to 6 mW/cm^2, dominated by the consumption of the analog front end. The periphery consumes significantly more than the matrix in the inner layers of the experiment due to the digital logic and especially the data transmitter unit with PLL, serializer and output driver. The latter takes about half the power consumption of the chip bringing the total power density in the worst case to about 30–40 mW/cm^2. The ALPIDE chip is also used in the Muon Forward Tracker in ALICE [63], and foreseen to be used in the Focal, a forward calorimeter [64] also in ALICE.

The success of the ALPIDE and the ITS2 raised interest by several other HEP experiments. The ALICE vertex detector itself is also planned to undergo an upgrade with the ITS3 [65,66], aimed to further reduce material budget by replacing the 3 inner layers with wafer-scale stitched MAPS sensors, thinned to a few tens of microns to make them flexible and bend them around the beam pipe. Bent sensors perform equally well before and after bending [67]. Significant progress has also been made towards the assembly of such a detector, Fig. 8d shows a mounting exercise with bare wafers thinned down to 50 μm. Challenges for such large stitched sensors will be discussed further below, but these developments open perspectives for totally new detector geometries.

4. Sensor optimization for extreme radiation tolerance

CMOS circuitry in MAPS follows the general trend of deep submicron CMOS technologies towards extreme tolerance to ionizing radiation, but traditional MAPS collect charge primarily by diffusion, and often already show significant performance degradation after NIEL fluences of 10^{12}–10^{13} 1 MeV n_{eq}/cm^2. MAPS devices with a higher radiation tolerance have been developed with a higher resistivity epitaxial layer for which the drift component in the charge collection is more important [38]. However, the most extreme environments of HEP impose a sufficiently high electric field to further accelerate the signal charge collection from the sensitive layer to minimize the probability for it to be captured by radiation-induced traps. Two main approaches have been used, either with a large collection electrode in which the readout is placed (Fig. 9a) [68], or with a small collection electrode (Fig. 9b) surrounded by a well containing the readout circuitry. The latter offers a significantly smaller sensor capacitance but needs specific

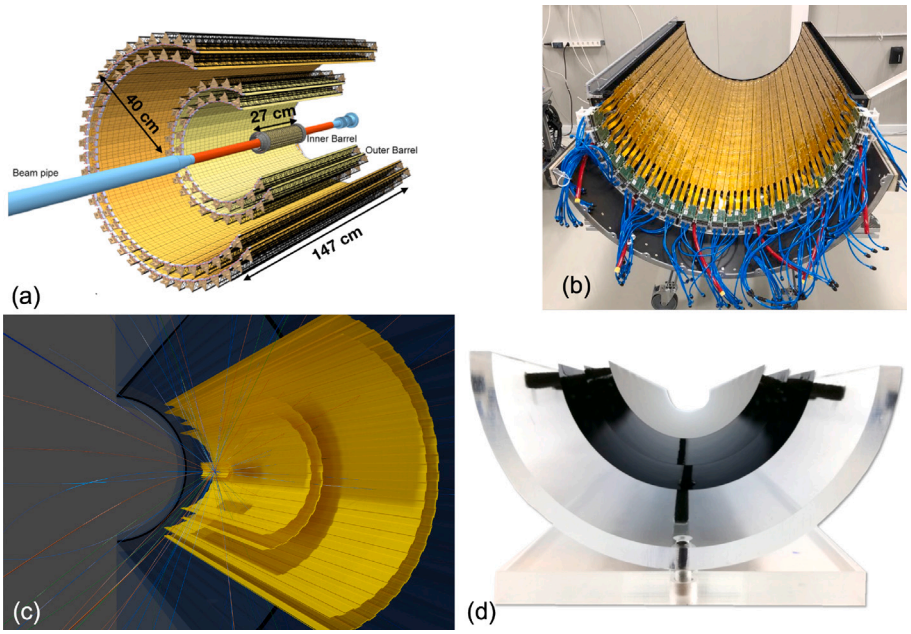

Fig. 8. (a) A schematic view of the ITS2 detector [59,60] with about 12.5 Gpixels over about 10 m^2, (b) outer half-barrels during construction, covering about 2 m^2, and (c) event display showing half of the ITS2 detector: all seven layers are clearly visible, the three inner layers are to be replaced for the ITS3 upgrade. (d) shows a mounting exercise for the ITS3 with bare wafers thinned to 50 μm.

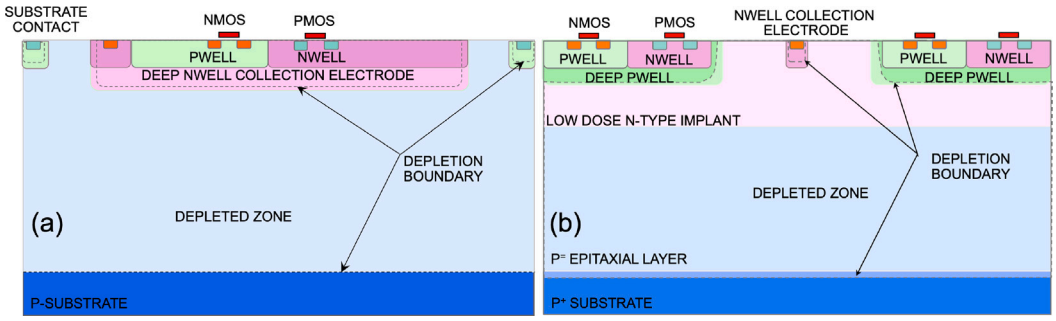

Fig. 9. Schematic view of two different sensor designs for increased radiation tolerance: (a) a large collection electrode with circuitry embedded and (b) a small collection electrode surrounded by wells containing the readout circuitry. The low dose n-type implant is added to move the junction away from the collection electrode and allow full depletion of both the very lowly doped P-type epitaxial layer (P^-) and the n-type implanted region.

optimization of the sensor to deplete the sensitive layer and accelerate charge collection.

4.1. Large collection electrode

A large collection electrode and significant reverse bias yields a large and uniform electric field to collect the signal charge, naturally resulting in significant NIEL tolerance. This was demonstrated on several different technologies, in particular by groups interested in MAPS for the outer pixel layer of the Inner Tracker (ITk) for the ATLAS High-Luminosity LHC upgrade. One example is the development of MuPIX [69,70] and ATLASPIX [71,72]. Fig. 10 shows a prototype of the vertex detector for the Mu3e experiment [70], and an earlier measurement showing NIEL tolerance to 2×10^{15} 1 MeV n_{eq}/cm^2. The ATLASPIX3 sensor chip [71] measures 20.2 × 21 mm^2 and contains 132 × 372 pixels of 150 by 50 μm^2. It is implemented in a 180 nm CMOS technology on a 200–400 Ohm cm substrate instead of the standard starting material.

A similar development, based on the LFoundry 150 nm CMOS process and addressing the LF-MONOPIX chip, which features 50 × 150 μm^2 pixels, lead to comparable radiation performance [73], see Fig. 11. Also the RD50 collaboration developed a pixel sensor prototype in the same technology [74].

4.2. Small collection electrode

As a first step towards better radiation tolerance, the 180 nm TowerJazz process was modified in a side development of the ALPIDE sensor [75]. An additional deep blanket low doped implant over the full pixel area (see Fig. 9b) created a planar junction of the sensor separated from the collection electrode and achieved full depletion of the epitaxial layer, and signal charge collection by drift. As this implant is the only difference in the layout, otherwise identical designs processed in the standard and the modified process could be compared in one of the early ALPIDE prototype mask sets. The process modification improved the tolerance to NIEL from 10^{13} 1 MeV n_{eq}/cm^2 by an order of magnitude. This triggered a development in this modified technology for the outer pixel layer in the ITk upgrade ATLAS, supported through the STREAM project. The development encompassed the design of two pixel sensors, the MALTA [76] and TJ MONOPIX [77], with similar pixel sensor layout but different readout architectures.

A first iteration showed efficiency losses at the pixel edges for fluences of 5×10^{14} 1 MeV n_{eq}/cm^2 or beyond due to a too small electric field and too slow charge collection [79]. Further process or sensor modifications [78] accelerated the charge collection by an order magnitude, either by introducing a gap in the low dose n-type implant, see Fig. 12a, or an additional deep p-well implant at the pixel

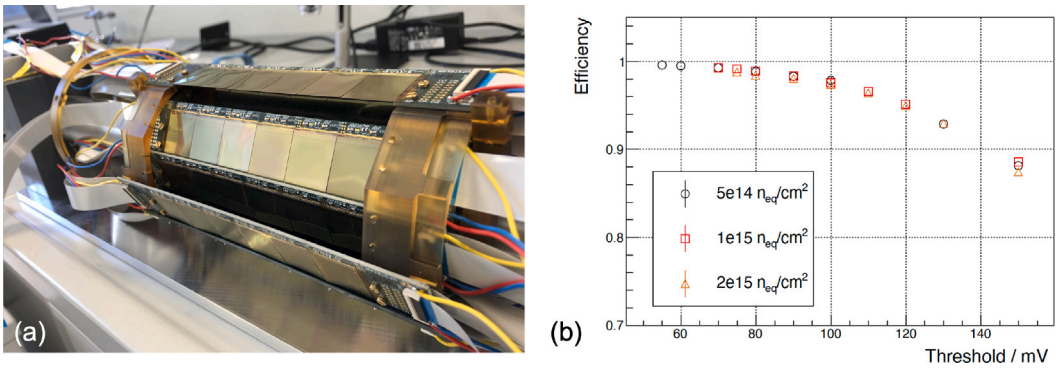

Fig. 10. (a) A photograph of a MuPix vertex detector prototype under test with cosmic rays. (b) an early detection efficiency measurement demonstrating NIEL tolerance up to 2×10^{15} 1 MeV n_{eq}/cm^2 [69].
Source: Courtesy A. Schöning and I. Peric.

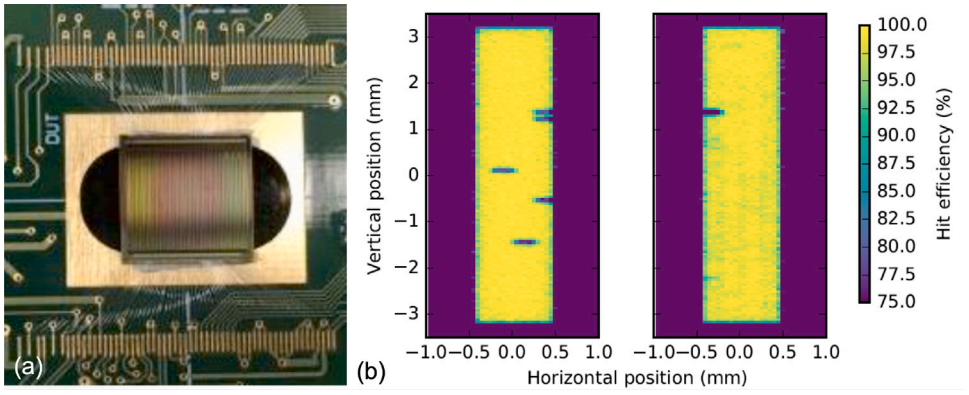

Fig. 11. (a) Photograph of the LF-MONOPIX prototype mounted on its carrier board and (b) its measured detection efficiency, 99.6% pre-rad, and 98.6% after 1.14×10^{15} 1 MeV n_{eq}/cm^2 [73].
Source: Courtesy N. Wermes.

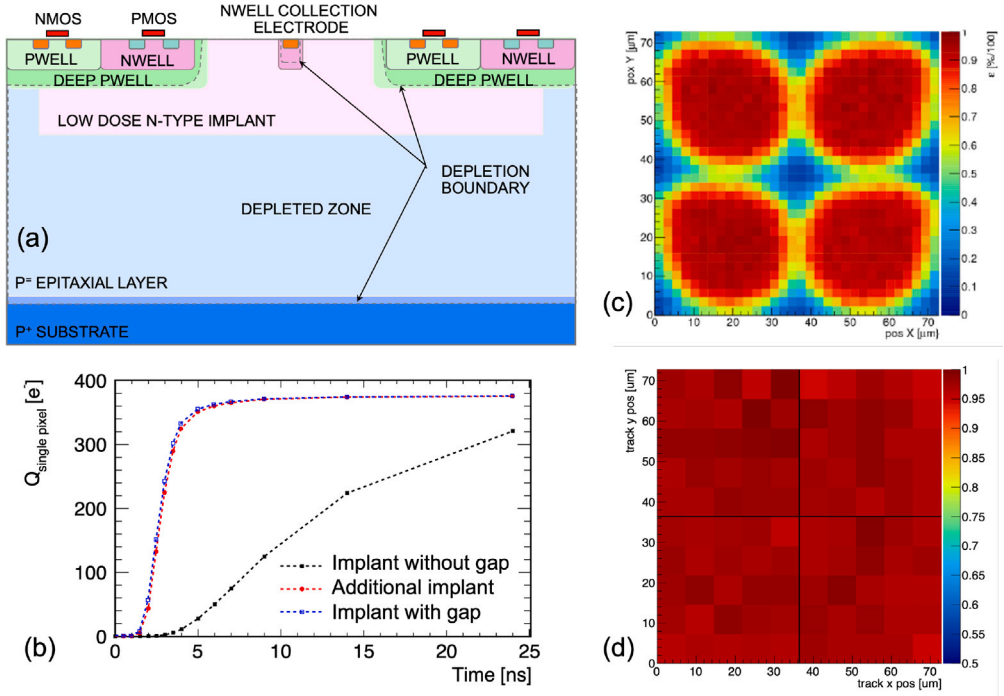

Fig. 12. (a) Schematic cross-section of a pixel showing a gap in the low dose n-type implant to further increase the lateral electric field near the pixel edges and accelerate the signal charge collection by an order of magnitude. (b) compares the collected signal as a function of time for the different pixel designs and illustrates the acceleration [78]. The in-pixel efficiency over a 4 pixel map after a 10^{15} 1 MeV n_{eq}/cm^2 irradiation is plotted in (c) before the improvement [79], and in (d) after the improvement [80].

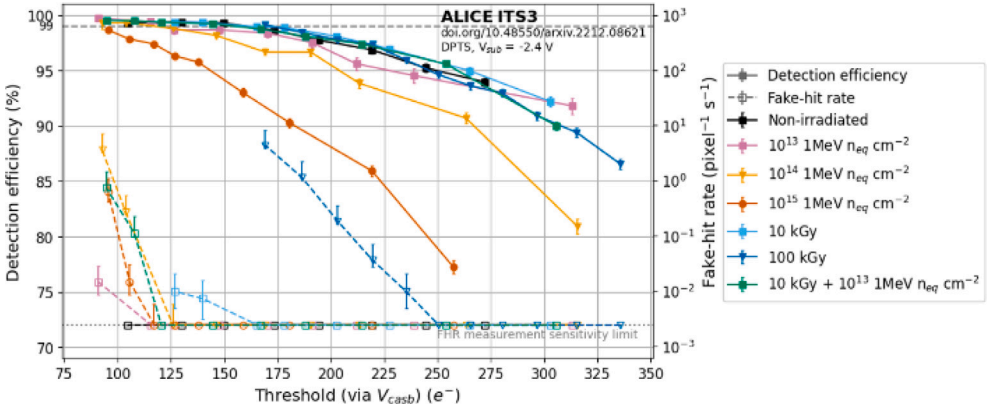

Fig. 13. Detection efficiency of the Digital Pixel Test Structure or DPTS [88] measured at room temperature, unirradiated and irradiated both with ionizing and non-ionizing radiation at different levels [89].

edges. The acceleration is illustrated in Fig. 12b, comparing the charge collected by each of the four pixels as a function of time for a minimum ionizing particle perpendicularly incident exactly in the corner shared by the four pixels. Together with an additional improvement from a higher gain and better uniformity of the pixel front end allowing lower charge thresholds [81], this acceleration was sufficient to fix or at least significantly improve the inefficiencies for fluences up to 10^{15} 1 MeV n_{eq}/cm^2 [80]. Fig. 12c [79] shows the 4 pixel efficiency map after irradiation without the gap in the implant, and Fig. 12d [80] with the implant. Further work with high resistivity Czochralski (Cz) wafers instead of the standard epitaxial material to obtain larger signals reached tolerance up to a few 10^{15} n_{eq}/cm^2 cooled at −20 ° C [82–84]. The modifications discussed here also improve sensor performance and operating margin before irradiation by concentrating more charge on a single pixel, experimentally confirmed also in [85].

After the 180 nm process, CERN in collaboration with several other institutes [86] started MAPS development in sub−100 nm technologies, offering better density and performance, and access to large, stitched sensors on 300 mm wafers, started at CERN in collaboration with several other institutes. A first technology identified was the TPSCo 65 nm ISC imaging CMOS technology. A first run was completed in synergy with the ALICE experiment and its ITS3 upgrade. It combined process modifications and pixel designs based on general principles already explored in the 180 nm technology, allowing the TPSCo 65 nm ISC technology to be qualified for HEP [87]:

The digital pixel test structure (DPTS) [88] contains a 32 × 32 pixel matrix on a 15 μm pitch and measures 1.5 mm by 1.5 mm with the full chain of sensor with process and pixel design modifications, front end and digital readout circuitry. The chip proved fully efficient in a particle beam before and after 10^{15} n_{eq}/cm^2 at room temperature [89], as illustrated in Fig. 13. Higher fluences are also under study, probably requiring cooling for good performance. Non-ionizing energy loss does not only cause trapping of the signal charge, but also an increase in sensor leakage current [90], and changes of the effective doping level [91]. Some signs of changes in effective doping level are also observed in this 65 nm process at high fluences through a decrease in the capacitance of the collection electrode. So far, increasing the collection field for faster charge collection was sufficient, but higher fluences may require a doping increase to reduce the relative impact of effective doping changes, or a reduction of the travel distance of the charge. Both push to a smaller detection volume per pixel and hence a reduction of the radiation induced leakage current. AC coupling would allow higher sensor biases and a higher electric field, to be traded off with the extra parasitic capacitance.

Transistor [92] and other measurements, for instance [93], established that circuits tolerant to a total ionizing dose up to several MGy can be designed in this 65 nm process. A second submission December 2022 explores stitching to construct chips larger than a reticle with two stitched chips of about 25.9 cm long but it also contains several smaller test chips.

MAPS do not necessarily require dedicated imaging technologies, but this section illustrates that some flexibility on the foundry side is desirable to enhance sensor performance.

5. Sensor optimization for precision timing

Precision timing and 4D tracking receive significant interest [94]. Monolithic CMOS sensor developments for HEP are generally still at an early stage in this area, often focusing on the sensor optimization itself. Significant challenges remain to conserve timing performance in larger circuits or systems.

A large collection electrode occupying most of the pixel area provides a large and uniform electric field and therefore a fast and uniform sensor time response. The CACTUS development [95], an evolution of LF-MONOPIX [73], is an example exploiting this. Another example is a development in SiGe BiCMOS technologies [96]. The SiGe Heterojunction Bipolar Transistors (HBTs) offer cut-off frequencies otherwise only reached in more expensive smaller linewidth CMOS technologies. Hexagonal pixels in the last iterations [97,98], see Fig. 14, reduce charge sharing to maximum three pixels providing on average a larger signal on a single pixel improving time resolution. With an additional gain layer 20 ps time resolution was reached [99]. Circuits covering larger areas are now in design.

Precision timing was also investigated in the TowerJazz 180 nm process with similar modifications as described earlier [100]. The small collection electrode offers a small capacitance but with a much less uniform electric field. A hexagonal pixel layout not only reduces charge sharing to a maximum of three pixels, but minimizes the largest distance the signal charge has to travel from the pixel edge to the collection electrode in the center. About 100 ps timing resolution was reached at full efficiency for a 20 μm pitch after applying timewalk and cluster size correction [101].

6. Future challenges: power density and stitching

A full breakthrough of MAPS covering large areas to systematically replace more traditional tracking detectors or calorimeters, requires further progress on power density and stitching at competitive cost. Power density significantly impacts material budget in trackers, and cannot increase as it would offset the initial position resolution advantage. More efficient assembly of larger areas in terms of both time and cost will be required for the HEP community to afford MAPS for trackers or other detectors of 100 m^2 or more. These challenges are discussed further below.

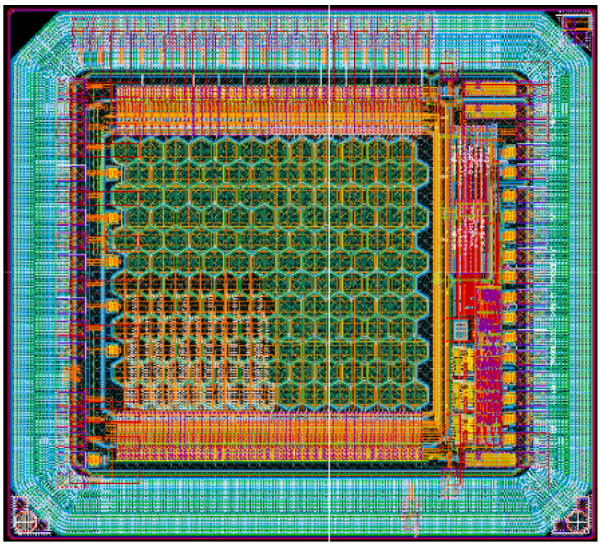

Fig. 14. Layout of a monolithic pixel prototype implemented in a 130 nm SiGe BiCMOS technology [98]. The hexagonal pixel layout is clearly visible.
Source: Courtesy G. Iacobucci.

6.1. Power density

Power density is important in terms of material budget, but also to reduce power supply drops for larger sensor chips. Additional margin can be gained through serial powering and dedicated regulation, investigated not only for hybrid sensors, but also for MAPS [102] but not yet on a very wide scale. The different contributors to the power consumption are discussed below.

6.2. Analog power consumption

The analog front end, usually continuously active to detect particle hits upon arrival, is often dominant in the power consumption. Under certain assumptions this power consumption is inversely proportional to the ratio of collected charge over capacitance at the front end input (Q/C) to at least a power of two, or even of four in case the input transistor carries a sufficiently low current to be in weak inversion [103]. The Q/C ratio can be seen as the voltage excursion at the input, a measure of the size of the signal driving the front end. It can be compared to the input-referred noise and input-referred channel-to-channel mismatch of the front end to evaluate signal-to-noise and signal-to-mismatch, but it also has a major impact on the power-speed performance.

A small collection electrode can be approximated as a spherical junction or a fraction of it with a capacitance:

$$C_{spherical} = \frac{4\pi\epsilon}{\frac{1}{R_1} - \frac{1}{R_2}} \approx 4\pi\epsilon R_1 \tag{1}$$

R_1 and R_2 are respectively the inner and outer radii of the depletion layer at the junction. For R_1 significantly smaller than R_2, the expression simplifies to the capacitance being proportional to R_1, essentially to the size of the undepleted part of the collection electrode. For a 1 μm radius this yields about 1 fF, to which in practice the capacitance of the connection to the front end and the input capacitance of the front end itself have to be added. A total of 1 fF would give an excursion of 160 μV/e$^-$. A Q/C of several 100 mV is more or less equivalent to a digital signal, as then the input transistor can be biased in standby at very low current and be 'switched on' by a hit. This would be a game-changer, practically reducing analog power consumption to zero.

Optimizing Q/C in MAPS has received significant attention not only in HEP but also more generally. Several developments reached sub-femtofarad capacitance and sufficient signal-to-noise to clearly distinguish the signal from a single visible photon generating one electron–hole pair. With this the quantized nature of visible light can be demonstrated taking spectra at sufficiently low light conditions. In [104] 220 μV/e$^-$ or an effective capacitance of 0.73 fF was reached for a 0.11 μm technology, and in [105] 350 μV/e$^-$ or an effective capacitance of 0.46 fF was reached for a 45 nm technology. Capacitances mentioned are the effective ones, with some part of the circuit capacitance compensated by the source follower at the input. At present not many developments for HEP have fully exploited the special features of CMOS imaging technologies, like pinned diodes and specifically optimized transistors in the pixel matrix, which would be one path to improve Q/C.

A finer linewidth CMOS technology also reduces capacitance: a simulation analysis [106] of ring oscillators showed that a charge of 2500 electrons flips a standard inverter in a 65 nm technology, reducing to 850 electrons in a 28 nm technology, and to 100 electrons in a 5 nm technology. A charge amplifier topology other than an inverter may be preferable but it illustrates the potential capacitance reduction with decreasing linewidth.

6.3. Digital architecture and power consumption

Power consumption of digital CMOS circuitry is typically activity dominated, although static power consumption from leakage current now becomes more important. Activity in the pixel matrix is normally dominated by the clock distribution and the transmission of the hit related data to the periphery. A minimum energy equal to CV^2 is necessary to toggle a capacitance C from 0 V to the power supply voltage V and back. For a capacitance of 2 pF/cm, a somewhat optimistic estimate for a heavily loaded line, this yields an energy per cm E_{line} of 6.5 pJ/cm for a supply voltage of 1.8 V and 2 pJ/cm in case of 1 V, illustrating the quadratic impact of the supply voltage. These energies are per unit length, the total required energy is therefore proportional to the distance over which the signal has to be transmitted. For a simple line and random encoding, the probability for a transition between levels in between bits is 50%, resulting in an average energy per bit of around 1 pJ/bit/cm at a power supply of 1 V or 1 mW/Gb/s/cm, half the energy per cem E_{line} required to toggle the line. The capacitance of the buffers required to reach 1–2 Gb/s on a single long line is typically negligible. At a hit rate density R (hits/cm^2/s), transferring all hit information along the pixel column down to the periphery, transmitting B bits/hit over on average half the column height H, yields a power density:

$$P_{hit} = \frac{E_{bit} B H R}{2} = \frac{E_{line} B H R}{4} \tag{2}$$

This translates into 5 mW/cm^2 for $E_{bit} = E_{line}/2$ = 1pJ/bit/cm, B = 5 bits/hit, H = 2 cm and for a hit rate R = 1 Ghit/cm^2. A 2 cm high column at 50 μm pitch contains 400 pixels. A fully binary encoding of the address would require B=9 bits, assuming single pixel clusters, but one may use parallel lines corresponding to a smaller address space. The number of bits B per hit should also take the cluster multiplicity into account: if hit information is just transferred per pixel without any correlation to neighboring pixels the number of bits per hit B should be multiplied by the average cluster size. Depending on the way the data is encoded, the data transmission within a pixel matrix may not be a full serial transmission, but rather a set of pulses. In that case one does not have the 50% reduction in the power density:

$$P_{hit} = \frac{E_{line} B H R}{2} \tag{3}$$

meaning 10 mW/cm^2 or 2 mW/cm^2 and 2pJ/pulse for the values considered above. Note that the power density associated with hit rate is proportional to the height H of the matrix, significantly impacting the design of larger area, and especially stitched pixel sensors.

Distributing a clock at frequency f over the matrix with pixel pitch p, reaching all pixels, without clock gating, can be done with a line every two columns and this requires a power density:

$$P_{clock} = \frac{E_{line} f}{2p} \tag{4}$$

meaning 16 mW/cm^2 at a 1 V supply for H = 2 cm, f= 40 MHz and p = 50 μm.

These simple calculations provide some input for architectural choices. One can either transmit hit data to the periphery immediately and carry out the time stamping of the hit there, or one can distribute a clock or a time reference over the matrix, and store hits locally and only transfer hits selected by a trigger. For the above example the power density required to transmit the clock or a time reference to every pixel is 16 mW/cm^2. The power density required to transfer the hit information immediately equals 10 mW/cm^2 for the very high hit rate of 1 Ghit/cm^2/s. Therefore it is still more power efficient under the given assumptions to transfer the hit data to the periphery immediately. In general time stamping and selecting hits prior to transmission of hit data to the periphery is advantageous for very high hit rates, otherwise it is better to immediately transmit hit information to the periphery to avoid the clock distribution to every pixel. One can of course also consider compromises, distributing the clock to groups of pixels but not to every pixel individually. The break-even hit rate $R_{P_{clock}=P_{hit}}$ where the power P_{clock} required to distribute the clock to every pixel equals the power P_{hit} to transfer the hit information to the periphery immediately depends on the number of pulses per hit, the clock frequency, the pixel pitch and the column height:

$$R_{P_{clock}=P_{hit}} = \frac{f}{pBH} \tag{5}$$

resulting in 0.8 Ghit/cm^2 for the values above, indicating the very high hit rates needed from a power density point of view to justify distributing the clock or a time reference over the matrix reaching all pixels. For the pixel detector upgrade of the ATLAS detector at the HL-LHC only the innermost pixel layer significantly exceeds this hit rate for a 2 cm column height and a 50 μm pixel pitch [103,107], and not any more for a 15 μm pixel pitch or below. If the height of the column would be increased, the pixel pitch should reduce further to justify not distributing the clock to every pixel. One possibility is to apply significant clock gating to avoid distributing the clock to every pixel to reduce the power consumption while still profiting from the simplification of a synchronous design. Please note that in the above only full swing CMOS transmission is considered. Other transmission schemes, like low-swing signaling can be considered to further reduce the power consumption, as for instance in [108], reaching 0.28 pJ/bit for 2 Gbit/sec over 1 cm at the price of increased complexity. Low swing signaling also significantly reduces the current peaks during the switching.

6.4. Off-chip data transmission

The interest in ever-increasing bandwidth for off-chip data transmission is much wider than only in HEP. State of the art was a few pJ/bit with a bandwidth exceeding tens of Gb/s a few years ago in 65 nm technology [109] and now over 200 Gbit/s, for instance at 1.88 pJ/bit in [110]. In HEP SEU sensitivity needs to be minimized especially for Phase Locked Loops (PLLs). This is to avoid significant data loss if the lock is lost, but typically requires large capacitances or redundancy through majority voting, leading to a higher power consumption. The transmitter on the Timepix4 chip [111], based on an earlier design for the VELOPIX chip [112], approaches the state of the art, reaching 10 Gb/s for 30 mW, or 3 pJ/bit.

6.5. Resistive voltage drops

Comparable numbers for power consumption for on-chip data transmission per cm (!), and off-chip data transmission, raises interesting system questions, beyond the scope of this paper: for instance where to locate the transmitters on a large chip, and the repeaters on a longer line, etc. Readout of pixel arrays is often organized by columns. It is therefore interesting to consider the resistive voltage drop in a pixel column: the voltage drop for a line of width W and thickness t, resistivity ρ for a column height H can be written as:

$$\Delta V = \int_0^H \frac{\rho}{Wt} I(y) dy \tag{6}$$

where I(y) is the current flowing through the line at position y in the column. If in this simplified calculation, it assumed that the width of the line covers the full pixel width, I(y) can be expressed as the integral of the current density J times W from the position y within the column to the top of the column. This then yields:

$$\Delta V = \int_0^H \frac{\rho}{Wt} \int_y^H W J dx dy = \int_0^H \frac{\rho}{t} J(H-y) dy = \frac{\rho J H^2}{2} = \frac{R_{sq} P H^2}{2VDD} \tag{7}$$

where R_{sq} is the sheet resistivity of the metal line, VDD the power supply voltage, and P the power density. The voltage drop is proportional to the square of the column height. For a 10x10 μm^2 pixel and 10 nA per pixel at 1 V, or 10 mW/cm^2 with 50 mΩ per pixel, the voltage drop for a column height of 2 cm is 1 mV, but 100 mV for a 20 cm high column, both for power and for ground, which is quite significant for a 1 V supply. Hit related power densities are proportional to the column height H, but the corresponding voltage drops are proportional to H^3, i.e. to the column height to the third power, and require specific optimization for large chips.

The analog power consumption can potentially reduce drastically with decreasing line width of the CMOS technology due to the lowering of the capacitance of the collection electrode. The benefit in terms of power consumption for the same data rate is less clear for the long-distance on-chip data transmission as neither the line capacitance nor the power supply voltage reduce that much any more in very deep submicron CMOS technologies. Similarly the power consumption of the off-chip data transmission for a certain data rate is determined more by the characteristics of the load rather than by the line width of the technology. However, a more advanced smaller linewidth technology will significantly improve the maximum data rates for both on- and off-chip data transmission.

6.6. Stitching and wafer stacking

Stitching is now offered in several CMOS technologies to obtain chips larger than a single reticle. This opens perspectives for wafer-scale sensors and unequaled integration possibilities, but represents several challenges:

- Power density and resistive drops become severe constraints as the size of the sensor increases. As illustrated above, voltage drops in the power network may actually easily become of the same order of the power supply itself. This can be mitigated with additional metal in redistribution layers or flex circuits at the cost of additional material, or by innovative design to cope with such voltage drops.
- Stitched sensors require to be designed with prior concern for yield, respecting more conservative design rules in certain places, and protecting the circuit against single defects killing the full sensor. In principle, if an otherwise fatal defect could be isolated with sufficiently high granularity, it may be possible to conserve functionality for a sufficiently large fraction of the full area,

for instance above 99%. This would allow the yield of wafer-scale sensors as defined for high energy physics but perhaps also for other applications to approach 100%, and would really be a break-through. This would be one of the most important fundamental differences between a monolithic CMOS sensor and a traditional sensor wafer, as the required granularity for this imposes the presence of circuitry on the wafer.

- The complexity and scale of stitched sensors require digital-on-top design and verification, and a very modular design to avoid excessively long verification times, especially if the full chip reaches wafer-scale.
- Connecting to a wafer-scale sensor should be sufficiently cheap to make stitching worthwhile, but this presents significant technical challenges: a sensor covering a full 300 mm wafer will require very large data transmission bandwidths in the inner layers, and every mW/cm^2 at 1 V supply corresponds to 0.7 Ampere for the full wafer.

Wafer stacking was already mentioned in 2.7. Several foundries now offer fully finished stacked assemblies just as they provide normal monolithic active pixel sensor chips implemented in a single wafer. This makes the distinction between hybrid and monolithic sensor less clear, but provides opportunities to the HEP community for even more advanced integration. Also this comes with design and verification challenges, as the different die in the stack need to be addressed with their interconnection. This increased complexity again pushes for a very modular design in a digital on top design flow.

If all the technical challenges of the sensor design itself and the connection to it are addressed to profit from the advanced integration possibilities, it will be essential to foresee from the start efficient ways to test, assemble, mount and commission very large area detectors in a more industrialized way to make them accessible for our community from a cost and time point of view. As an example construction of a 300 m^2 detector over three years would require a pace of about 2 m^2 per week.

7. Other applications

Large area pixel sensors are enabling devices for tracking and calorimetry in HEP, but also for space-borne instruments, other scientific instruments, and also in the medical field: Time-of-flight Positron Emission Tomography was already mentioned. Another application in the medical area is proton therapy, where about 50% of the time is 'lost' localizing the patient with respect to the proton beam before the real treatment can take place. Both a tracker and a calorimeter are considered to fully reconstruct trajectories and energy loss of the protons. This has been investigated with ALPIDE chips for the tracking and a calorimeter prototype using SiPMs [113,114]. A similar development was carried out in [115]. A further illustration of the interest in pixel sensors is the successful Medipix project [116] where primarily hybrid pixel sensors have been pursued, for medical applications but also dosimetry and neutron detection.

8. Conclusions

Monolithic sensors for HEP profit from the progress of CMOS imagers for visible light and the integration these technologies offer with stitching and wafer stacking. Requirements for HEP exhibit several specific differences. Images in HEP are typically very sparse with occupancies less than 1%, where the sensor has to tell where and when particle hits were recorded. The in-pixel circuitry for HEP is typically much more complex, contains typically hundreds transistors instead of only few. Some foundry flexibility is still helpful for HEP.

Circuit radiation tolerance has significantly increased as with standard CMOS attaining several MGy in 65 nm. Sensor radiation tolerance in monolithic sensors is reaching 10^{15-16} 1 MeV n_{eq}/cm^2 primarily using a higher electric field to accelerate the charge collection. For higher radiation levels, thinner detection layers, smaller detection volumes per channel, and higher initial doping may be required.

Lower power densities are needed to be competitive with traditional technologies in the outer tracking layers. Analog power consumption is often dominant. It can be reduced by increasing the Q/C ratio at the input of the circuit, either by lowering the capacitance using a smaller feature size technology or optimizing the sensor, or by introducing a gain mechanism in the sensor. Also front end improvements could lower the analog power. Hit rate related power consumption becomes more and more important and requires specific optimization. Large sensors present significant challenges related to resistive voltage drops.

The presence of circuitry on a monolithic sensor is a fundamental difference with traditional sensors, and may actually allow the design of wafer-scale sensors in which the effect of local, otherwise fatal defects is mitigated enabling high yield. This would present a true game-changer for the construction of large area detectors. Efficient volume test, assembly, mounting and commissioning should complement this to make very large area detectors accessible for our community.

Many foundries now propose wafer stacking, providing opportunities for even more advanced integration and making the distinction between monolithic and hybrid detectors less clear.

A Monolithic Active Pixel Sensor is a complex circuit with extra constraints: sensor bias, coupling into the sensor, etc. The increasing complexity requires an evolution towards digital-on-top design techniques with increasing verification effort by a team of expert chip designers, complemented with device/TCAD/Monte Carlo experts for sensor optimization and simulation. It takes years to train people for this activity and our community should preserve critical mass and know-how for this activity.

Large area pixel sensors are enabling devices for many cutting edge research fields and practical applications like tracking in HEP, medical imaging, space-borne instruments, etc. MAPS are one of the few areas where production volume even within HEP would not be negligible, but where our community can have an impact not only on the quality of its own measurements, but also on society in general, and which we should try to exploit to enable access to the most advanced technologies. A significant evolution in this area is the increasing interest in precision timing and 4D tracking applications.

It is the author's belief that monolithic sensors will become very widely applied in HEP, in tracking, calorimetry and timing detectors. NIEL tolerance up to a few 10^{16} 1 MeV n_{eq}/cm^2 will be reached in the near future, even for small collection electrodes, together with the tolerance to ionizing radiation of several MGy already established now. Unprecedented integration possibilities have become accessible through stitching and wafer stacking, enabling pixel pitches of the order of 10 μm in the very near future, limited in practice primarily by the power consumption and the associated on-chip power supply drops. Significant advances in this area will be an enabler practically for all applications in HEP. This concerns not only the most demanding in terms of rate, radiation tolerance and timing, but also the ones targeting low mass, much lower rates, and the layers further removed from the interaction point, where the production volume is. This may also result in the adoption of smaller pixels even for applications where this is not a primary requirement.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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