

Study of operational properties of the ASDBLR chip for the LHCb Outer Tracker.

V.Gromov, T.Sluijk, A.Berkien, E. van den Born.
NIKHEF, Amsterdam.

Abstract.

Operational properties of the ASDBLR chip have been studied in view of its intended use as front-end chip for the LHCb Outer Tracker. Particular attention was paid to after pulsing behavior, cross talk and double pulse resolution. We measured responses to a point ionization source (Fe^{55}) in 5mm diameter straw tubes, filled with Ar-CF₄-CO₂ gas mixture. Further, a detailed study of cross talk on the board has been carried out to identify the cause of multiple response to pulses of large amplitude, as observed in earlier test beam data.

Introduction.

The ASDBLR chip (Amplifier-Shaper-Discriminator with Baseline Restoration) is a leading candidate to be employed as front-end chip of the LHCb Outer Tracker. The eight channel analog bipolar integrated circuit serves as the interface between straw proportional tubes and the edge sensitive timing circuit required to extract position information from the straw chamber [1]. Being designed for use in the straw-based Transition Radiation Tracker (TRT) of the ATLAS detector the chip meets competing requirements for short measurement time ($\approx 8\text{ns}$), good double pulse resolution ($\approx 40\text{ns}$), low power ($< 30\text{mW/ch}$) and low operational threshold ($\approx 1.5\text{fC}$).

Track resolution in a straw is about 150-200 μm , which translates to an electronic resolution of 1.5-2.5ns when the Ar(65%) CO₂(5%) CF₄(30%) gas mixture proposed for the detector is used. The most reliable method to achieve nanosecond timing is to trigger on the earliest available clusters, which requires an electronics threshold that is as low as possible. Being optimized from signal-to-noise ratio point of view, the chip indeed permits threshold operation down to 1.5fC. The ASDBLR's peaking time of 8ns is set to minimize time jitter arising due to varying pulse height from the statistically small number of primary drift electrons. Low power consumption ($< 30\text{mW/ch}$) makes it possible to place the electronics on the detector directly, minimizing pickup noise and input capacitance .

A minimum ionizing particle (m.i.p.) leaves a track of primary electron clusters when it traverses the straw volume. The electrons drift to anode wire in the course of 0...30ns depending on the track position. To be able to integrate as many clusters as possible on one hand and to get a good double pulse resolution on the other hand the ASDBLR has 25ns shaping time. A non-linear differentiation circuit called baseline restorer is implemented in the chip to break the DC path from the shaper to the discriminator. DC offsets or low-frequency noise cannot reach the discriminator inputs. Though two discriminators are available in the ASDBLR, only the 'tracking discriminator' is used for our application. This is time-over-threshold circuit that provides sharp turn-on with a 1 ns risetime and minimum output width of approximately 5 ns.

The straw current signal has a sharp subnanosecond risetime (see Fig.1), but slowly returns to baseline over the course of many microseconds. This behavior is determined by positive ion drift from the anode wire towards the cathode straw tube. The long ion tail is incompatible with the high rate performance required for the Outer Tracker. This problem is solved by a special ion tail cancellation network in the ASDBLR after the preamplifier stage (see Fig.2). Since the shape of the ion tail is different for different gases the network must be suited to the particular straw geometry and particular type of the gas mixture. The ASDBLR provides selectable ion tail cancellation for two gas options. One is suited for Xenon-based gas, and other is optimized for CF₄-based gas. The Ar(65%) CO₂(5%) CF₄(30%) mixture envisaged in the Outer Tracker is neither Xe-based nor CF₄-based. Figure 1 shows how different the ion tails are. Non-optimum tail cancellation results in improper operation of the baseline restorer, which is in fact a differentiation circuit. In case of overcompensation it can cause mini-oscillation and after pulsing

on the discriminator output, whereas undercompensation results in pulse widening and decreasing double pulse resolution capability (see Fig.3).

The purpose of our research was to study ASDBLR response to a point ionization source (Fe^{55}) in 5mm diameter straw tube, filled with $\text{Ar}(65\%) \text{CO}_2(5\%) \text{CF}_4(30\%)$ mixture from point of view of after pulsing behavior and double pulse resolution time.

In test beam data we also have found cases where a single track led to many spurious hits within one straw plane, which indicates a cross talk phenomenon. Some of these hits were in remote channels. This does not fit usual pattern of preferred cross talk between active and neighbour channels. The cross talk can in principle come from straw-to-straw coupling, from trace-to-trace coupling on the board or from inside of the ASDBLR. We would like to understand where does it come from, how many channels it affects, what is level of the cross-talk to be able to solve the problem afterwards.

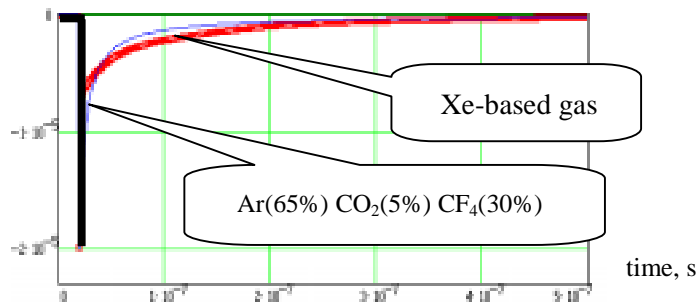


Fig.1. Current from a straw, filled with Xe-based gas (thick trace) and from a straw, filled with our $\text{Ar}(65\%) \text{CO}_2(5\%) \text{CF}_4(30\%)$ gas mixture.

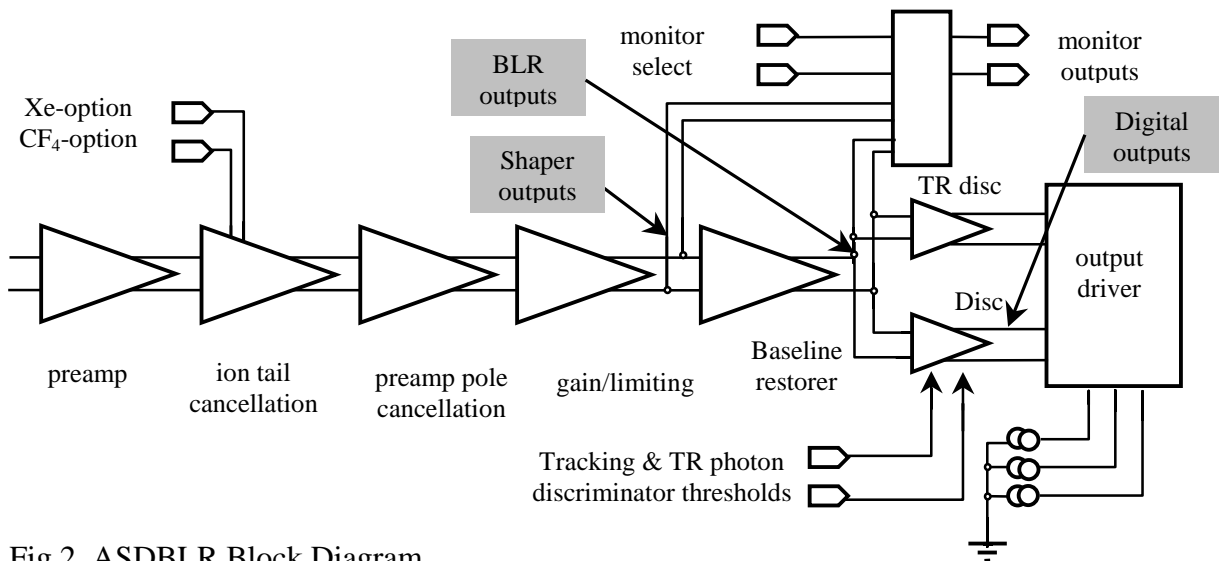


Fig.2. ASDBLR Block Diagram.

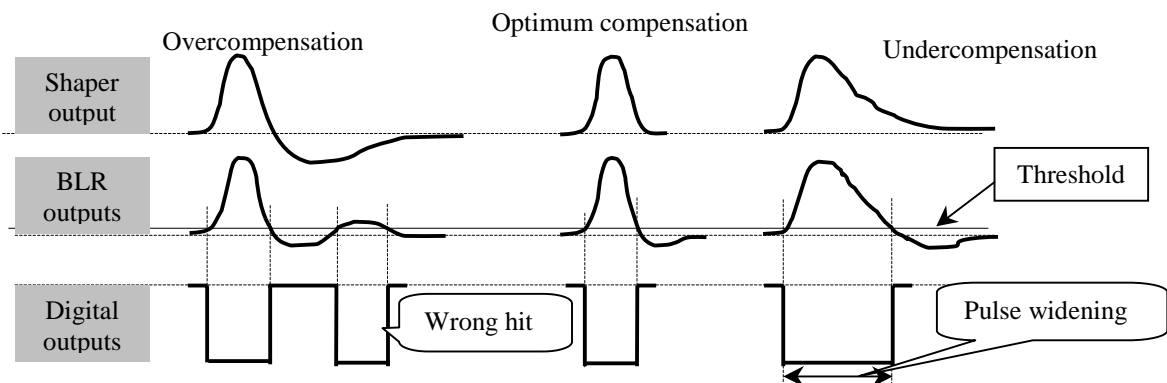


Fig.3. Example of some effects due to incorrect ion tail compensation .

The experimental set-up.

A sketch of the experimental set-up is given in figure 4. A detector module consists of two layers of 5mm diameter straws (made of double windings of Carbon doped kapton) enclosed in a box to get a gas tight volume. Straw-to-straw distance is 1mm within one layer. The layers are separated by a grounded foil of 25 μ m aluminum to provide a good signal transmission. The chamber is supplied with an Ar(65%) CO₂(5%) CF₄(30%) gas mixture. The straw current response to a Fe⁵⁵ radiation source is identical to the m.i.p. response in its decay part, which depends on the gas mixture and the electrical field inside the straw (see Fig.1). For study of the quality of ion tail cancellation, use of a Fe⁵⁵ source is thus quite suitable. The m.i.p. pulse height distribution (with pulses up to 300fC, distributed according the Landau expression) differs strongly from the distribution for Fe⁵⁵. However, by adjusting the high voltage on the anode wire we are able to produce pulses within the same dynamic range with Fe⁵⁵.

Anode wire leads feed the ASDBLR inputs through a high voltage capacitor. Shaper or BLR outputs of two channels on each chip can be monitored optionally (see Fig.2). A digital scope in single shot mode or in averaging mode was used to observe the signals.

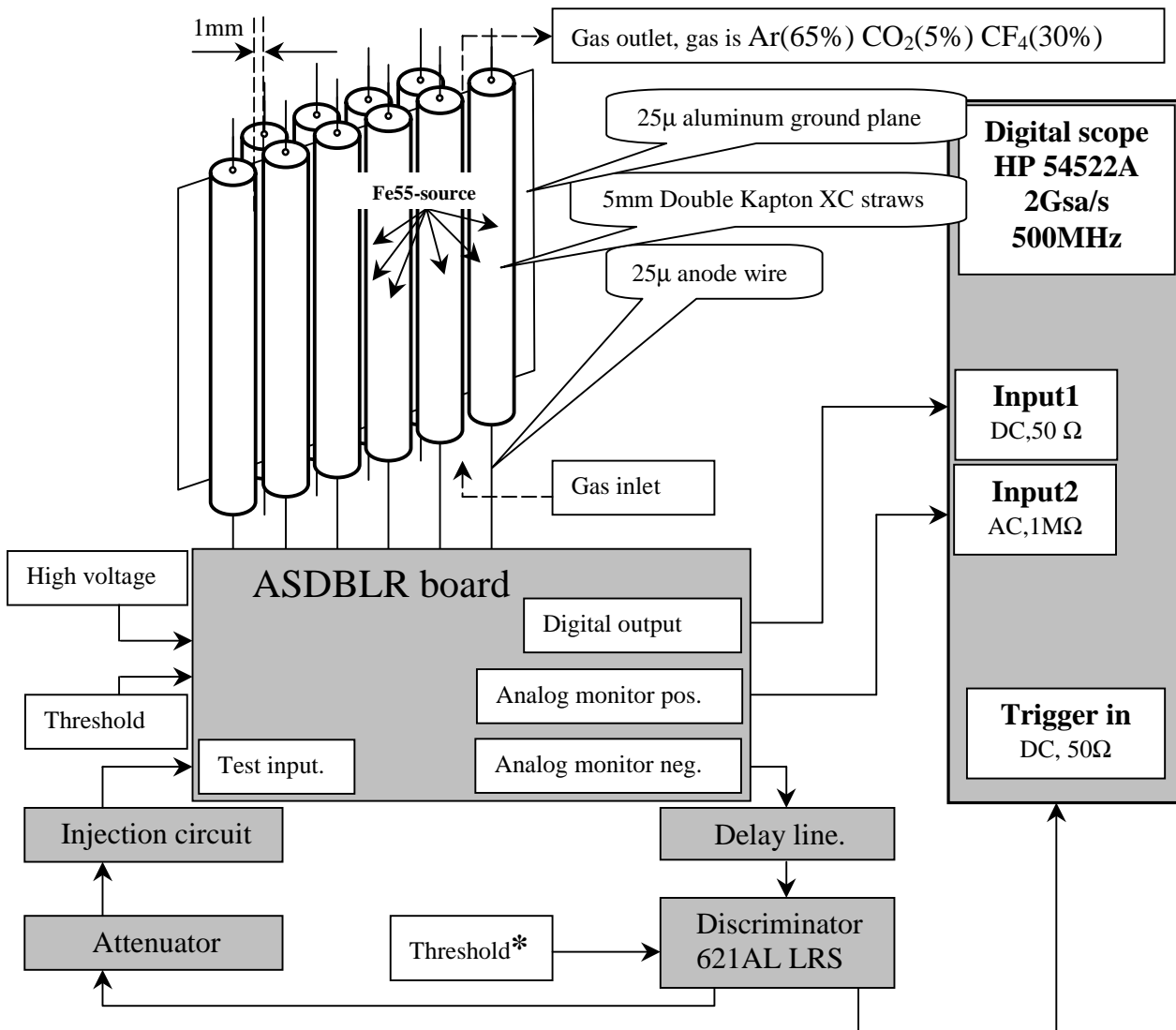


Fig.4. The experimental set-up.

To study double pulse resolution, a Fe⁵⁵ hit must be followed by a second pulse. We want to know how often the second pulse does not produce a separate digital output as a function of its amplitude and latency and the amplitude of the first hit. A dedicated chain has been constructed to make all the parameters adjustable. The chain consists of delay line, discriminator, attenuator and injection circuit. The negative analog monitor output triggers the chain to inject an ionization-like current into the test input of the ASDBLR.

ASDBLR calibration.

Input charge is used as a measure of signal amplitude. For example, we call a Fe^{55} hit a 2fC signal when its amplitude at the ASDBLR output is equal to that of a 2fC δ -pulse. The ASDBLR calibration curve is given in figure 5.

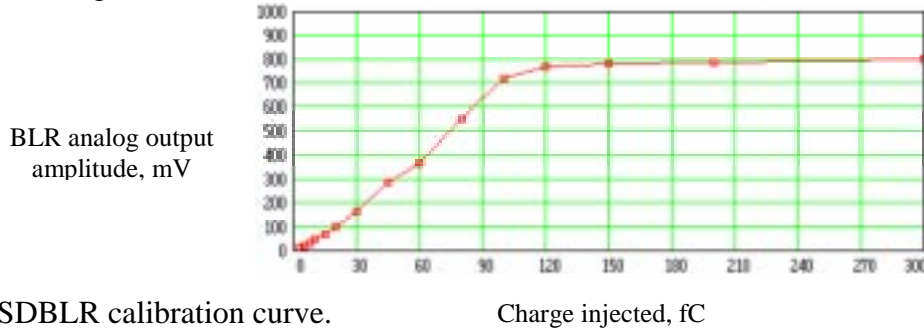


Fig.5. ASDBLR calibration curve.

Charge injected, fC

ASDBLR after pulsing study with Fe^{55} .

As stated before, the ASDBLR offers two tail cancellation options. It is possible to select one of them externally. We tested both with our gas mixture.

By means of high voltage tuning, signals of different amplitudes have been studied. The threshold was set at 2fC. ASDBLR output signals are given in figure 6 and figure 7.

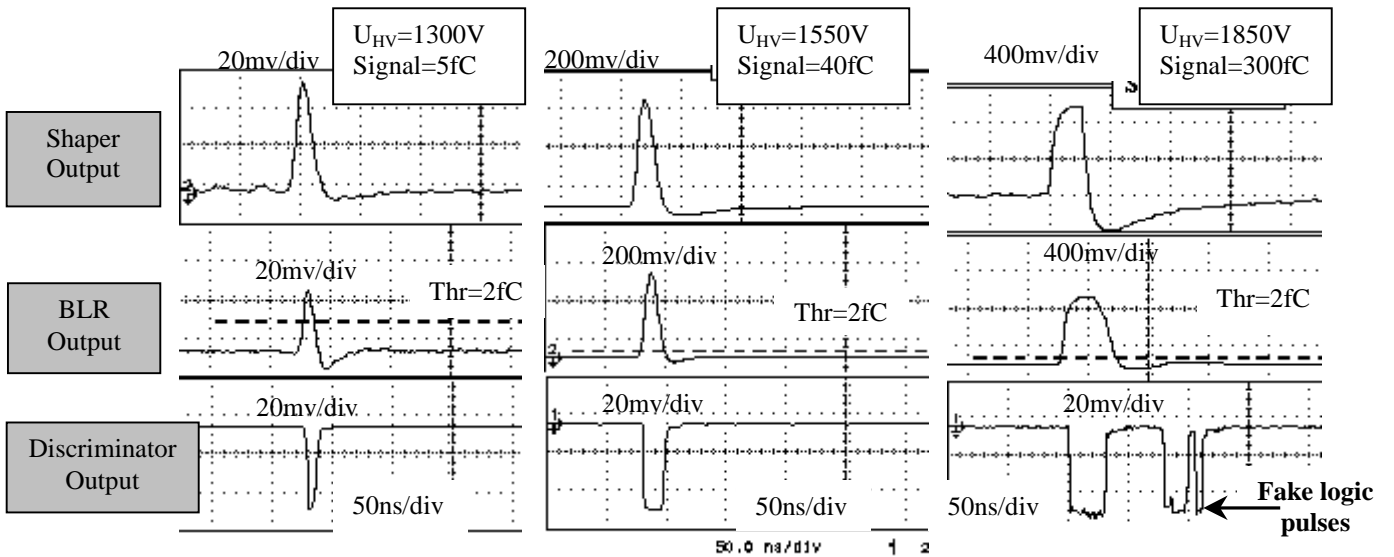


Fig.6. ASDBLR responses to 5fC, 40fC and 300fC equivalent hits. Xe-optimized tail cancellation circuit.

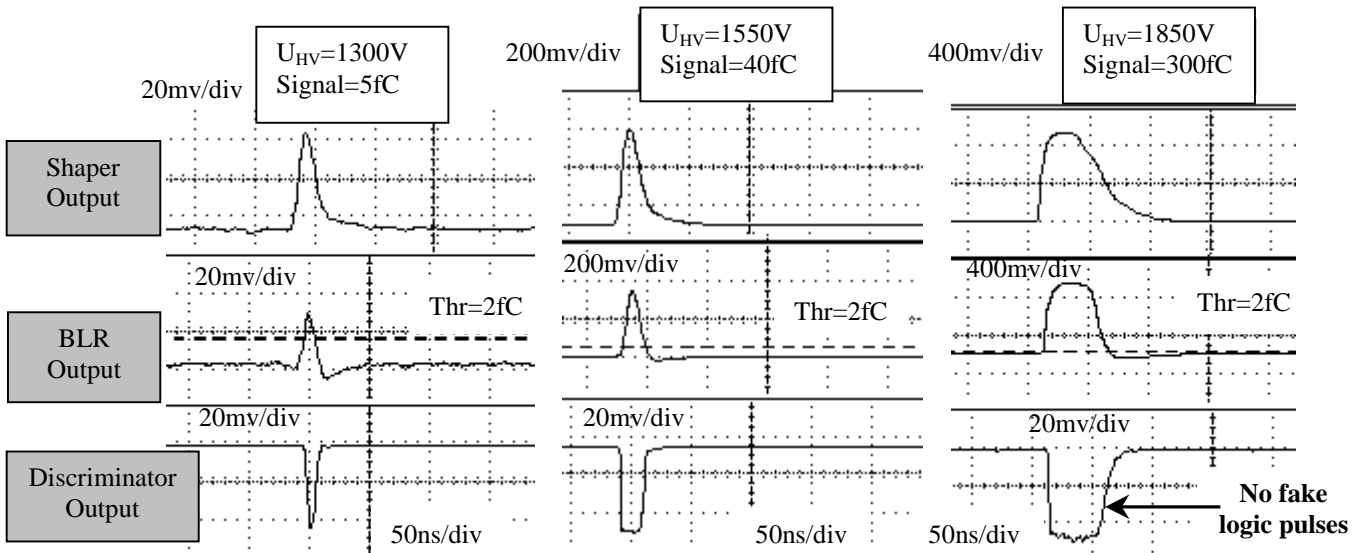


Fig.7. ASDBLR responses to 5fC, 40fC and 300fC equivalent hits. CF_4 -optimized tail cancellation circuit.

No fake pulses appear at the discriminator output if the CF₄-option is chosen for ion tail cancellation (see Fig.7). When Xe-option is selected, the ASDBLR does produce fake pulses (see Fig.6). In figure 8 and figure 9 the same pictures are given on a finer scale to show the source of the fake pulse.

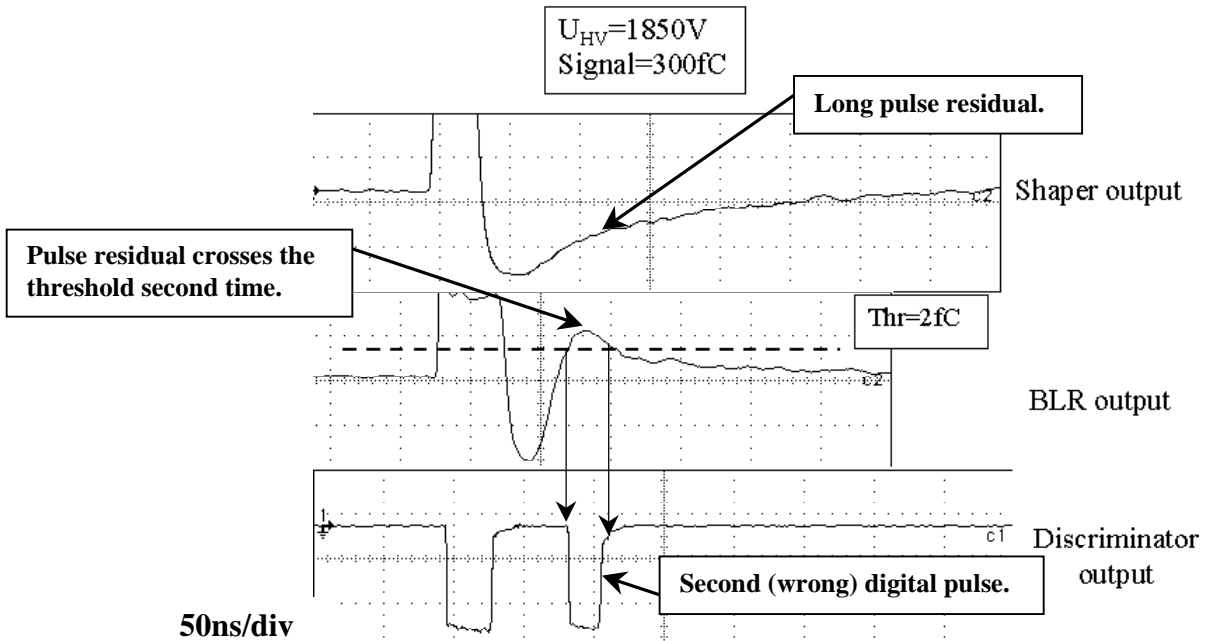


Fig.8. ASDBLR response to a 300fC equivalent hits. Xe-optimized tail cancellation circuit. **50ns/div**.

Figure 8 shows that ion tail overcompensation on the shaper output results in wrong BLR operation, which in turn causes fake pulses at the discriminator output.

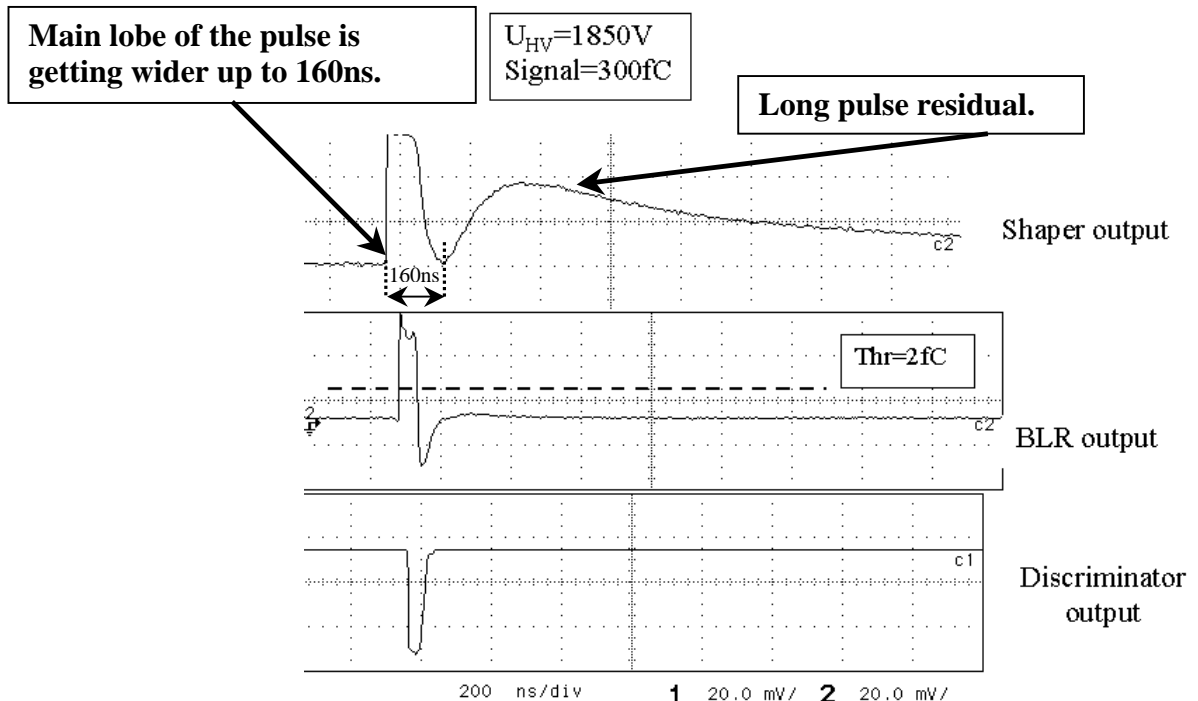


Fig.9. ASDBLR response to a 300fC equivalent hits. CF₄-optimized tail cancellation circuit. **200ns/div**

Ion tail cancellation is not perfect in the CF₄ case either, but the tail residual is quite slow (time scale is 200ns/div in Fig.9). The fast BLR used manages to get it down below the threshold level preventing the wrong logic pulse to appear. It does not show up even if the hit is very big (up to 300fC) at very low (2fC) threshold (see fig.9).

ASDBLR double pulse study.

To study double pulse resolution we used Fe^{55} hits as a trigger to start injection of a second pulse into the test input of the ASDBLR. The question is to what degree the first hit masks the following one. We used the CF₄-option on the ASDBLR along with 2fC threshold. Different combinations of the pulse amplitudes and their spacing in time have been studied. In figures 10 to 14 several cases are presented. Because of internal delay it was not possible to get a delay below 30ns. It anyhow is not of interest to consider a pulse-to-pulse gap shorter than 35ns, since the total charge collection time from ionizations along a single track segment will typically be of that order.

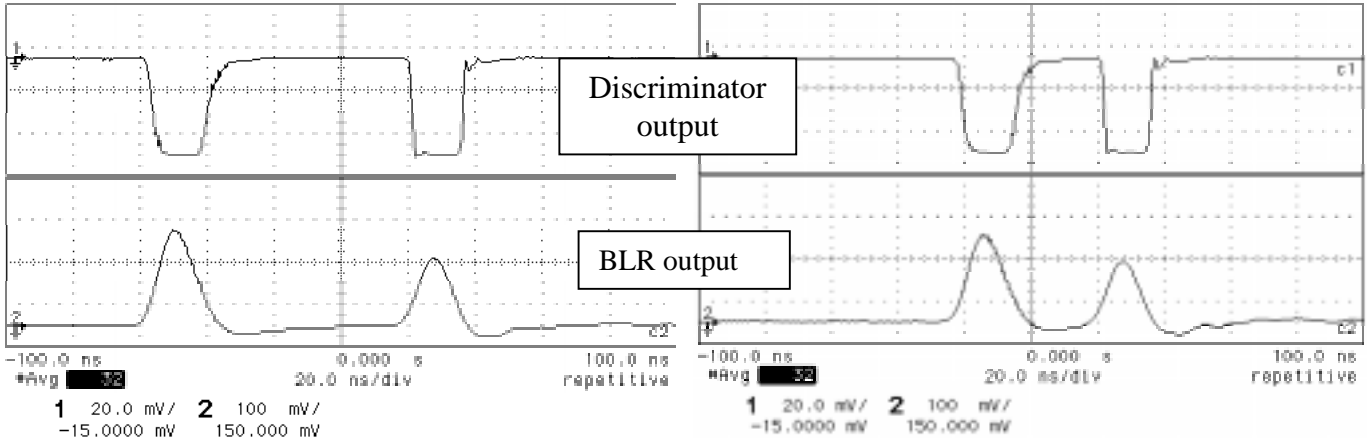


Fig.10. Averaged 25fC pulse (one MIP), followed by 18fC pulse at 75ns and 40ns distances.

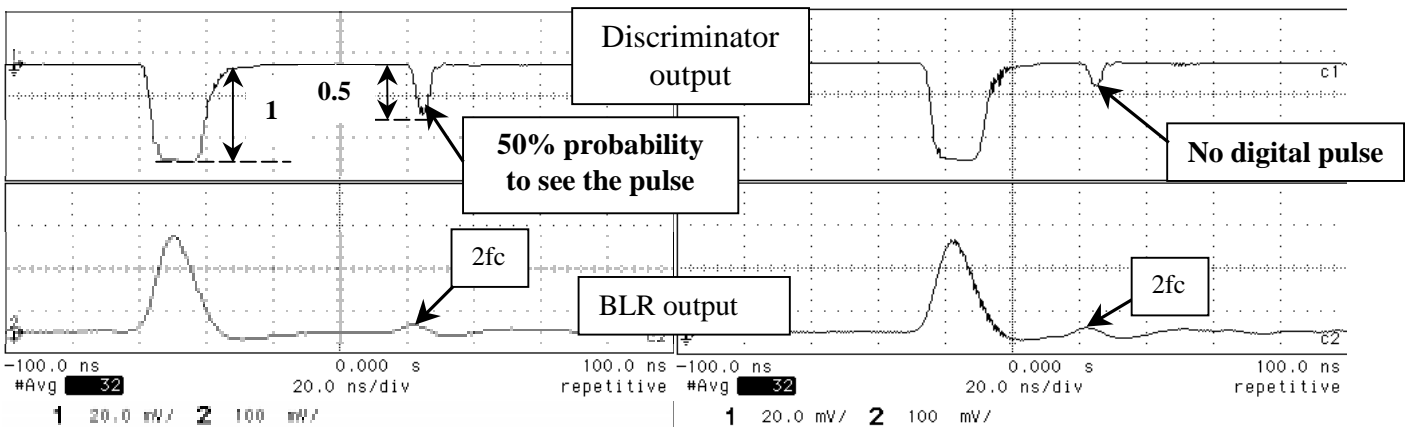


Fig.11. Averaged 25fC pulse (one MIP), followed by 2fC (the smallest possible) pulse at 75ns and 40ns distances. The 2fC pulse is definitely lost at 40ns distance.

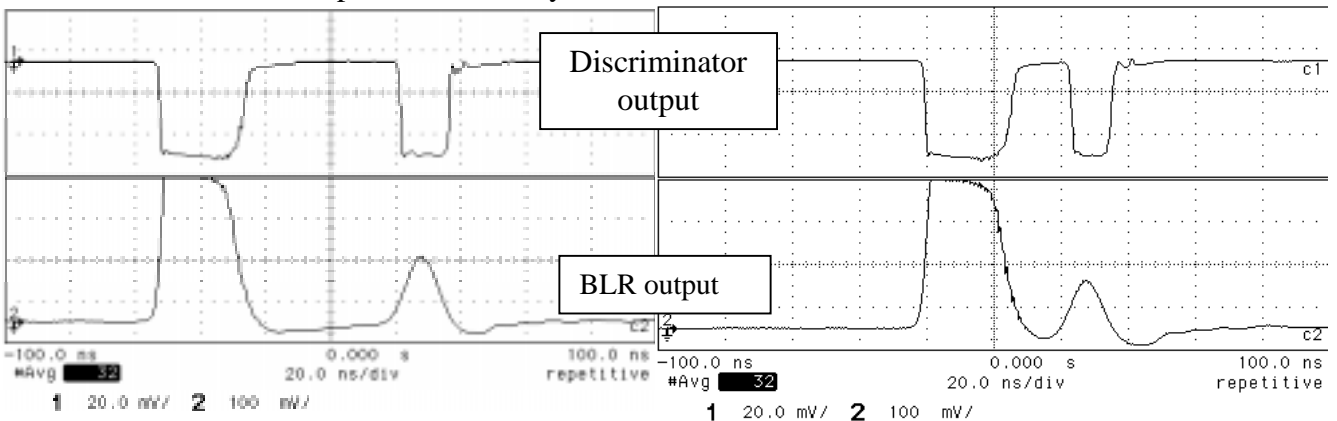


Fig.12. Averaged 100fC pulse (four MIPs), followed by 18fC (close to MIP) pulse at 75ns and 40ns distances. No problem.

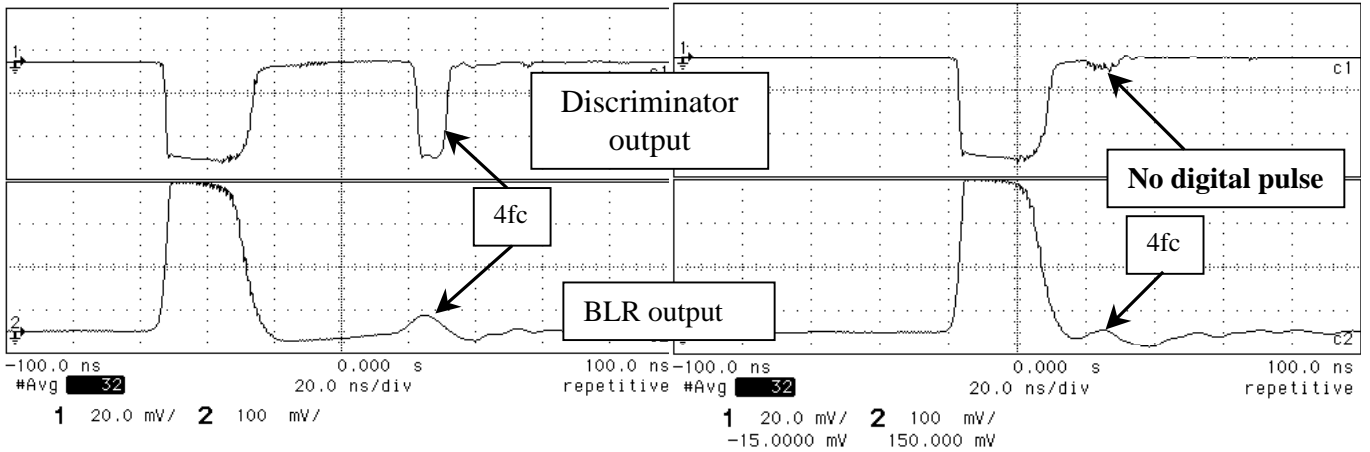


Fig.13. Averaged 100fC pulse (four MIPs), followed by 4fC (close to the smallest possible) pulse at 75ns and 40ns distances. The 4fC pulse is definitely lost at 40ns distance.

The pictures above indicate that small signals (2fC...4fC) are not visible when they follow an average single m.i.p. hit within 40ns distance (see Fig.11, Fig.13). We do not lose the second pulse when it is of order of one m.i.p. even at 40ns after the first one. At 2 MHz hit rate (corresponding to the hottest regions in the LHC Outer Tracker) the chance is small to get two hits within 40ns while one of them is smaller than 6fC.

If the pulse-to-pulse gap is smaller than 30ns, pulses of the normal size (few times the average m.i.p. amplitude) stick together forming one wide pulse on discriminator output.

Summarizing, it seems to be reasonable to estimate the double pulse resolution time of the ASDBLR itself as 40ns for our gas mixture. The chip designers give the same number [1], which proves that the ASDBLR is quite optimal for our detector regarding double pulse resolution.

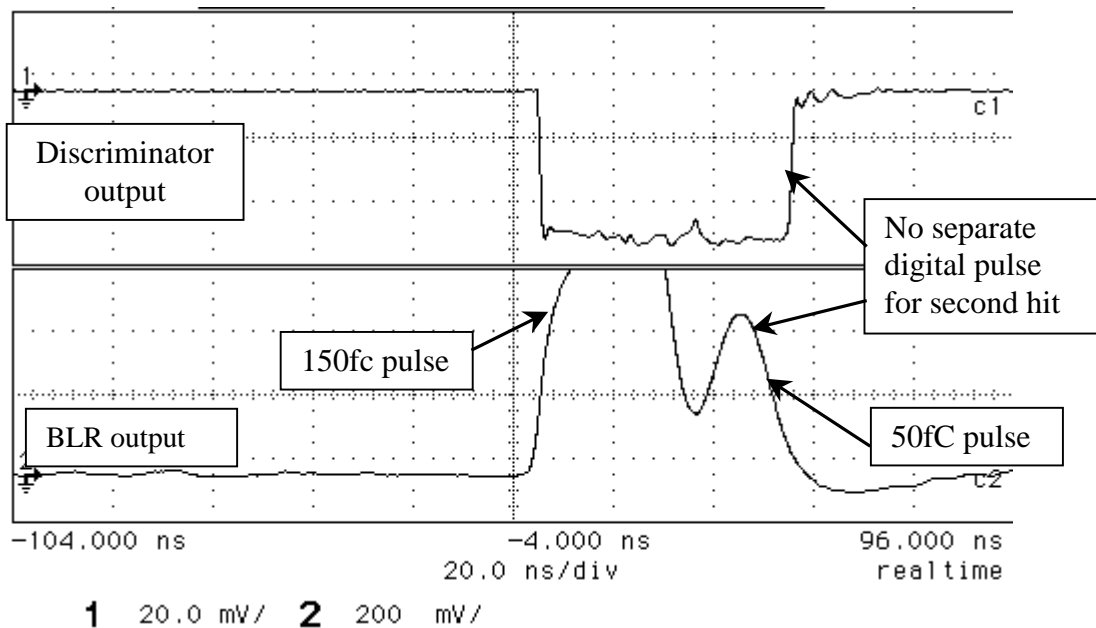


Fig.14. Averaged 150fC pulse (five MIPs) followed by 50fC pulse at 30ns distance. No way to resolve them.

ASDBLR cross-talk study.

In the test beam data taken in 1999 we found that number of fake hits increases with gas gain. It looks like a particle fires up to 8 channels when it traverses one plane of straws. The wrong hits from neighbour channels come a bit later than the real track hits, forming an additional peak at 20 ns in TDC data (see Fig.15).

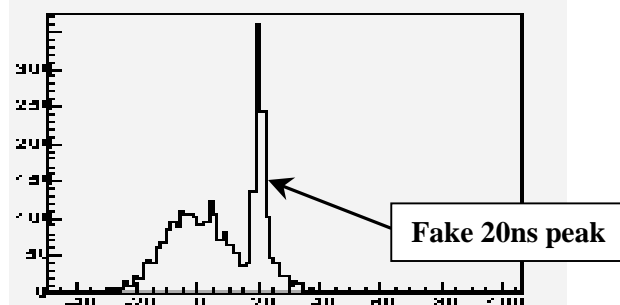


Fig.15. Example of a time spectrum of spurious hits in test beam data.

Since a lot of channels were fired at the same time, we suspect it to be due to cross talk in the electronics. We looked simultaneously at the active channel and channels close by, with signals of different amplitude in the active channel. Threshold of 2fC and CF₄-option were used.

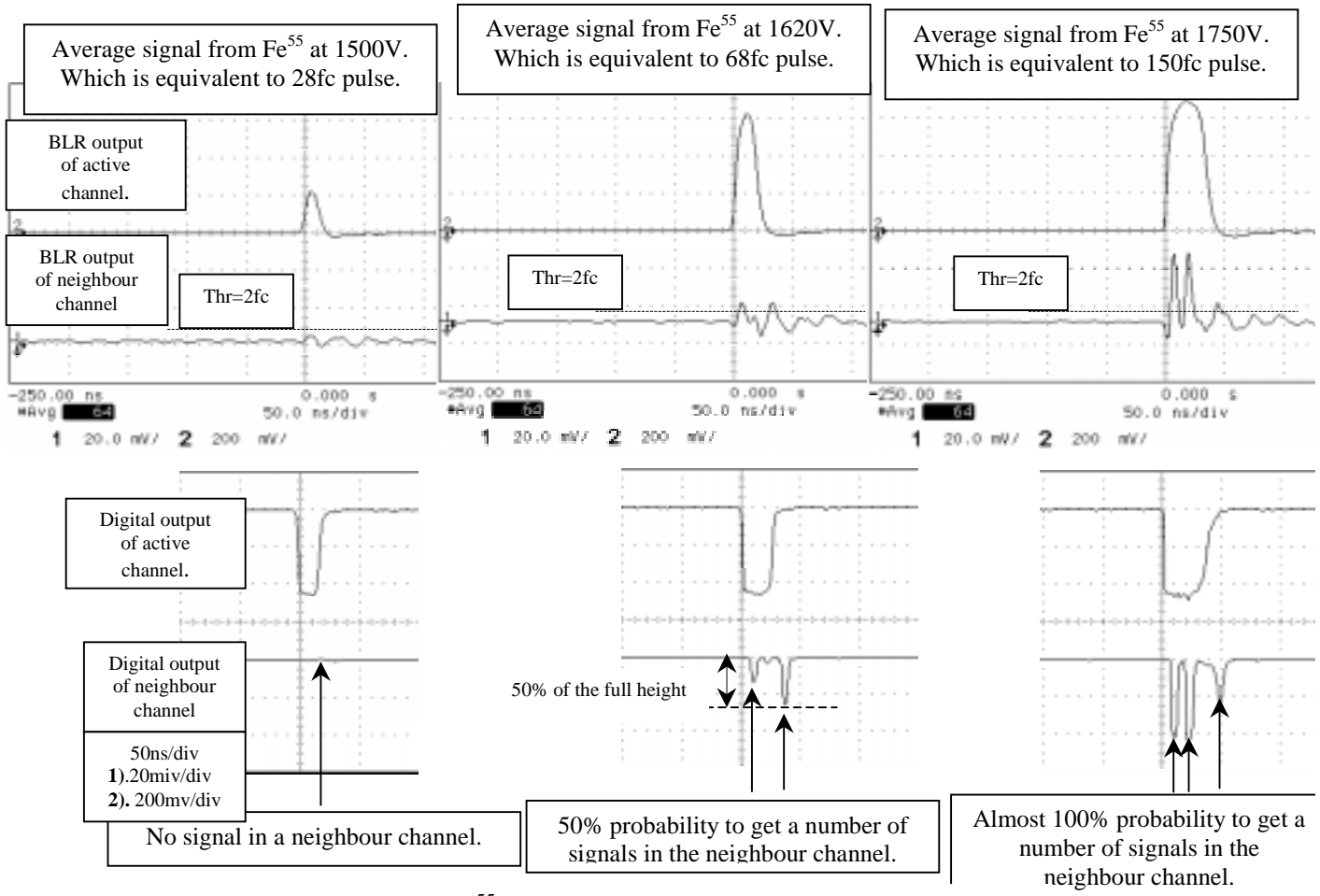


Fig.16. ASDBLR responses to Fe⁵⁵ source at different high voltage values.

Since the Fe⁵⁵ signal is due to γ -conversion at a single space point, only one straw gets hit at a particular time. No unexpected coincidences occur due to the low decay rate (few KHZ) of the source. Figure16 shows that cross talk pulses do not occur at low gas gain (HV=1500V), at 1620V they appear sometimes, they are certainly there at 1750V. The charge seen in a neighbour channel increases with the amplitude of the true signal, increasing the chance to reach the threshold and to trigger a fake pulse. The shape of the cross talk pulses resembles a mini-oscillation as may arise from parasitic capacitive coupling.

The pulse may cross the threshold more than once, causing up to three logic pulses with typical delays of 10ns, 20ns and 45ns (see Fig.17).

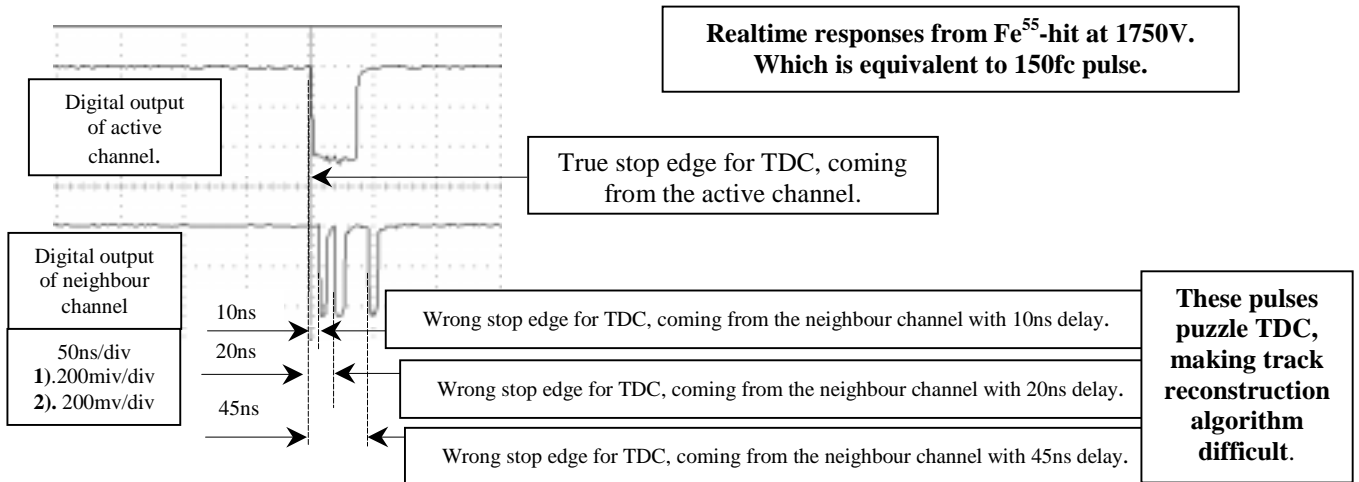


Fig.17. ASDBLR response to Fe⁵⁵ source at 1750V.

The cross-talk pulses are not only present at neighbour channels but also in remote ones. We can hardly imagine that two remote straws have cross talk to the same degree as adjoining straws. One rather suspects the electronics board as the source. On the board all channels are coupled through common traces like ground, power supply bus, test bus.

Results of cross talk measurements on the front-end board.

A dedicated test set-up has been developed to measure cross-talk level on the board (see Fig.18).

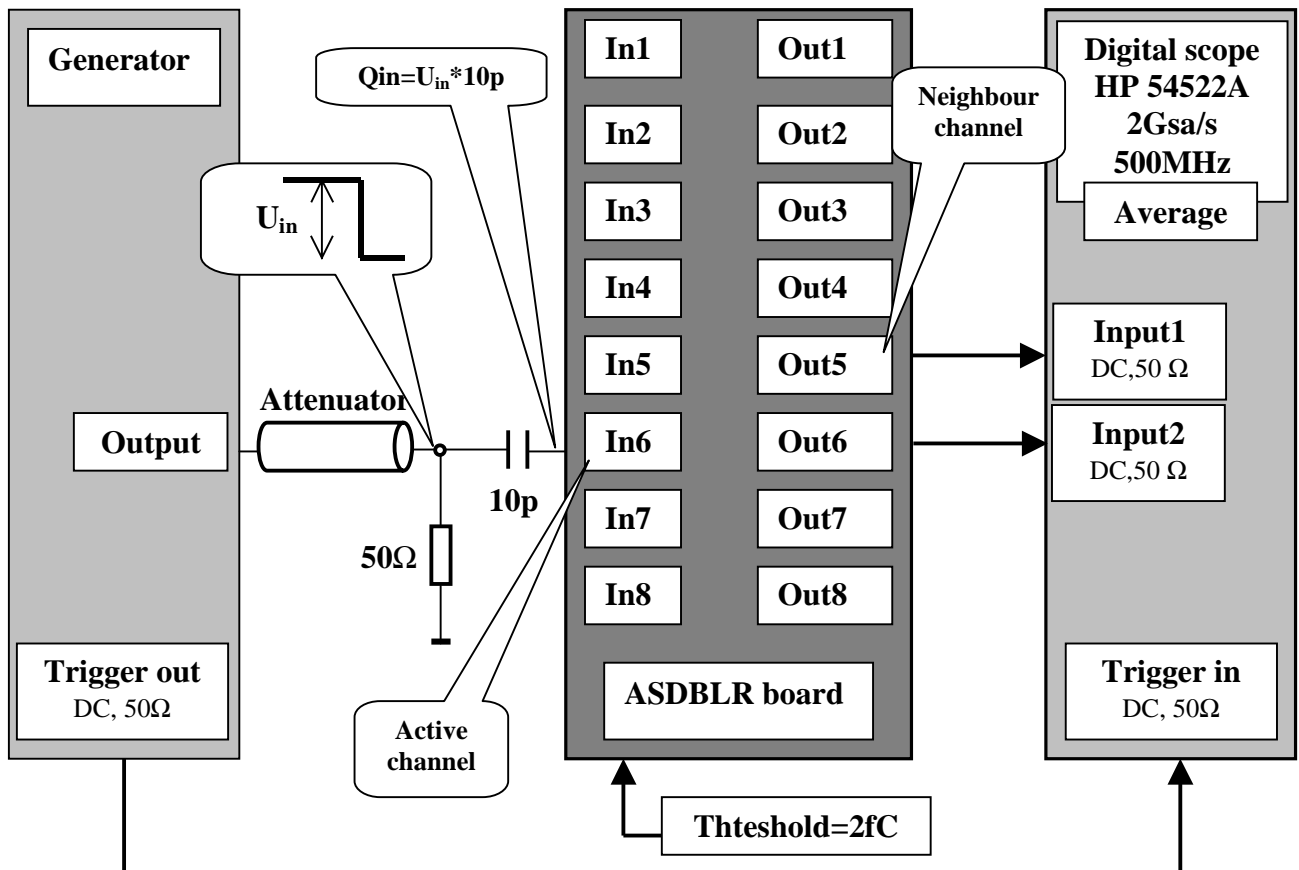


Fig.18. Test set-up to measure cross talk level on the ASDBLR board.

A very short current pulse is injected into the ASDBLR input. We monitor the digital outputs of the active channel and another channel. When a cross-talk pulse just reaches the threshold level, the probability to cross is 50% due to electronic noise. The averaged digital pulse becomes half of the standard height (see Fig.19). Since the injected charge is easy to calculate and the threshold is known we are capable to calculate the cross-talk coefficient as follows: $K_{\text{cross-talk}} = 2fC/Q_{\text{in}}$

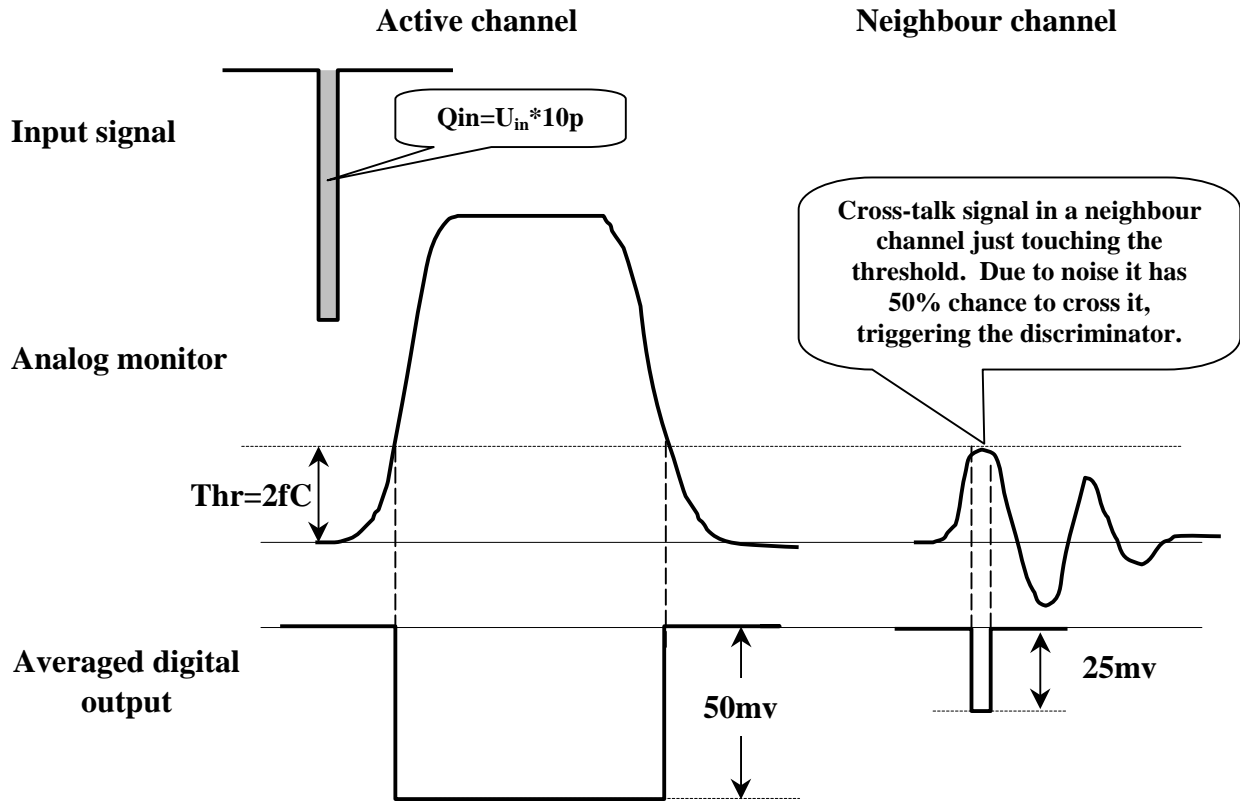


Fig.19. The method to measure cross-talk level on the ASDBLR board .

Cross-talk levels of two front-end boards were carefully measured (see Tables 1-2). We have checked all 32 channels of four ASDBLR chips on the board searching for a tendency. Cross-talk levels much higher than from specification (0.2%) [2] have been found only between channels belonging to the same chip. All channels of the chip are affected by the cross talk in almost the same degree. The level of the cross talk is different for different chips, in range 0.2%...2%. No unexpected chip-to-chip cross talk can be noticed.

Table 1. Cross-talk level on front-end board 6034 B.

	ASDBLR chip IC3				Next chip 9		ASDBLR chip IC4				Next chip 9
	1	2	3	4			1	2	3	4	
Active Channel →											
Monitored Channel ↓											
1	100%	0.3%	0.2%	0.2%	0		0.3%	0.2%	0	0	
2	0.3%	100%	0.1%	0.2%	0		100%	0.3%	0.2%	0	
3	0.3%	0.3%	100%	0.3%	0		0.3%	100%	0.3%	0	
4	0.2%	0.3%	0.2%	100%	0		0.3%	0.3%	100%	0	
9 (Next chip)	0	0	0	0	100%		0	0	0	100%	
	ASDBLR chip IC5				Next chip 9		ASDBLR chip IC6				Next chip 9
	1	2	3	4			1	2	3	4	
Active Channel →											
Monitored Channel ↓											
1	100%	1%	0.8%	0.8%	0		100%	0.5%	0.5%	0.4%	0
2	1%	100%	1%	1%	0		0.5%	100%	0.5%	0.5%	0
3	1%	1%	100%	1%	0		0.5%	0.5%	100%	0.5%	0
4	1%	1%	1%	100%	0		0.4%	0.4%	0.5%	100%	0
9 (Next chip)	0	0	0	0	100%		0	0	0	0	100%

Table 2. Cross-talk level on front-end board

9004 B.

		ASDBLR chip IC3				Next chip	ASDBLR chip IC4				Next chip
Active Channel →		1	2	3	4	9	1	2	3	4	9
Monitored Channel ↓											
1		100%	1%	1%	1%	0	100%	2%	2%	2%	0
2		1%	100%	1%	1%	0	2%	100%	2%	2%	0
3		1%	1%	100%	1%	0	2%	2%	100%	2%	0
4		1%	1%	1%	100%	0	2%	2%	2%	100%	0
9 (Next chip)		0	0	0	0	100%	0	0	0	0	100%
		ASDBLR chip IC5				Next chip	ASDBLR chip IC6				Next chip
Active Channel →		1	2	3	4	9	1	2	3	4	9
Monitored Channel ↓											
1		100%	1%	-	1%	0	100%	1%	1%	1%	0
2		1%	100%	-	1%	0	1%	100%	1%	1%	0
3		-	-	-	-	0	1%	1%	100%	1%	0
4		1%	1%	-	100%	0	1%	1%	1%	100%	0
9 (Next chip)		0	0	-	0	100%	0	0	0	0	100%

To make sure that the chips themselves meet the cross-talk specification, separate chip measurements were performed in a test chip socket (see Table 3). We did not see any deviations from specification (apart from extra cross talk to previous channel, known to be caused by imperfection of the socket layout). These tested chips and chips on the front-end boards were from the same batch, so most probably the board is somehow to blame.

Table 3. ASDBLR chip cross-talk level measurements in the test socket.

		ASDBLR Chip#133				ASDBLR Chip#131			
Active Channel →		2	3	4	7	2	3	4	7
Monitored Channel ↓									
1		4%	0.3%	<0.2%	<0.3%	4%	0.2%	<0.2%	<0.2%
2		100%	4%	0.2%	<0.3%	100%	4%	0.2%	<0.2%
3		0.3%	100%	4%	<0.3%	0.3%	100%	4%	<0.2%
4		<0.3%	0.3%	100%	<0.3%	<0.3%	0.2%	100%	<0.2%
5		<0.3%	<0.3%	0.2%	0.3%	<0.3%	<0.2%	0.2%	0.2%
6		-	-	-	4%	<0.3%	<0.2%	<0.2%	4%
7		<0.3%	<0.2%	<0.2%	100%	<0.3%	<0.2%	<0.2%	100%
8		<0.3%	<0.2%	<0.2%	0.3%	<0.3%	<0.2%	<0.2%	0.2%
		Chip#108		Chip#112		Chip#111		Chip#117	
Active Channel →		2		2		2		2	
Monitored Channel ↓									
1		4%		4%		4%		4%	
2		100%		100%		100%		100%	
3		0.2%		0.2%		0.2%		0.2%	
4		<0.2%		<0.2%		<0.2%		<0.2%	
5		<0.2%		<0.2%		<0.2%		<0.2%	
6		-		<0.2%		<0.2%		<0.2%	
7		<0.2%		<0.2%		<0.2%		<0.2%	
8		<0.2%		<0.2%		<0.2%		<0.2%	

We thus continued with measurements on the boards. Since all channels of an ASDBLR chip have almost equal cross-talk level, a single number can characterize the chip. We repeated the measurements for 12 front-end boards (see table 4).

Table 4. Cross-talk level on the boards used in a test beam run.

Board\ASDBLR Chip	IC3	IC4	IC5	IC6
6034B	0.3%	0.2%	1%	0.5%
9004B	1%	2%	1%	1%
6032B	1%	0.4%	1%	1%
6001A	1.5%	-	-	1.5%
6030A	0.2%	0.3%	0.2%	0.3%

6030B	1%	2%	1%	0.3%
6031A	0.3%	0.3%	0.3%	0.2%
6031B	1.5%	0.3%	0.2%	0.3%
6032A	0.3%	0.3	0.3%	0.3%
6033A	1%	2%	1.5%	1.5%
6034B	0.2%	0.3%	1.5%	0.4%
6034A	0.4%	0.3%	0.2%	0.3%

If the cross talk comes from the board, one expects to see it to the same degree on all boards because of their identical layout. However, different cross-talk levels were measured.

We next examined two boards that have chips with different cross-talk level (0.2% and 2%). We found gain factor, bias voltages and nominals of components within 10% tolerance. The only way to decrease the cross talk to a low level (0.4%) turned out to be to disconnect the input lead of the neighbour channel from the board. Remarkable is that the cross talk is confined to one chip and is about the same size on all 8 channels. The neighbour chip is unaffected.

The measurements do not clearly pinpoint the source of the cross talk. Most likely, a new front-end board design is needed to answer the question.

At the same time, a strong correlation has been found between high cross-talk level (more than 1%) on the chip and appearance of fake hits at 20 ns from a true signal on a channel within the same chip (see Fig.20).

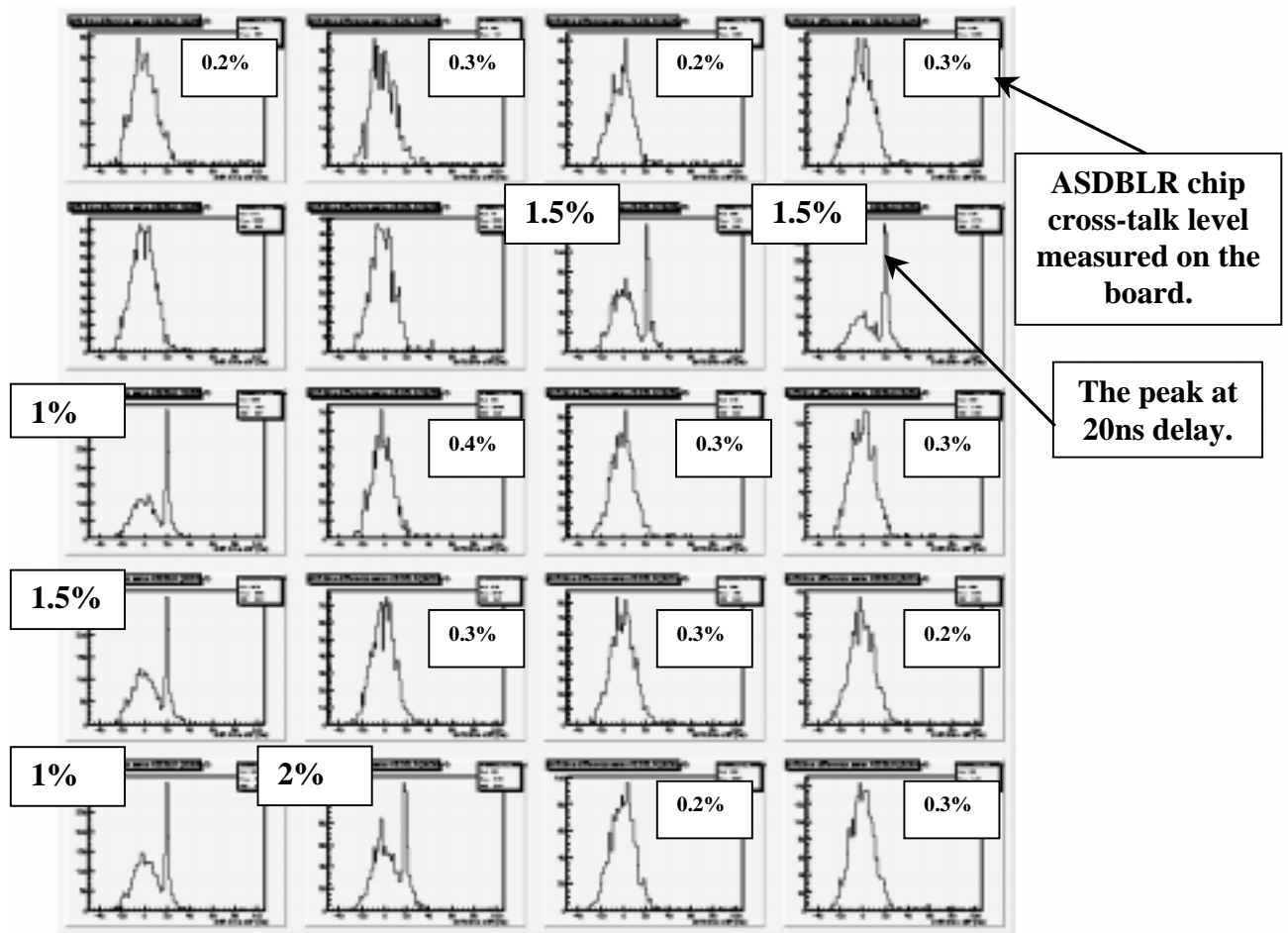


Fig.20. Time distribution of fake hits in non-active straws relative to the hit time in an active one, all being coupled to the same ASDBLR chip.

We think this is the source of data distortion seen in our 1999 test beam run. Being able to measure the board cross-talk level in the test set-up, we can now reliably select good boards. This was proven in the test beam runs of 2000.

Conclusion.

A study of operational properties of the ASDBLR chip has been carried out in view of its foreseen use in the LHC Outer Tracker detector. We constructed a dedicated test set-up to characterize the chip performance relative to the needs of the detector. By doing so we demonstrated the following.

First, of the two ion cancellation circuits inside the chip, only the CF₄ option satisfies our requirements. We studied the chip response to signals from a Fe⁵⁵ source in the range 3fC...300fC. No erroneous logic pulsing has been found. Neither was logic pulse widening found with CF₄ option selected. This is even true at very low threshold (2fC). As expected, the Xe optimized ion tail cancellation option in the chip is not suitable for our detector, since we use the Ar-based gas mixture (Ar(65%) CO₂(5%) CF₄(30%)), which has a different ion tail behavior. In this case a large signal (more than 100fC) triggers a train of a few logic pulses.

Second, double pulse resolution study indicates we easily see a second hit when it is separated from the first one by at least 40ns (CF₄ option is on, threshold is 2fC). Only very small (3fC...5fC) pulses may occasionally be lost at this time separation. Since the process of clusters collection from a track segment in the long (1m...3.6m) non-terminated straws will also typically take 40ns, we expect that ASDBLR contribution to the overall detector dead time will not prevail.

Third, we investigated the source of fake hits within a single straw detector plane, as observed in previous test beam run. Due to parasitic coupling between the channels, an active channel fires up to seven neighbour ones when the original signal is large enough (more than 68fC). Several consecutive logic pulses occur in the non-active channels due to the oscillatory shape of the cross-talk coupling. We found that the parasitic coupling mainly occurs on the front-end board. Only channels belonging to the same ASDBLR chip are affected by this extra cross-talk. The level differs from chip to chip in range 0.2%...2%. The measurements with the ASDBLR chips itself in a test socket indicate no cross-talk above the specified level (0.2%) [2]. It was found that the extra cross-talk could only be reduced by disconnecting the input lead of non-active channel from the front-end board. The board will be redesigned, taking care to avoid parasitic coupling between channels.

Fourth, although the precise source of the extra cross talk has not been found, we observe strong correlation between high cross talk on the boards and a case of data distortion during an earlier test beam run. We are now equipped to test all front-end boards and reliably select good ones.

References.

[1] F.M.Newcomer et. al., *An Amplifier-Shaper-Discriminator with Baseline Restoration for the ATLAS Transition Radiation Tracker*, IEEE Transactions on Nuclear Science, Vol.43, No.3.

[2] ATLAS Inner Detector Technical Desing Report, Vol.II, p.501.