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Progress in the construction of the DELPHI pixel detector

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Abstract

The status of the pixel detector for the DELPHI Silicon Tracker is presented. The main characteristics of the detector, the readout chip and the assembly are summarized.

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1 INTRODUCTION

Tracking hermeticity at LEP 2 energies plays a crucial role for both electroweak physics and detection of Higgs and supersymmetric particles.

The W^+W^- production cross section close to threshold is about 16 pb and the foreseen integrated luminosity at LEP 2 is 500 pb^{-1} per experiment [1], so that the expected number of events is relatively small and the detector efficiency has to be optimized. Pairs of W bosons are produced through the neutrino t-channel exchange and the γ^* and Z^* s-channel exchange. The former process is dominant close to threshold and, as a t-channel, the cross section is forward peaked; because of the W polarization, the final state fermions are sensitive to the W angular distribution, so that about 30% of $e^+e^- \rightarrow W^+W^-$ events feature at least one of the final state fermions below 30^o with respect to the beam line [2].

The detection of a Higgs particle is highly demanding on the detector performances, in terms of tracking and calorimetric hermeticity, b-tagging capabilites and jet reconstruction [3].

In order to optimize the track reconstruction, DELPHI has been planning an upgrade [4] of the current Silicon Vertex detector, extending its acceptance down to 10^o and relying on the use of hybrid pixel detectors in the forward region. The detector assembly is currently under way and commissioning is foreseen for the 1996 data taking run.

2 THE DELPHI SILICON TRACKER

The structure of the new detector is schematically shown in fig. 1. The barrel part consists of three coaxial layers of microstrip detectors [5], arranged so that along a track there will be at least two three dimensional hits from double sided microstrip detectors and one extra hit from single sided detectors having the strips parallel to the beam direction. The end-caps on each side are made out of two crowns of hybrid pixel detectors and two crowns of ministrip detectors [6], arranged to cover the polar angle region between 10^o and 25^o and to guarantee at least three space points along a track.

Each pixel crown consists of 38 modules of 8064 pixels, for a total number of 1225728 channels. The pixel dimensions are 330×330 μm^2 and they are read out in binary mode by bump bonded custom designed front end chips. The detector thickness is about 280 μm and chip thickness is about 380 μm. More details about the detector and the electronics are reported below.

The modules of the innermost (outermost) crowns are inclined by 12^o (32^o) with respect to the beam line; particles will cross the detectors at angles between 52^o (36^o) and 62^o (47^o) with respect to the normal direction to the detector plane, firing a single pixel cluster with a 42% (78%) probability and a two pixel cluster in 55% (20%) of the cases.

Adjacent modules in the innermost (outermost) crowns overlap by about 35% (25%) of their acceptance, providing helpful redundancy for detector alignment and solving pattern recognition ambiguities.

The modules are precisely mounted on Aluminum rings, housing the cooling pipes and mechanically hold by a 3 mm thick Carbon Fiber structure made out of 10 Carbon/Epoxy layers, chosen in order to minimize the distortions associated to thermal gradients existing among the different parts of the Silicon Tracker [7]. The expected power dissipation amounts to about 15 W/crown which is removed by a water cooling system [8]. Each module is controlled by four voltages and four currents; depending on the expected module to module variation and sensitivity, the supply is controlled at different detector levels, for a total number of 240 monitored and supplied quantities.

The end-cap design is intended to provide a self consistent pattern recognition. Track search is performed relying on either three hits from the Silicon Tracker detectors or two hits compatible with a track element reconstructed by the external tracking chambers. In both cases, the track candidate is constrained by the beam spot, reducing the number of fake associations. The tracking efficiency improvement in the forward region is shown in fig. 2 for particles in two momentum ranges.

3 THE PIXEL DETECTOR MODULE

The layout of a module, manufactured by CSEM[1)] , is shown in fig. 3. It consists of 8064 squared pixels of 330 μm pitch, DC coupled to the readout electronics. The active area is subdivided in ten regions of 24×24 pixels and six regions of 24×16 pixels, corresponding to the 16 readout electronics chips. Pixels at the boundary between neighbouring chips have increased dimensions, so that blind regions in the active area are avoided.

Bus lines bringing the I/O signals to each of the chips have been integrated on the detector substrate by a double metal process. This design has the advantage of avoiding any extra material beyond the detector and the VLSI, allowing at the same time a reduction in the amount of signals by multiplexing on the integrated bus. On the other hand, it is a highly demanding design, both in terms of failure rate of the interconnection technique and detector testing. In fact, it should be considered that the connection between the bus lines and the corresponding I/O pad on the chip is achieved by the same bump bonding technique used for the pixel interconnection. Since each chip requires 27 I/O signals, in order to achieve a production yield above 80% a bonding failure rate below 5×10^{-4} is required. The current results obtained with the IBM C4 bump bonding process [9] are reported in section 5, while results from alternative low cost techniques pursued inside the DELPHI Silicon Tracker collaboration are reported in [10] and [11]. The identification of either interrupted lines or short-circuits in the integrated bus has been achieved measuring each line capacitance with a C-V meter operating at 100 kHz and an automatic probe station, for a total number of 608 measurements per detector [12]. Over a sample of 294 detectors, 3 had interrupted lines, 21 had short-circuits, 9 were rejected because of a leakage current exceeding 10 μA and finally 3 detectors had both a high leakage current and bus faults.

4 THE FRONT END ELECTRONICS

The readout electronics has been described in detail elsewhere [13]. A block diagram of the front end analog cell is shown in fig. 4. It consists of a charge folded cascode preamplifier with 10 fF feed back capacitor, a RC-CR shaping filter with 200 ns peaking time, a discriminator and a 1 bit memory. On two cells per chip, a p well underneath the input pad defines a 30 fF calibration capacitance. Because of the large number of pixels and the expected low occupancy, a selective readout scheme has been implemented on chip [14], identifying and outputting the addresses of the hit pixels at 7 MHz rate.

The detector efficiency is essentially determined by two parameters: the number of noisy pixels to be masked out and the discriminator threshold level, defining the detected minimum signal amplitude. A standard figure of merit for the chip performances is defined by the threshold level for 1% noisy pixels. The measured mean value for chips bonded to a detector is 7800 electrons, with a dispersion of 1200 electrons r.m.s.. The detection efficiency versus the threshold level was estimated using a dedicated simulation, verified in a test beam for several incident angles. Results for detectors in the DELPHI geometry are shown in fig. 5. It is clearly seen a detection efficiency above 99.9% is retained till threshold values around 10000 electrons, corresponding to a 0.12% measured mean level of noisy pixels.

The assembly of the 152 detectors needed for the DELPHI Silicon Tracker requires 2432 electronics chips. About 5000 chips were produced and sorted after the solder bump deposition, using a probe card with 30 flexible Copper-Berillium needles with convex tips. The tests are automatically carried out in two stages. In the first step, chips are selected checking the power consumption , the selective readout logic, the minimum threshold level and each cell response in a low threshold regime. So far, the yield on 44 wafers (3652 chips) is 59%. In the second step, the input impedance of the control currents is measured. Since control currents are bussed per module, the chips have to be sorted according to equal input transfer characteristics, in order to avoid having unequal working points. Sorting can be done without significant loss of available chips.

[1)] CSEM, Rue de la Maladiére 41, CH 2007, Neuchatel, Switzerland

5 MODULE ASSEMBLY

The module assembly proceeds through different steps, shown in fig. 6:

• interconnection between the detector and the 16 electronics chips. It has been carried out at IBM, relying on their patented C4 (Controlled Collapse Chip Connection) processing [9], growing lead-tin bumps about 100 μm in diameter and 30 μm high. A measurement of the bump bonding failure rate has been performed testing the assembled detectors response to a $^{90}Sr\beta$ source and identifying dead pixels. According to this procedure, we can state a $(2.4 \pm 0.2) \times 10^{-4}$ failure rate. Beyond the random failures on the pixel interconnection, 20% of the modules were rejected after chip flipping, mostly because of either errors in the selective readout or increased reverse current;

• glueing of a 300 μm thick ceramics support at the slim end of the module, in order to allow a precise mounting on the crown and provide a good thermal coupling to the cooling system. The Silicon sensitive area edges are then surveyed with 5 μm precision with respect to the ceramics [15];

• glueing of a 4 layer flat Kapton on top of the readout chips, carrying supply and depletion voltages;

• glueing of a pre-shaped multilayer Kapton, routing signals and supplies between each module and the repeater electronics, located on rings outside the Silicon Tracker acceptance. The Kapton is 460 μm thick and about 16 to 32 cm long, depending on the module position;

• wire bonding between the long and flat Kapton and to the detector, carried out by a semi-automatic bonding machine.

After the assembly, final tests on the detector quality are performed. Using a PC controlled set-up, based on CAMAC and LabVIEW software [16], each module is fully characterized, both performing electrical tests and assigning the mask of noisy and dead pixels.

So far, 204 detectors have been assembled; 80% were accepted after bump bonding and chip flipping. After wire bonding, a number of short-circuits between power lines were observed. As there were no visible short-circuits between individual bond wires, these are suspected to be due to pin-holes introduced during bonding connecting power lines close to the bond pads. This unforeseen problem lead to a 30% loss of modules.

6 CONCLUSIONS

The main characteristics of the pixel detector designed for DELPHI have been described and progresses in its construction have been reported. Currently, 5/8 half crowns have been mounted, tested and ready to be installed in DELPHI for the 1996 run.

7 Acknowledgements

We are greatly indebted to R. Campagnolo, L. Maggi and M. Scarpa for their skill and dedication during the module tests.

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Figure Captions

fig.1 A schematic view of the DELPHI Silicon Tracker

fig.2 Tracking efficiency versus polar angle in the forward region, with (solid crosses) and without (dashed crosses) the Silicon Tracker, for particles with momenta below $4GeV$ (a) and above $4GeV$ (b)

fig.3 Layout of the DELPHI pixel detector module

fig.4 Block diagram of the analog front end cell

fig.5 Detection efficiency versus threshold (in electrons) for the DELPHI pixel detectors

fig.6 A sketch of the different steps in the module assembly

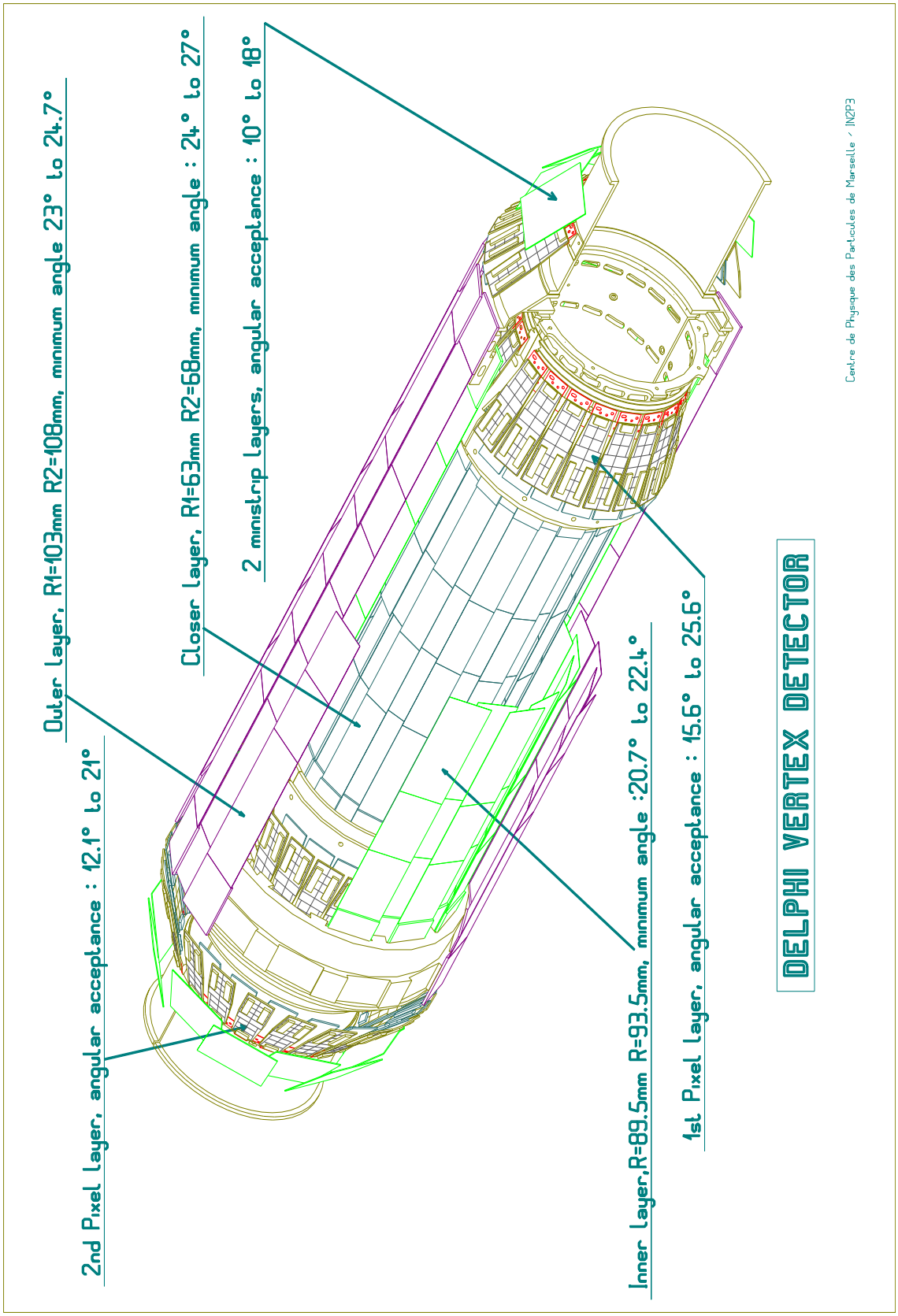

Figure 1: A schematic view of the DELPHI Silicon Tracker

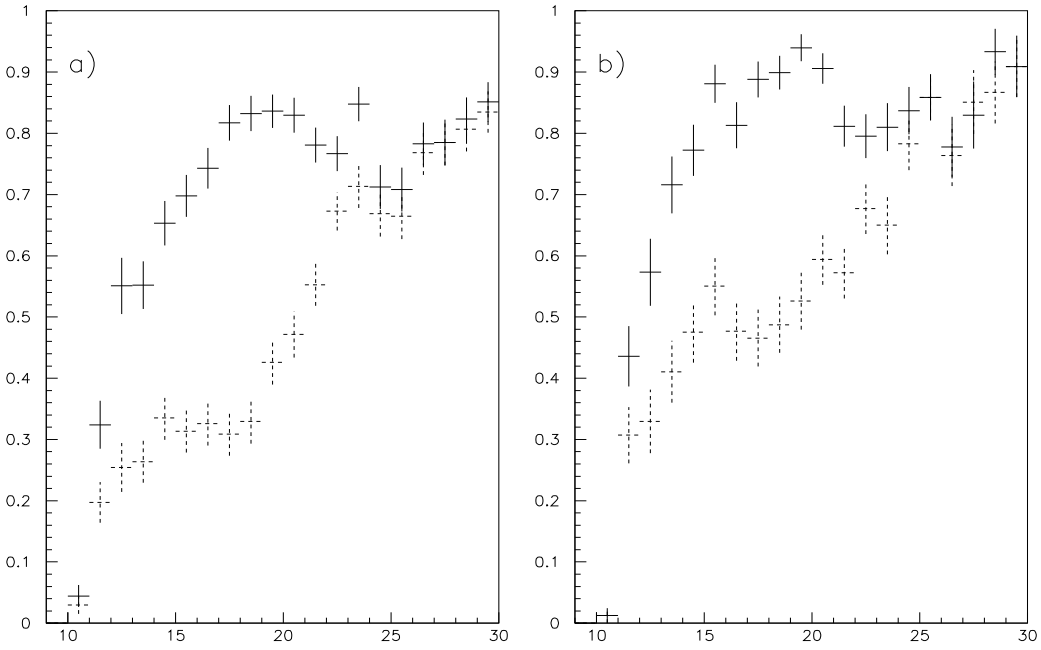

Figure 2: Tracking efficiency versus polar angle in the forward region, with (solid crosses) and without (dashed crosses) the Silicon Tracker, for particles with momenta below 4 GeV (a) and above 4 GeV (b)

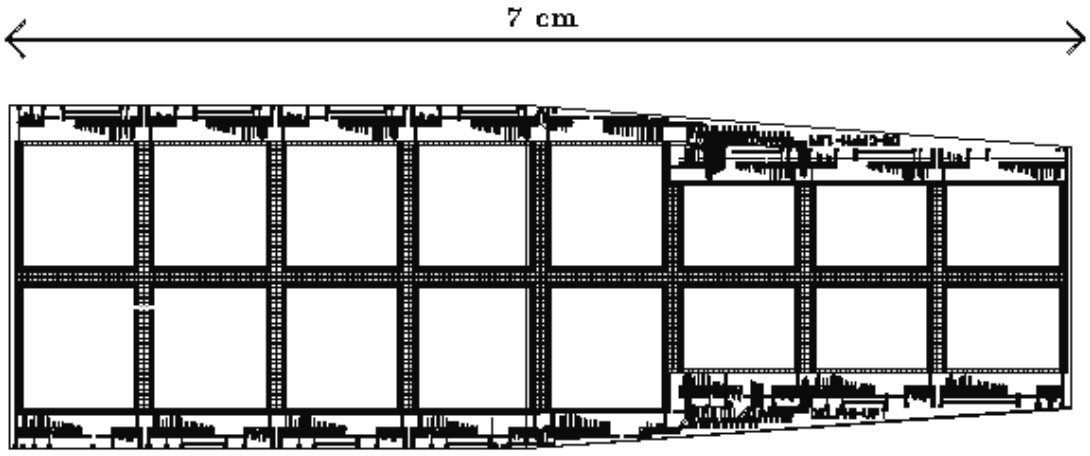

Figure 3: Layout of the DELPHI pixel detector module

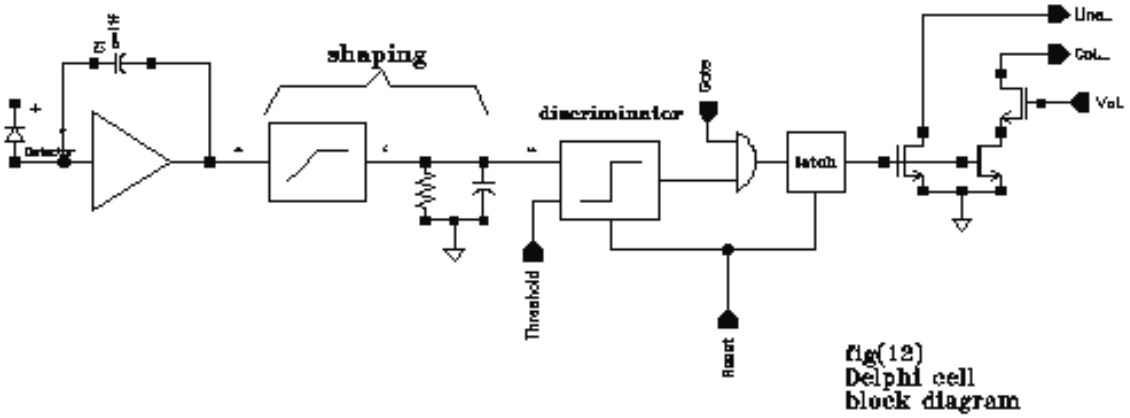

Figure 4: Block diagram of the analog front end cell

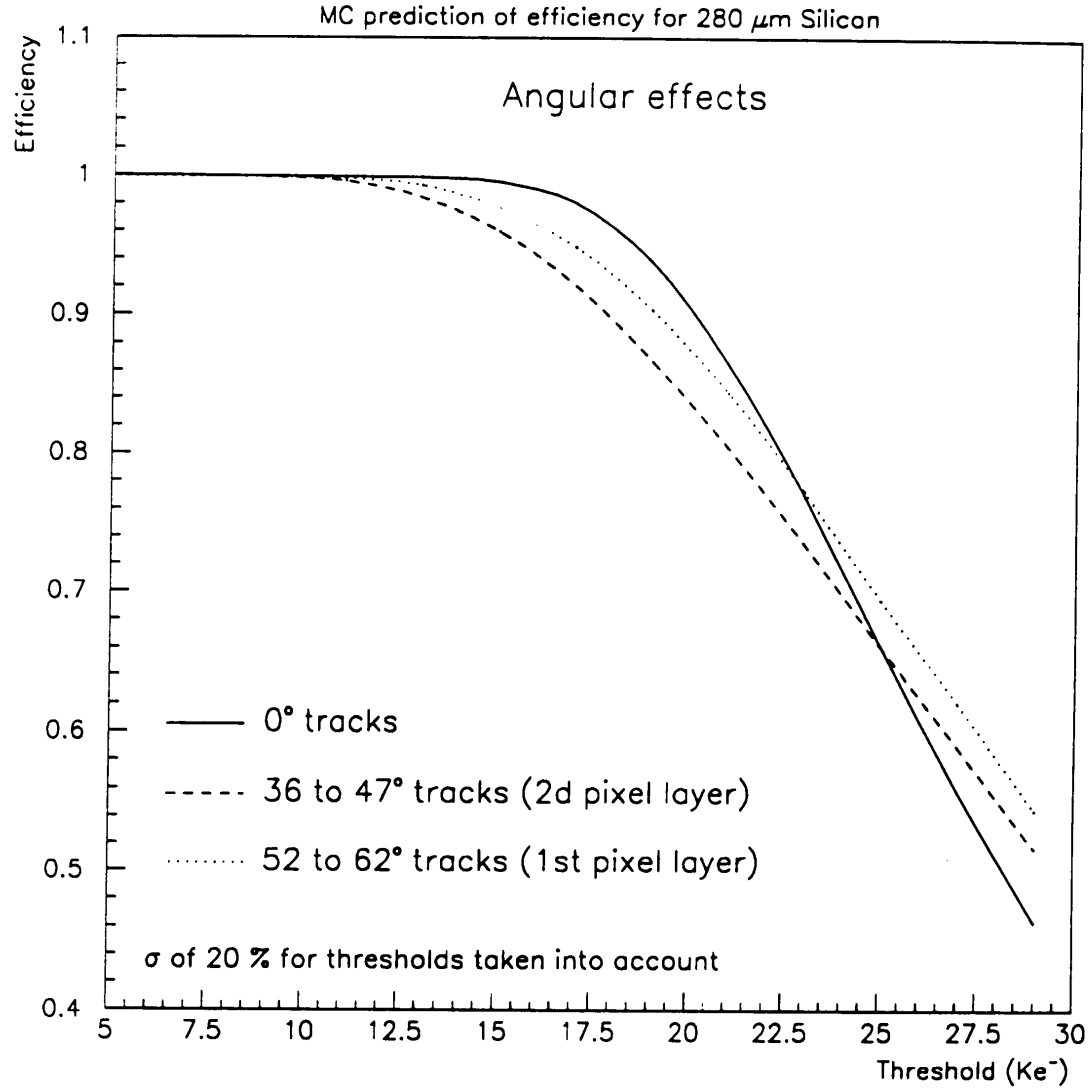

Figure 5: Detection efficiency versus threshold (in electrons) for the DELPHI pixel detectors

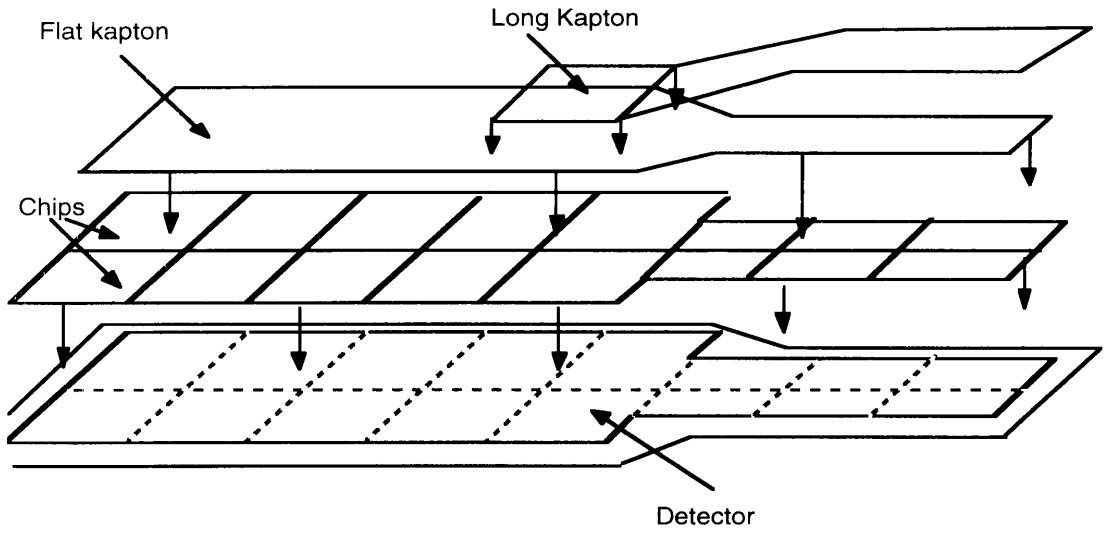

Figure 6: A sketch of the different steps in the module assembly