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PERFORMANCE VERIFICATION OF NEW MACHINE PROTECTION SYSTEM PROTOTYPE FOR RIKEN RI BEAM FACTORY

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Abstract

We herein report on the performance verification of a new machine protection system prototype for the RIKEN Radioactive Isotope Beam Factory (RIBF) and on the study to improve its performance. This prototype has been developed to update the existing beam interlock system (BIS) that has been in operation since 2006. The new system, as was the BIS, was configured using programmable logic controllers (PLC).

We applied the prototype to a small part of RIBF and started its operation in September 2020. It consists of two separate PLC stations, has 28 digital and 23 analog inputs as interlock signals, and has five digital outputs used to stop a beam. The observed response time averaged 2 ms and 5.4 ms, within one station and with both stations, respectively. When deploying the prototype at the same scale as the BIS, which consists of five PLC stations with roughly 400 signals, the resulting performance would barely meet our requirements. Further, there is a risk that the system cannot protect the hardware when the beam intensity of the RIBF becomes higher. Therefore, we are redesigning a system by adding field-programmable gate arrays to significantly shorten the response time, rather than repeating minor improvements to save a few milliseconds.

INTRODUCTION

The RIKEN Radioactive Isotope Beam Factory (RIBF) consists of two heavy-ion linear accelerators and five heavy-ion cyclotrons. One of the linear accelerators is mainly used for experiments to search for super heavy elements, whereas the other is used as an injector to the cascades of the cyclotrons used for nuclear physics, material science, and life science applications. The cyclotron cascades can provide the world's most intense RI beams over the entire atomic mass range by using fragmentation or fission of high-energy heavy ions [1].

The components of the RIBF accelerator complex (such as the magnet power supplies, beam diagnostic devices, and vacuum systems) are controlled by the Experimental Physics and Industrial Control System (EPICS) [2] with a few exceptions, such as the control system dedicated to RIBF's radio frequency system [3]. However, all the essential operation datasets of the EPICS and other control systems were integrated into an EPICS-based control system [4]. Additionally, two types of independent interlock systems are operated in the RIBF facility: a radiation safety interlock system for human protection [5] and a beam interlock system (BIS) that protects hardware from high-power heavy-ion beams [6].

BIS OVERVIEW AND DEVELOPMENT OF NEW MACHINE PROTECTION SYSTEM

The BIS began operation in 2006, along with the beam commissioning of the RIBF. Figure 1 shows the hardware configuration and process flow of the BIS, which was developed based on Melsec-Q series programmable logic controllers (PLCs) [7]. It was designed to stop beams within 10 ms after receiving an alarm signal from the accelerator and beam line components. Upon receiving an alarm signal, the BIS outputs a signal to one of the beam choppers, which immediately deflects the beam just below the ion source. It also inserts one of the beam stoppers (Faraday cup) installed upstream of the problematic component. The BIS ignores the problems that occur downstream of the beam stopper insertion point. After inserting the relevant beam stopper, the beam chopper can be switched off, and the beam delivery can resume up to the inserted beam stopper. This feature is particularly important because if the problematic component cannot be recovered within a short time, the problem recovery time can be effectively used to readjust the beam to the inserted beam stopper. The inserted beam stopper can then be extracted from the beam line after the problem is fixed.

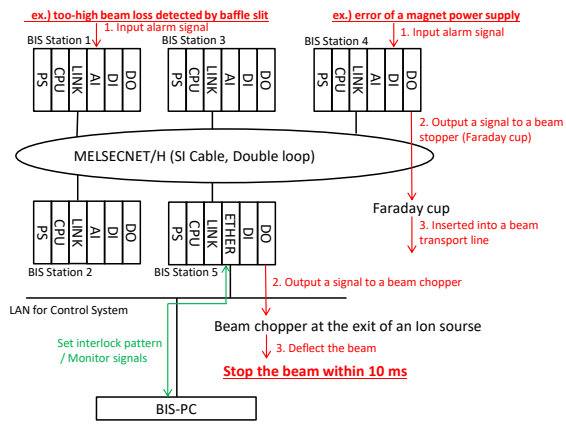

Figure 1: Example of the hardware configuration and process flow in the BIS. The green line signifies communication via Ethernet.

The BIS is still under stable operation; however, its maintenance has become gradually difficult because some

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of the modules used in the system are discontinued and cannot be replaced. Additionally, the performance of the system has been declining owing to the increasing interlock signals input to the system during the 15-year developments of RIBF. The measurements performed in summer 2020 show that the average response time of the BIS, the time from when the system receives the interlock signal to when the beam is stopped is approximately 18 ms, which is greater than 10 ms, the system response time that was originally required. A response time of 10 ms or less is required to operate higher-power beams more safely in the future. Therefore, we have been developing a successor system to the BIS for a few years and attempted to apply the prototype to a small part of the facility: the AVF cyclotron and its low-energy experimental facility (AVF-BIS) in summer 2020.

The hardware constitution and process flow of the prototype and modules used in the prototype are summarized in Fig. 2 and Table 1, respectively.

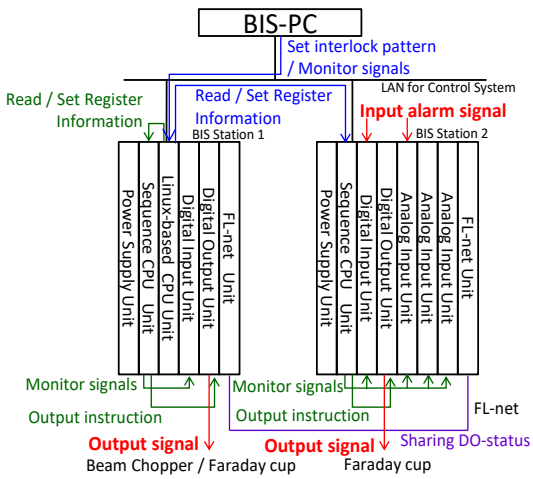

Figure 2: Hardware constitution and process flow in the prototype. Blue lines represent communication via Ethernet, green lines represent communication via PLC bus, and purple lines represent communication via FL-net.

Table 1: FA-M3 Modules Used in the Prototype

Type	Product	Note
CPU1	F3SP71-4S	Sequence CPU
CPU2	F3RP61-2L	Linux-based CPU
DI Module	F3XD32-3F	
DO Module	F3YD14-5A	Transistor contact
AI Module	F3AD08-1V	
FL-net Module	F3LX02-1N	Transmission speed: 10 Mbps

To develop the prototype, instead of adopting the Melsec-Q series PLC following the BIS, we adopted the FA-M3 series PLC, a product of Yokogawa Electric Corporation, which is widely used in RIBF control systems [8]. Details of the prototype were reported previously [9].

A new advantage of the prototype is that it utilizes two different types of central processing units (CPUs): the sequence CPU and Linux-based CPU. The former is dedicated to high-speed signal processing such as beam stop after receiving an alarm signal, whereas the latter mainly handles tasks that do not require high-speed response, such as the parameter setting of the interlock system. The introduction of the latter reduces tasks for the former, and a reduction in the response time is expected. We set up a prototype comprising two PLC stations: one with a Linux-based CPU and a sequence CPU installed in a location close to the ion sources, and the other with a sequence CPU installed in the location where wiring of various input signals was gathered. The communication between the two stations is performed through FL-net (an open network protocol used for interconnection between controllers) using dedicated wiring [10], and the signal setting and monitoring are performed by the terminal in the control room via Ethernet. In the AVF-BIS, 28 digital inputs and 23 analog inputs were used as interlock signals, and five digital outputs were used to stop the beam.

As a result of the oscilloscope-measured signal response speed in the AVF-BIS, the observed response time averaged 2 ms and 5.4 ms, respectively, within one station and with both stations. Figures 3 and 4 depict examples of the measurements, in which the yellow and green lines show the input and output signals, respectively. In Fig. 3, the signal is input to BIS station 1 in Fig. 2 and the output from BIS station 1. In Fig. 4, the signal is input to BIS station 2 and the output from BIS station 1. For both measurements, the oscilloscope was connected to BIS station 1. Therefore, in the measurement shown in Fig. 4, a cable is temporarily laid from BIS station 2 to the oscilloscope placed beside BIS station 1, and the signal is input to BIS station 2 and at the same time input to the oscilloscope via the cable.

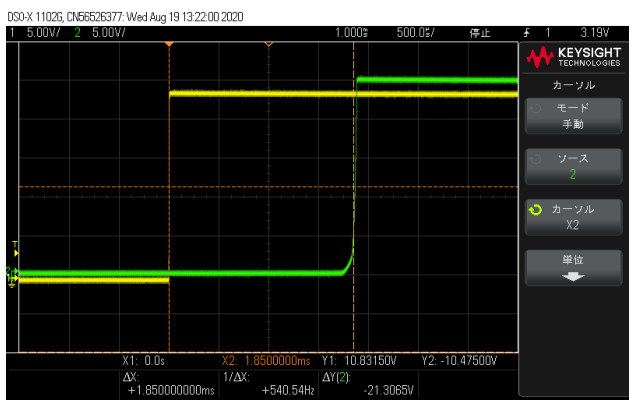

Figure 3: Signal output timing at AVF-BIS (within the same station, 1.85 ms).

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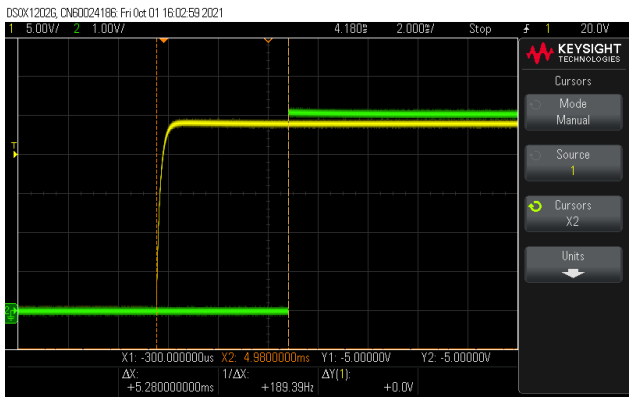

Figure 4: Signal output timing at AVF-BIS (between separate stations, 5.28 ms).

The average response time was obtained as 1.4 ms and 3.8 ms for the operation within one station and using two stations, respectively, in the test involving two stations side by side before installing the prototype as AVF-BIS [11]. The results of the two aforementioned measurements show that the signal response time increases after the prototype is installed as the AVF-BIS. There are mainly two differences before and after installing the prototype as AVF-BIS: one is that the distance between two stations increases from side by side to approximately 70 m, and the other is that the length of the program executed on the sequence CPU increases by approximately 1.2 times in the AVF-BIS as compared to the measurement in the prototype. However, these reasons are not sufficient to explain the difference in the response time, and details of the cause are currently under investigation.

The measurement result of the response time was sufficient for the performance of the AVF-BIS. However, scaling up the prototype to a system consisting of five PLC stations with approximately 400 signals, similar to the existing BIS, it is estimated that the response time of the system will be long because the transmission time varies depending on the number of stations. According to the data released by Yokogawa Electric Corporation, when the number of stations in the system increases from two to five, the signal transmission time is almost doubled under the condition that the size of the transmitted data is the scale of the AVF-BIS. Because the ratio of the transmission time to the response time between two stations is under investigation and is not currently clear, it is not possible to accurately estimate the response time of the system when the AVF-BIS is expanded to five stations. However, we reckoned that it was necessary to consider the possibility that the performance required for the system could not be achieved with a sufficient margin in the expansion of the current system using the sequence CPU and FL-net. Therefore, we began to redesign the system.

To reduce the signal transmission time in the stations, we opted to use a twisted cable. Additionally, to further shorten the response time, we plan to introduce a field-programmable gate array (FPGA) to process interlock signals as fast as possible in the new system. Because the signal propagation speeds of the twisted cables range from 4.5 to 5.5 ns/m, the response speed of the new system is expected to be an order of magnitude faster than the existing BIS.

DEVELOPMENT OF FPGA-BASED MACHINE PROTECTION SYSTEM

In the development of a BIS system using FPGAs (hereinafter, FPGA-BIS), the method of stopping a beam to protect the machine is basically the same as that of the BIS and AVF-BIS. In the AVF-BIS, which has been improved based on the operational experiences of the BIS, the system response time was successfully reduced using two types of CPUs according to the required processing speed. Therefore, we also properly use FPGAs and CPUs according to the signal processing time required in FPGA-BIS, which will be used to evaluate various interlock conditions imposed on each input signal as fast as possible. For example, we require a certain duration time for some interlock signals to avoid false alarm signals originating from the malfunction and/or noises of the system. Furthermore, the BIS should stop the beam only when an alarm signal is output from the device upstream of the beam stopper inserted in the beam line. By executing these condition judgements on the FPGA, we expect that the high-speed processing of signals in the system is realized. However, CPUs constantly execute processing such as setting signal parameters and monitoring signals indicating the state of the beam stopper. As in the case of the AVF-BIS, the EPICS will be executed on the CPU.

Each station that composes the FPGA-BIS will be installed at or near the existing BIS station to maximize the reuse of the existing signal wiring of the BIS. Therefore, the stations are widely distributed in the facility as well as in the BIS.

To achieve the performance required in FPGA-BIS, we are now studying two systems as candidates: FA-M3 series PLC by adding input/output (I/O) modules with an FPGA (FPIO module) [12], and CompactRIO, a product by National Instruments [13]. The FPIO module (F3DF01-0N) was equipped with an FPGA and had 24 input contacts and 24 output contacts. The advantages and disadvantages of each system are as follows.

- The advantage of the FA-M3 PLC system is that it is familiar with its operation because it is widely used in the RIBF control system. Additionally, because each FPIO module has an FPGA, the processing of the input signal can be closed in the module, thus, the system can be expanded simply by adding the FPIO module (there is no need to coordinate with other FPIO modules).
- The disadvantage of the FA-M3 PLC system is that the total cost increases. The FPIO module is more expensive than a normal I/O module; however, many FPIO modules are required because all alarm and output signals that require high-speed processing need to be connected to the FPIO module. Another concern is the duration of maintaining the present FPIO module that uses Spartan 6 FPGA, the release of which was more than 10 years ago.

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- The advantage of the CompactRIO system is that the total cost can be reduced (estimated to be approximately half that of the FPIO system). In the CompactRIO system, an FPGA is mounted on the chassis instead of individual modules, thus, normal I/O modules can be used to connect the signals even if they require high-speed processing. Additionally, LabVIEW can be used to develop FPGA logic [14], and even if the FPGA is updated to a new one, it is not necessary to recreate the logic once it is developed on LabVIEW because it is expected to absorb the difference between different FPGA versions. LabVIEW is widely used in various systems at the RIBF, so it is familiar to us as well as the FA-M3 PLC system. Furthermore, the machine protection system using CompactRIO has been in operation for more than 10 years at one of the core experimental facilities of the RIBF and can be used as a reference, although the system scale is different [15].
- The disadvantage of the CompactRIO system is that it is necessary to recompile the FPGA logic whenever the number of signals handled by the system increases and new modules are added.

We are currently preparing to build prototypes for both the systems. After testing both prototypes, we selected the FPGA-BIS. We aim to replace the BIS with the FPGA-BIS within 2 years.

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