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Review

Silicon spin qubits: a viable path towards industrial manufacturing of large-scale quantum processors

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Abstract Based on silicon, modern computers are engineered and manufactured using advanced Very-Large-Scale Integration technology (VLSI). After significant progress over a series of decades in controlling silicon-based spin qubits, researchers recently demonstrated that good spin qubits can be made out of silicon nanocircuits using the same advanced VLSI technology. This means that it may be possible to leverage all the knowledge of VLSI technology to efficiently build the future of large-scale quantum machines. In this review, we will survey the recent developments in silicon spin qubits and discuss the challenges that remain for building silicon quantum machines.

1 Introduction

In the past few years, significant progress has been reported in the field of quantum computing. It is now possible to access the first prototypes of quantum computers. They rely on different platforms, and most of them are based on technology developed in academic labs over the span of many years. At the individual quantum object level, their coherence properties have been studied intensively by the physics community for the past four decades. Having proven that quantum computing is possible, researchers' attention has now turned towards the problem of scaling these systems into larger quantum machines while respecting the specificities of each qubit platform. Thus far, they have succeeded in developing quantum machines with upwards of one thousand qubits [1]. As a result, the algorithmic community is now leading an important research effort focused on identifying user applications for Noisy Intermediate-Scale Machines (NISQ) with limited calculation depth [2]. The goal of this research is to demonstrate the potential advantage of quantum machines on algorithmic applications at this scale [3].

Current research is also centered around larger-scale quantum machines, which have the potential to reach regimes where the gains in quantum calculation become significant. This type of system would require the implementation of error correction protocols which, themselves, are quite greedy in terms of physical qubits. Some estimate that larger-scale quantum machines would need over 1 million qubits [4]. Successfully reaching these regimes presents extraordinary challenges, both in terms of the technology itself as well as the underlying physics. It begs two questions: first, is it feasible to control million-qubit machines? Second, is it feasible to maintain the coherence in such large quantum systems while performing millions of operations? Answering these two questions will be crucial to successfully developing future large-scale quantum machines. As it stands, the prospects for large-scale quantum machines are strongly debated and vary from system to system.

In relation to these two questions, silicon spin qubits have a potential advantage over other qubit platforms. This is why there are significant research efforts underway to understand their coherence properties and to increase the number of controlled qubits. Robust and low-error, silicon spin qubits have a small footprint (below 1 μ m^2) and can be operated at relatively high temperatures (above 500 mK) [5,6]. Based on these facts, they present a potential path towards scalability. Having identified this potential, there have been attempts at keeping qubit manufacturing technology as close as possible to the technologies used in industrial nanofabrication facilities for the fabrication of classical processors, as this is the only technology that has proven to be scalable to a million objects and above. This would provide the added benefit of compatibility between classical and quantum circuits, poten-

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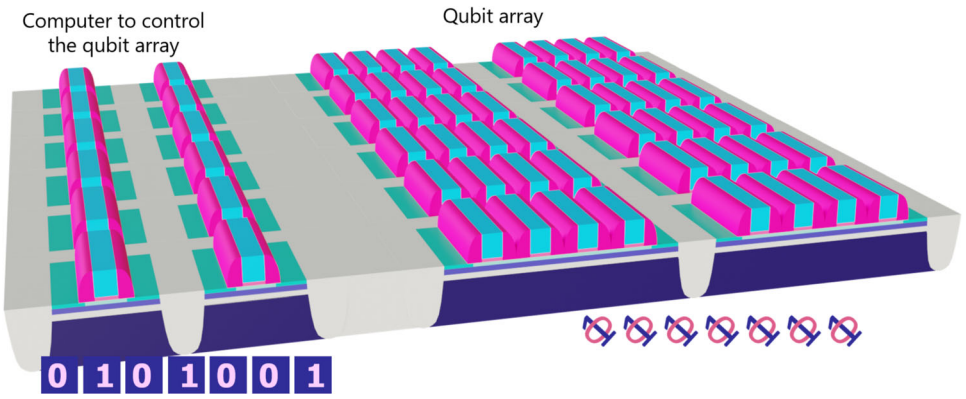

Fig. 1 Schematic diagram of the monolithic co-integration of quantum (right part) and control (left) systems in FD-SOI technology

tially leveraging the co-integratibility of quantum and control units, working at the same temperature and paving the way to large-scale control (see Fig. 1).

Despite obvious advantages, the use of existent technologies for scaling up qubit systems comes with constraints and the belief that the use of silicon spin qubits in it of itself would be enough to channel the scaling advantages of the semiconductor industry would be naive. Decades of technological developments within the semiconductor industry itself provide important insight into the technological path towards scalability, as well as the costs associated with the development of such technology. In CMOS, innovative modules (such as High-K/Metal Gate (HKMG) or liner stressors) require, on average, more than 11 years to make it from concept to manufacturing [7] and the complete FDSOI journey from proof-of-concept to industry took more than 30 years. To truly achieve large-scale semiconductor-based quantum computing within a short time scale, there seems to be little choice but to marginally customize existing manufacturing technologies. On a more fundamental level, the very reason why CMOS technologies have mastered the 0.1nm scale in terms of thickness, or the nm scale in terms of critical dimensions, or even ppm in terms of the chemical composition, is by virtue of large-scale reproduction where the same processes are being used over and over on tens of thousands of wafers. When applied to quantum computing, though the control needs are the same, the materials, dimensions and geometries diverge, and therefore one can surmise that the same amount of wafers would be needed to reach a similar level of precision. As it stands, the size of the quantum computing market does not justify such a heavy investment. So, once again, the argument must be made for marginal modifications on existing technologies. Doing this is not straightforward because, while CMOS technologies have been optimized for large amounts of carriers at room temperature, silicon qubits require single charges at low temperature. Thus, several strategies, at different maturity readiness levels (MRL), for customizing existent technologies are being explored in parallel, in order to both understand the underlying physics and identify what customization would be needed for industrial CMOS.

The goal of this survey is fourfold: to provide insight into the different approaches being used for realizing silicon spin-based quantum processors, to identify their relationship to industrial efforts in microelectronics, to provide a summary of each approach's main achievements and, finally, to discuss some of the scalability challenges for quantum systems.

2 Spin qubit platforms

Due to its strong technological potential and relatively low maturity with respect to other qubit platforms, a diversity of approaches are being explored in order to produce semiconductor qubits (see Fig. 3). The most advanced demonstrations are currently being produced in academic lab facilities, and entail quantum circuit processing with recipes not used in advanced VLSI technologies. The main achievements have been: the implementation of processors with up to 6 qubits [8], the consistent entanglement of up to three qubits [8,9] and the investigation of some of the first protocols for quantum error correction with spin qubits [10]. In parallel to these developments, qubits manufactured within the parameters of industrial flows have also been explored and demonstrated, therefore setting the stage for large-scale integration[11,12]. In this section we will review the various platforms associated with semiconductor quantum circuits.

The basic element that carries quantum information in a semiconductor is the elementary charge located at the semiconductor/semiconductor (semiconductor quantum well) or semiconductor/insulator interface. In this configuration, charges are confined to the normal direction on the interface and their motion is therefore planar. The definition of the qubit relies on charge being trapped in a quantum dot, for which many procedures have already been investigated (self-assembled quantum dots, electrostatic dots, vertical dots). Close attention was given to electrostatically defined quantum dots where the gates, nanofabricated on top of the semi-

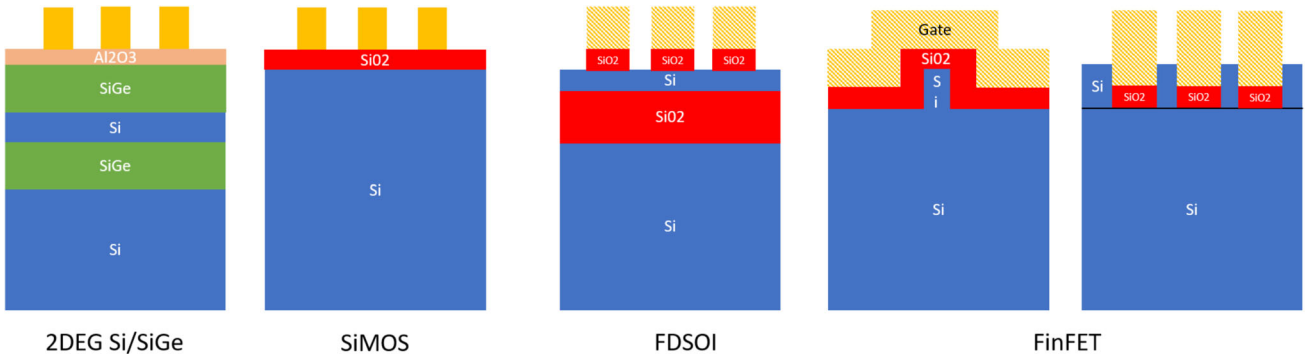

Fig. 2 **a** Schematic representation of the different platforms for Silicon spin qubits. From the left to rigth, the first two (2DEG and SiMOS are the one having been used to realize quantum devices in academic labs. The remaining two are the closest to the process flow used in advanced VLSI platforms, for high throughput realization of the processors. A color-coded is used for the different materials used in the process: Si (blue), SiGe (green), SiO_2 (red), Al_2O_3 (pink) and gate stack material (orange). The texture of the gate stack material in the representation stresses the difference in academic and advanced VLSI flows, respectively metallic (Al, Pd, Au etc..) and TiN/Poly Silicon

conductor structure, were polarized to engineer and control the associated confinement potential. A multi-gate layout was necessary to define an egg-carton-like electrostatic potential for the several charges necessary in order to define the multi-qubit processor. Barriers separating quantum dots and the respective potential of each quantum dot were controlled by the voltage applied on the gates. In this way, the spin qubit processor platform mimicked a famous problem in condensed matter physics, the Fermi Hubbard model. The associated phase diagram and spectrum at large numbers of sites were identified as a complex problem to solve on a classical computer [13].

As far as dimensions are concerned, the typical gate pitch fixes the distance between two quantum dots and is mostly dependent on the charge effective mass, a parameter defining the size of the charge within the trapping potential. A heavier charge means a smaller pitch, in order to allow tunneling between two dots. Typically, it varies from 60 nm (for heavy effective mass) to 120 nm (for lighter ones). For an analogy with advanced CMOS process, these pitches correspond to 10 to 32–28 nm node and are only available in the advanced VLSI foundries but do not correspond to the most advanced (and thus most complex and expensive) CMOS processes.

All these descriptions point to the necessity for the quantum dots to be solely defined by their electrostatic potential. However, if disorder potential is induced by charges on insulators, or if defects in the semiconductor layer are too strong, this observation is no longer valid and control of the charge position becomes more difficult. Therefore the amplitude of the disorder potential in the low charge density regime should be reduced compared with the potential induced by the gate voltage. This compromise is at the heart of how semiconductor qubits function and is an important figure of merit in semiconductor quantum devices.

For most of the advanced work in academic labs, researchers use two-dimensional electron gas (2DEG) of different materials to allow for robust electrostatic charge trapping. In electronics, these layered semiconductor materials have been investigated to decrease disorder and nanostructure resistivity, by increasing as much as possible the charge mobility. It is done by separating the gates and the charge carriers using epitaxial heterostructures. Not surprisingly, disorder potential is reduced at the price of a reduced gate lever arm (capacitive gate effect on the charge trapped in the quantum dot). This compromise opens a very effective window for manipulating charges electrostatically in quantum dot arrays. This is especially true for semiconductors with the light effective mass of the carriers, which affords the use of relaxed gate pitch [14]. Nevertheless, these systems, though of high interest for initial scientific demonstrations, present significant technological limitations in terms of scalability. Not least of which, because they are sensitive to high temperature thermal annealing (above 750°C) that leads to interdiffusion between layers. In regular CMOS technology, for yield and performance reliability, gate stacks require annealing above 800°C. From that perspective, though they rely on materials similar to those of CMOS technology (Si, SiGe, Ge), the process needed for scaling would require drastic adjustments with respect to advanced industrial CMOS fabrication flows. Such adjustments are currently being investigated within advanced CMOS R&D centers, with a recent demonstration performed on a 12 qubit quantum processor [15].

This is the reason why the spin-qubit community invested quite a bit of effort in the development of qubits with charges trapped at the interface between Si and SiO_2. In this case, the disorder potential is greater but the distance between the gates and the charge is reduced significantly. It gives rise to a second lever arm-disorder window for the control of spin qubits. Academic labs with non-VLSI gate stack techniques

(metallic gate and lift-off fabrication recipes) have demonstrated high fidelity in quantum operations up to two qubits. Interestingly, inversion charges located at the Si-SiO2 interface are the basic elements of VLSI technology and used for the most advanced electronic circuits with 300 mm fabrication tools (namely, FinFet and FD-SOI). This same technology has been demonstrated to work on qubit fabrication [11,12]. To do this, heating processes and specific gate stacks for high-yield and reproducible performances were reused. In SOI architecture, the back bias (Vbb) can be leveraged to move the carriers away from the interface. We have demonstrated that it allows for a decrease in the charge noise by a decade [16], thus decreasing the sensitivity to any disorder coming from the interfaces or the dielectrics. All this taken into account, it is worth noting that the development of qubits within the constrains of an industrial process are still currently lagging behind the work being done by academic research groups.

3 Types of spin qubits

Semiconductor quantum processors are based on quantum dot arrays with control of the dot potential and the tunneling process between dots. In addition, they must include charge detection to probe the qubits and excitation antennae for qubit radio frequency manipulation. Even though the degree of freedom of the charge was considered in the early days for storing quantum information, researchers quickly realized that spin had more potential. Spin is indeed, to a large extent, separated from the charge properties and therefore protected from the strong electrical disturbances occurring in semiconductor devices. To store quantum information, the spin of the charge carriers in quantum dots turns out to possess extremely interesting properties. Indeed, long spin relaxation [17] and coherence time [18] have been reported for individual trapped charges. As a collateral effect, this protection significantly alters the susceptibility of the spin qubits and therefore plays a significant role in qubit manipulation and detection. Indeed, one of the important challenges for the spin qubit community is to induce sufficient coupling between the spin qubits using the probe and the excitation antennae. As a consequence, the semiconductor quantum circuit community is still investigating a diversity of tactics for encoding quantum information. They differ in terms of the type of charges, the number of charges and the number of quantum dots needed to define a qubit (for example exchange-only qubits [19] or hybrid qubits [20]. At the scale of a few spin qubits, it is worth noting that gate fidelity performances are very similar for these different approaches, and it explains there is no consensus among the spin qubit community as to their preferred choice of qubit. In this survey, we will concentrate on the most prominent spin qubit being used in semiconductor quantum circuits, one that relies on a single charge trapped in a quantum dot, or the so-called Loss-di Vincenzo qubit [21]. The underlying semiconductor band structure is key to defining its spin properties and energy spectrum. The charge being a spin 1/2, the application of a magnetic field creates a canonical two-level system. A significant energy difference exists between the qubit and the other energy levels of the system (valley, orbital excited energy levels), which means that leakage outside of the qubit space can be neglected while it is being manipulated.

The most popular strategies used to manipulate qubits attempt to “dress” the spin with charge properties. In this way, spin qubits become sensitive to an electric field. Electrical driving induces a small charge displacement at the single charge level that will reflect as an effective magnetic driver for the spin. This strategy makes it possible to use low-power excitation protocols with no on-chip hardware added to the gated nanostructures. However, due to the qubit’s susceptibility to charge noise, it is worth noting that this manipulation potentially comes at the cost of reduced coherence properties. The underlying physical mechanisms are based on intrinsic or extrinsic spin-orbit coupling. Hole spin qubits are representative of the first approach [11,22]. They are both explored in the two Si platforms and are compatible with VLSI manufacturing technology. Hole spin qubits are characterized by having larger qubit energy variability, as well as no valley splitting [23]. This second approach is mainly conducted for electron spin qubits, where valley splitting is present. It entails the deposit of micromagnet nanostructures close to the spin qubit, making the spin orbit strength relatively controllable [24,25].

Approaches aimed at generating the driving field via radiofrequency magnetic fields have also been demonstrated. Because they avoid displacement of the charge, they potentially minimize electrical perturbation within the semiconductor system. They therefore preserve the intrinsic coherence properties of the qubit and the potential associated errors. It is usually more demanding in terms of excitation hardware but simultaneous excitation of qubits can be implemented both in 1D and 2D qubit array using, respectively, stripline [18,26] or magnetic cavities [27]. Nevertheless, it usually requires a strong magnetic field (amplitude close 100 μT) to reach μs-qubit driving. For the moment, this has only been applied on a single Si electron, where globally displacing the electron is relatively harmless for the spin (no spin-orbit) and the variability in terms of magnetic properties is extremely low (below 0.1%).

For these two types of individual spin qubits, coupling between qubits is local, switchable (on/off) and engineered using the process of exchange interaction. As we are going to discuss in the next section, it gives rise to controlled spin-dependent energy shifts and therefore the possibility to engineer two-qubit gates.

4 Primitive gates for spin qubits

Each qubit platform has specific roadmaps, each with their own limitations, in terms of the development of the basic quantum operations required for quantum computation. They form a set of primitive gates that are the input to quantum compilers and transpilers, a software optimization process used to identify the gates needed to perform a specific quantum algorithm. It concerns the three quantum gates (one- and two-qubit gates, measurement gate) necessary to obtain a universal set of gates. In addition, semiconductor spin qubits are special in the sense that displacing qubits is an additional functionality that could result in interesting perspectives for manipulation and scalability purposes. In the following chapter we will describe the different qubit operations, their limitations in terms of architecture and we will highlight the importance of controlled displacement within the array to engineer those gates.

To discuss the primitive gates, it is convenient to imagine the isolation of two tunnel-coupled dots in the array, each filled with one electron [28]. Each spin qubit is characterized by a specific energy difference between the two qubit levels. When the spin qubits are isolated, the qubit basis is then defined by the Zeeman hamiltonian and is up-up, down-down, up-down and down-up. Interaction between the qubits is then activated through control of the tunnel coupling between the dots. Tunnel coupling only selectively affects the spin states. It is closely related to the Pauli exclusion principle. When tunnel coupling is smaller than the energy difference between the qubits, an equal repulsion of antiparallel Zeeman spin states results, while the parallel spin remains unaffected. At higher levels of tunneling, spin eigenstates change from Zeeman to coupled spin states basis (S, T0, T+ and T-). As we will describe, these characteristics are at the heart of both the measurement gate and the two-qubit gate.

In this section, we will go over the gate principle, the states-of-the-art in terms their fidelities and speed, and analyze the maturity of each platform. In order to stay up to date with the progress and achievements of the spin qubit community, it is now possible to access a complete review of the field [29].

Spin readout and initialization

In large scale quantum computation, both initialisation and read-out gates are intensively used in the context of error correction protocols. Efficient and fast read-outs of spin states along the quantum axis can be carried out in semiconductor spin qubits, the quantum axis being defined by the applied magnetic field. In addition, following the read-out, the spin state is either preserved or known, which points towards the existence of a promising by-product of the read-out gate: a path for efficient and quick initialization.

In order to efficiently read out the charge of the spin states, the position of the charge carrier must be changed. This represents one of the main limitations of the architecture, a subject we will look at more closely in the following section. Achieving high-fidelity spin read-out in semiconductor quantum circuits is only possible thanks to two distinct physical functionalities: efficient charge detection and spin-dependent charge tunneling. First, let's discuss efficient charge detection. Information is extracted via efficient and robust charge read-out, allowing for the probe of local charge variation in quantum dots. To probe this variation, two strategies are being explored by the spin qubit community: the first strategy consists in capacitively coupling an electrometer close to the qubit. By doing this, researchers are able to detect absolute number of charges contained in the dot [30]. In the second strategy, a probe measures changes in capacitance induced by charge displacement [31]. Compared with the first option, this second is less demanding of on-chip hardware, since it only requires a gate coupled to the dot. The downside, however, is that this method of probing only accounts for charge displacement and so it is not useful for (or, capable of) detecting absolute charge. Both strategies have proven fidelity over 99%, fast timescales close to 1 μs and compatibility with radiofrequency multiplexing for simultaneous qubit read-out.

Now let's turn to the second distinct physical functionality needed for efficient read-out: spin-dependent charge tunneling, a characteristic that is critical for converting spin to charge information. It requires either a charge reservoir or a dot filled with an odd number of charges coupled to the dot containing the qubit. In the first case, the energy separation between spin states ensures spin state selectivity, meaning that only excited spin state charges may tunnel to the charge reservoir. It requires the qubit to have a relatively high Larmor frequency (i.e. relatively strong magnetic field) due to thermal broadening of the charge reservoir. The second strategy relies on the impact of the Pauli principle in a double dot configuration with two charges. In this case, only charges in antisymetric spin states may be allowed to experience charge tunneling between the dots which results in spin-dependent tunneling. Contrary to the first strategy, this second puts no condition on the magnetic field strength needed and the process could be intrinsically state-preserving. Both tunneling strategies have been demonstrated to be fast (timescale that is controlled by the tunneling process either to the second dot or the charge reservoir) and efficient, with fidelity over 99% in few μs, both in academic SiGe quantum circuits [32] and VLSI-compatible quantum circuits (FD-SOI) [33].

The initialization protocol often relies on a relaxation process that prepares the qubit in its ground state. For spin qubits, this process is rather slow and requires significant energy-splitting between qubit states compared with thermal energy $k_B T$. Potentially, this may limit the qubit processor's speed

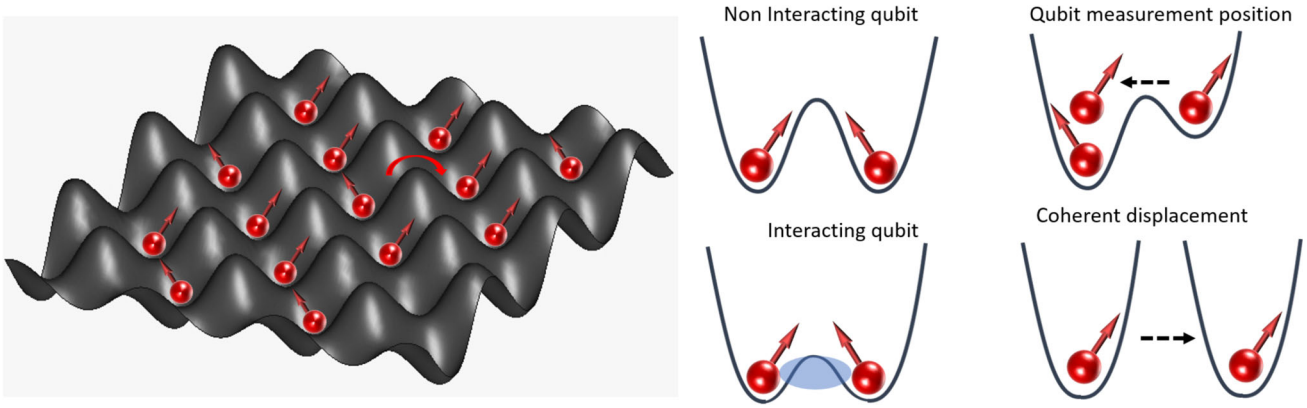

Fig. 3 Representation of the dot potential configuration when performing different primitive quantum gates. Top left: non-interacting qubits. In a double dot configuration with equal potential on both dots, two qubits are loaded and are non interactive due to the high potential barrier separating the qubits. Bottom left: In the same configuration, the tunnel barrier is lower and the qubits are closer, presenting the ideal configuration for qubit interaction. Top right: qubit measurement configuration in the so-called "Pauli Spin blockade read-out". The qubit is in the right dot, the ancilla spin needed for read-out is in the left dot. The double dot is now detuned with lower potential on the left dot. Consequently, spin-dependent transfer is occurring and results in a charge state dependent on the spin of the qubit. Bottom left: qubit displacement. The trapping potential of the qubit shifts position with the potentials applied on the gates

and operation temperature. Researchers have also experimented with initialization in two qubit ground spin states, characterized by larger energy separation to excited spin states and fast relaxation [34]. More recently, initialization after high-fidelity read-out was also proposed and quantified [8].

One-qubit gate

Inspired by NMR techniques, single qubit manipulation consists of performing controlled rotation in the Bloch sphere $R_{\mathbf{n}}(\theta)$ where $\mathbf{n}$ is the rotation axis and θ the rotation angle. For a rotation axis perpendicular to the quantum axis, it is based on the physical process called "Rabi oscillations" where the spin qubit revolution is driven via radiofrequency pulses at the Larmor frequency and oriented at a perpendicular angle to the quantum axis. The specific implementation of the RF excitation has been the subject of several different strategies discussed in the previous section. The most widely-used strategy in academic labs consists of displacing the charge on a scale smaller than the size of the dot along a magnetic gradient (electrons), or with a strong spin orbit (holes). In this configuration, fast (100ns) and efficient qubit manipulation with fidelities approaching 99.9% have been reported using $Si^{28}Ge$ in an academic setting [24]. In VLSI technology, the use of ferromagnetic micromagnets is not standard [35] and the most advanced demonstration relies on hole manipulation in FD-SOI [36]. It is worth noting that cross talk between qubits has been reported during manipulation. This tendency is heavily dependent on the type of underlying semiconductor nanostructures and the strategies that are implemented in order to compensate for them. Direct magnetic driving is compatible with VLSI technology but researchers have achieved lower precession speed (a few μs) than with electrical driving. As a consequence, high fidelity gates (over 99.9% fidelity) were obtained with pulse-shaping of the RF excitation in academic $Si^{28}-SiO_2$ quantum circuits [37]. The state-of-the-art (99% fidelity) for VLSI-compatible quantum circuits was obtained with Si^{28} FinFET technology [12], and more recently in FdSOI holes devices [38]. A great deal of work still needs to be done in order reduce the generation of spurious electric fields and thus avoid errors during the driving [39]. Finally, for rotation along the quantum axis, individual phase gates at an arbitrary angle are implemented via the fast gate control of the energy separation. The underlying mechanism is either displacing the electron within a magnetic field gradient or a change in the g-factor [18].

Two-qubit gate

Two-qubit gates are only possible thanks to the spin-dependent tunneling process. This means that, the two-qubit interaction is local in the sense that it is present between adjacent dots and can be switched on and off by controlling the inter-dot tunneling process. Such an operation results in a slight change of electron position, and, again, controlled qubit positioning enables the two-qubit gate. From a physics point of view, the interaction between two spin qubits gives rise to a controllable Heisenberg-type coupling $J(t)S1.S2)$, J being the exchange interaction. Importantly for gate implementation, the eigenbasis of the Heisenberg hamiltonian is the coupled spin basis (singlet and triplet states) and differs from the Zeeman qubit basis for antiparallel spin states.

Different regimes are possible depending on the relative strength between J and the Larmor energy difference between the qubits [28]. When tunneling is active, an energy

shift in the Zeeman spin state connected to the asymmetric state occurs. With a precise ns-control allowing adiabatic increase of the tunneling, a Controlled-Z(theta) gate is implemented with relatively low overhead in terms of manipulation hardware. Such a demonstration was used recently to reach 99.6% fidelity in 100 ns [40]. Ramping the tunneling non-adiabatically (from low to high tunnel coupling value) was also investigated for two-qubit gates. It induces coherent oscillation between antiparallel spin states and results in $\sqrt{(SWAP)}$ gates for specific time of interaction. Nevertheless, it is still today a noncompetitive option as far as two-qubit gate fidelity is concerned.

Other two-qubit gates (CNOT [25,41] or iSWAP) can be implemented by selectively driving one of the six separated transitions of the two-qubit interacting system with the Rabi oscillation mechanisms described in the one-qubit section. For CNOT operations, fidelity above 99% and with timescales below μs were reported.

For two-qubit gates, most of the state-of-art is coming from academic effort both in SiGe [40] and $Si - SiO_2$ platforms [42]. So far, the level of charge control in few-electron FDSOI/FinFet multidot structures was not sufficient due to the constrains induced by the standard VLSI manufacturing. A significant effort is pursued nowadays to understand what limits the controllability in VLSI-compatible quantum devices, with recent advancements in FDSOI [43].

Coherent displacement

We have seen that precise control of the electron's position within the semiconductor quantum device may lead to many interesting possibilities in terms of quantum manipulations. The ability to coherently displace electron spins at larger scale and on a faster timescale [44] is a differentiating characteristic for spin qubits and may open interesting paths for large-scale integration. The coherent displacement gate makes it possible to transfer the qubit between two distant dots and, ideally, with no impact on the degree of freedom of the internal spin. Nevertheless, depending on the specificity of the semiconductor's underlying nanostructure and the process used to transfer the electron [45], additional controlled rotation in the Bloch sphere could be observed and would still need to be characterized and quantified. For example, even a small spin-orbit interaction can result in the addition of an effective magnetic field, and therefore have a significant impact on spin rotation if the transfer occurs over 10 microns. Two modes for electron shuttling have been identified: multiple tunneling processes between adjacent dots and the development of moving quantum dots. At present, the two mechanisms have been demonstrated experimentally in Si quantum nanostructures, with coherent displacement up to several microns and with fidelity above 99% between two adjacent dots separated by 30nm [46] in Si-MOS nanostructures, and more recently in SiGe 2DEG nanstructures [47,48].

Decoherence

Fidelity of quantum gates is limited by the semiconductor environment in which the electron spins are embedded. For isolated spin qubits and single-qubit operations, decoherence is characterized by an important asymmetry between bit-flips and phase-flips and it explains the important gain obtained by dynamical decoupling techniques in the spin qubit community. Indeed, spin relaxation processes have been proven to be as long as several seconds for individually-isolated spin qubits [17,49]. This is closely related to the relative protection of the spin's degree of freedom from electrical perturbation by semiconductor devices (phonons, electrical noise). Coherence properties are proven to be limited by other physical processes. Indeed, the underlying presence of nuclear spins or the fluctuation in dot positions due to charge noise are the results of fluctuations in the qubit Larmor energy. Since exchange energy is inherently defined by its charge properties, charge noise is responsible for the fluctuation in two-qubit gates. Understanding the limitation and dynamics of these fluctuations is the subject of intense research [36,50]. Nowadays the coherence is characterized by timescales of several orders of magnitude below the relaxation time, approaching several tens of microseconds in purified Si^{28}. Coherence properties in academic and VLSI-compatible quantum devices have so far been proven to be comparable.

Combining these different functionalities offers a platform for quantum computation and for scaling. In Fig. 4, we summarize the performances of the different platforms. The next section will discuss the impact of the platform's constrains on the architecture of the quantum unit.

5 Architectures

Having demonstrated the ability to fulfill all the basic gate requirements for quantum computation, the spin qubit community has turned its attention to increasing the number of qubits and engineering spin-based quantum processors at intermediate and large-scale. As for other platforms, the question of scalability is a true challenge, and begs questions about the coherence and control that can be achieved and maintained at this scale. For semiconductor spin qubits, the ability to engineer a control unit and a quantum system on the same chip, in addition to the qubit's tolerance for operational temperature [22,33,37] where strong cooling capabilities are available (above 100mW), are clearly differentiating properties that need to be precisely quantified. This survey will not attempt to summarize the work being done around cryoelectronics to create such a control unit [51]. We will be

	SiGe	SiMOS	FinFet	FDSOI
Spin measurement	98% in 6μs [32]	tbd*	tbd*	99% in 4μs [33]
1-qubit gate	99.9% [24]	99.9%[37]	99.1% [12]	99.1% [39]
2-qubit gate	99.6% [40]	99.4% [42]	tbd	tbd
Coherent displacement	99% [47] (between up to five dots)	99.4%[46] (between two dots)	tbd	tbd

Fig. 4 Summary of the operation performances for the different Si Qubit platforms. tbd means "to be determined" and the addition of a star indicates that the operation has been demonstrated without fidelity evaluation

more focused on the quantum unit and we will discuss the approaches being explored within the spin qubits community for scaling up semiconductor quantum circuits.

There is a close relationship between increasing the number of spin qubits and the production of larger and larger quantum dot arrays. Most of the demonstrations so far have been realized in one-dimensional or quasi one-dimensional systems. Due to the higher charge control demonstrated in SiGe, researchers were able to demonstrate up to 12 tunnel-coupled quantum dot arrays [8,15]. In these systems, qubit operations were functional and three-qubit entanglement was demonstrated. For VLSI-compatible devices, linear and bilinear quantum dot arrays were demonstrated in FD-SOI [52,53].

Planar arrangement of the qubits is very well-suited for modern nanofabrication processes and, therefore, for semicondutor quantum devices. It provides a promising angle for the production of a two-dimensional array of quantum bits and quantum dots. Prototype devices at the scale of a few dots have been developed and tested. Nevertheless, increasing the number of dots in two dimensions for quantum computing raises concrete challenges and leaves several unanswered questions. In the following, we will discuss the main factors that may limit the quantum unit's architecture.

Initialization in deterministic filling

Contrary to superconducting qubits, spin qubit information is not stored within the circuit, but within each individual quantum particle that is precisely controlled and positioned within the quantum circuits. Similar to atomic quantum systems, it is necessary to define the qubit by applying an individual charge to the targeted dots. For state-of-the-art dot arrays, several strategies have been proposed and demonstrated at relatively small scales [54–57]. They require proper compensation of the gate's cross-talk in order to independently control each quantum dot and, more broadly, the charge pumping within the array. The path to successfully scaling these methods is still open and will strongly depend on the dot control that is available at large scale.

Number of gates to form a quantum dot

To reach the highest possible fidelity for quantum gates in semiconductor quantum circuits, control of the trapping potential for up to 2 qubits must be ensured by at least 2 gates per qubit. This has been demonstrated on a one-dimensional array, where the connectivity, defined as the number of qubits with direct coupling to one qubit, is 2. Maintaining the same strategy while taking into account a connectivity of 4, the number of gates per qubit in a two-dimensional array will increase to 3. For small-scale processors, strategies using up to 3 layers of gates separated by thin insulators allow for control of the charge configuration and make it possible to realize the first quantum operation. Nevertheless, it will quickly become a limiting factor on a larger scale. This has been identified as one of the main issues facing spin-qubit architectures. Strategies aimed at sharing gate control between dots, the so-called "line-column addressing" (see Figure) used, for example, in the production of memory within the semiconductor industry, have been proposed and are currently being explored and evaluated within the spin qubit community [55]. An important figure of merit in this context is the variability from dot-to-dot of the spin and charge properties [58].

Incorporation of spin read-out technology

In the primitive gate section, we stressed the importance of the qubit read-out. While most qubit systems extract information about the particle's state through individual qubit susceptibility [59] or by manipulating the qubit's internal properties [60], the spin qubit read-out is based on a spin-dependent change in the charge's position. Consequently, its implementation has a significant overhead in on-chip hardware close to the qubit. More precisely, it requires the presence of a charge reservoir or a quantum dot tunnel-coupled to the qubit for read-out. So far, quantum chip development has placed read-out on the side, which is not sustainable when increasing the array's dimensions. Therefore, integrating read-out hardware directly into the architecture would require significant adjustments. Several strategies have been put forth: the first idea would consist in assigning some of the array's quantum dots to the task of read-out. This strategy would come at the price of reduced connectivity [61]. The second approach would build on the idea of maintaining quantum processors' topology intact. It has been proposed as a solution for enabling not only planar but also vertical tunneling for read-out in 3D nanoscale geometry [62]. Such a proposition has some

advantages in regards to initialization but it is technologically challenging. Other strategies propose intensive use of coherent displacement to interconnect quantum nodes separated by a few microns. Adjustable surface for read-out and control of the node's hardware are potentially available and may allow for the reduction of limitations of a dense quantum dot array [63,64], at the price of increasing quantum operations.

6 Conclusions

A careful review of the work around spin qubits clearly demonstrates that they have promising features at a small number of qubits and will be a serious contender in reaching regimes allowing them to efficiently tackle complex computer problems, therefore enabling large-scale quantum computing. Researchers are already exploring the possibility of leveraging VLSI capabilities to build and control qubits, with the goal of understanding how to scale silicon qubit platforms. Yet silicon quantum machines still face a number of challenges, both in terms of the underlying physics and the technology itself. VLSI technologies will be key to addressing these challenges because, though VLSI has more inherent limitations and less versatility, it holds the promise of higher-quality devices and higher yields. These aspects will be the most critical aspects for reaching large-scale quantum machines.

Data Availability Statement This manuscript has no associated data. [Authors' comment: Data sharing not applicable to this article as no datasets were generated or analysed during the current study.].

Code Availability Statement This manuscript has no associated code/software. [Authors' comment: Code/Software sharing not applicable to this article as no code/software was generated or analysed during the current study.].

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