

Preliminary Design of Pulse Digitalization and Readout Electronics for CDEX-10

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Abstract. CDEX (China Dark Matter Experiment) is now planning to be upgraded to about 10 Kg HPGe (High Purity Germanium) detectors (CDEX-10) and the new suitable dedicated pulse digitizer and readout electronics are on demand. The readout system is interfaced to the front preamplifiers, which has two “slow” outputs with typical 6- μ s shaping time and two “fast” output with typical 300-ns shaping time. In this preliminary design of pulse digitalization and readout electronics, 8-channel 14-Bit 100 MSPS ADC (Analog-to-Digital Converter) and 4-channel 12-Bit 1 GSPS ADC are embedded in the 6U-size readout prototype board. The RAIN1000Z1 readout module based on ZYNQ SoC (System on Chip) is used for readout with Gigabit Ethernet. The ENOB (Effective Number Of Bits) of ADC and the TCP data throughput of Gigabit Ethernet will be discussed. The preliminary result of gamma-ray spectrum will also be presented.

1. Introduction

The CDEX [1] experiment is deployed in CJPL (China Jinping Underground Laboratory) [2] located in Xichang, Sichuan province, China. The new generation of HPGe detector will be increased to about 10 detector modules (the total weight is about 10 Kg) [3]. A new pulse digitalization and readout electronics are needed for the pulse signals from the array of detectors, which should be plugged in the 6U-size crate and transmit data to server or PC with Gigabit Ethernet interface.

Figure 1 depicts the overall system architecture of CDEX-10 experiment and the details of readout electronics with trigger and synchronized clock. Commercial Ethernet switches and servers are used for online transmission and storage. The Germanium detectors are operated in a cryogenic environment and the preamplifiers' circuit (include the JFET, several resistors, capacitors, etc.) also must be operated at cryogenic temperate, the others of preamplifiers can be deployed in the warm place [5], including the output drivers, shaping, amplifiers, etc. The preliminary design of pulse digitalization and readout electronics is used for the pulse digitalization and readout of different signals. These include two “slow” signals and two “fast” signals from Germanium detector, and two signals from NaI (TI) Anti-Compton detector. The pulse waveform data from ADCs (Analog-to-Digital Converter) is buffered in the FPGA with external DDR3 SDRAM. The readout module RAIN1000Z1 [6] is used for data readout to server with Gigabit Ethernet. Synchronized clock is fan-out to every readout board from the rubidium clock in 10 MHz with 10 ps jitter.



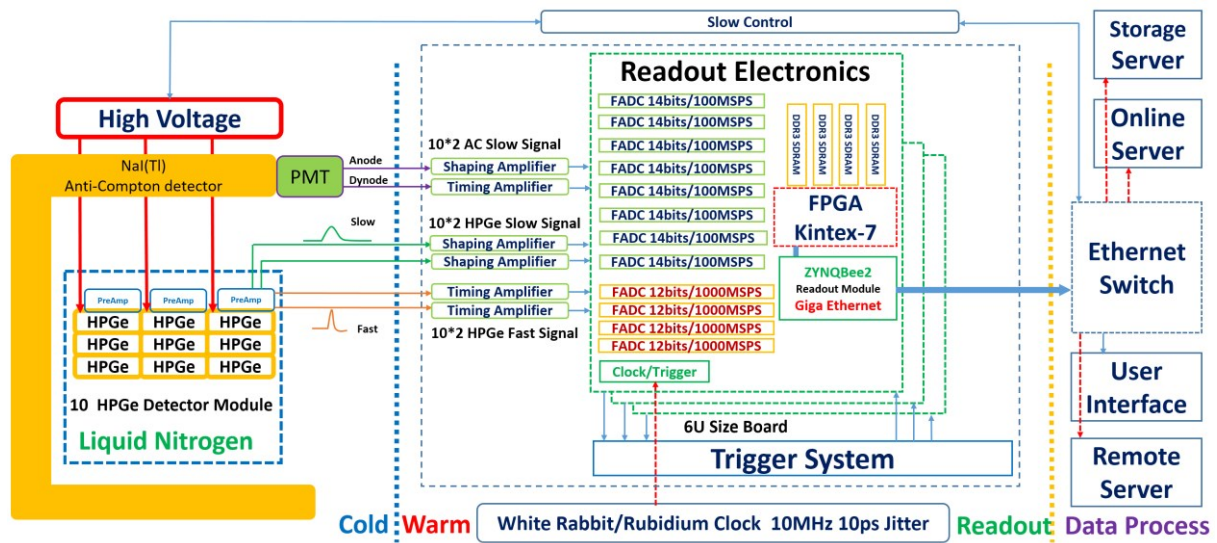


Figure 1. The whole system architecture of readout electronics in CDEX-10 experiment.

2. Performance test and preliminary result

The performance test includes the analog part with the ENOB of ADCs (14-Bit 100 MSPS ADC and 12-Bit 1 GSPS ADC) at different input sine wave frequency and the digital part with data throughput of Gigabit Ethernet. The gamma-ray source ^{57}Co is used to obtain the preliminary result of energy spectrum.

2.1. ENOB (Effective Number Of Bits) of ADC

The analogue performance is conducted with a precision SMA100A pure sine signal generator from Rohde & Schwarz with dedicated band-pass filters (BPFs), according to IEEE 1241-2000 standard. The DES (Dual Edge Sampling) mode is where the ADC12D1000 is operated at 2 GSPS and Non-DES mode is 1 GSPS. In the prototype, the ENOB performance of the AD9253 and ADC12D1000 is described in figure 2.

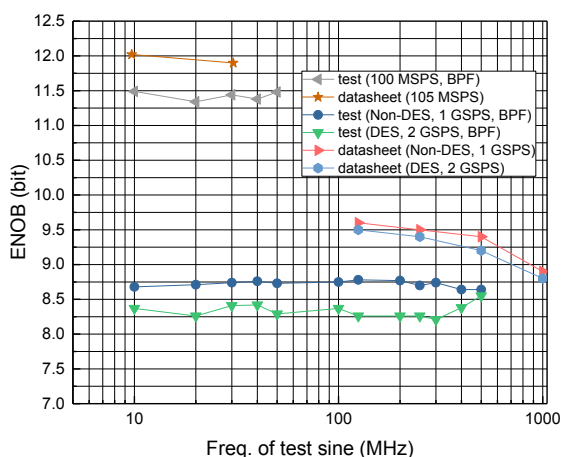


Figure 2. The ENOB of the AD9253 and ADC12D1000 in this design with the SMA100A and BPFs.

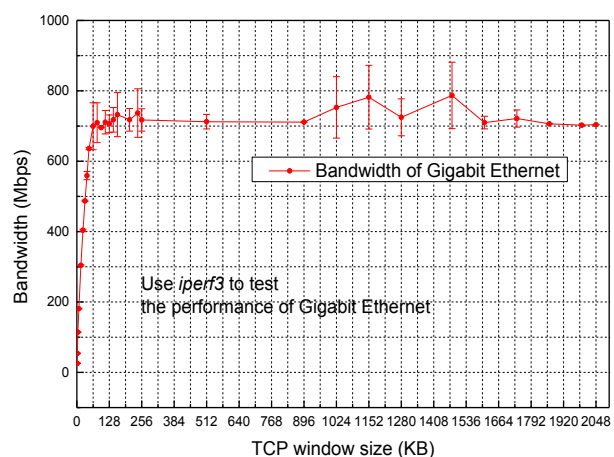


Figure 3. The data throughput performance of the Gigabit Ethernet readout.

2.2. Ethernet data throughput performance test

Ethernet data throughput based on RAIN1000Z1 readout module is also tested. The TCP/IP raw data throughput with Gigabit Ethernet interface is more than 700 Mbps with the RAIN1000Z1 readout module and associated software in PC or servers. The data throughput performance is depicted in figure 3. It is tested with *iperf3* (e.g. the command `./iperf3 -c 166.111.32.251 -i 2 -w 1024B -t 20` are used to test the 1 KB size of the TCP window). For every test point, there are ten samples, which have the interval of two seconds.

2.3. Preliminary result of energy spectrum

The typical 6- μ s shaping pulse is shown in figure 4. The pulse is from the shaping amplifier (Canberra 2026) by the 14-bit 100 MSPS ADC. The spectrum of ^{57}Co is shown in figure 5. The energy resolution is (535 ± 9) eV @ 122 keV.

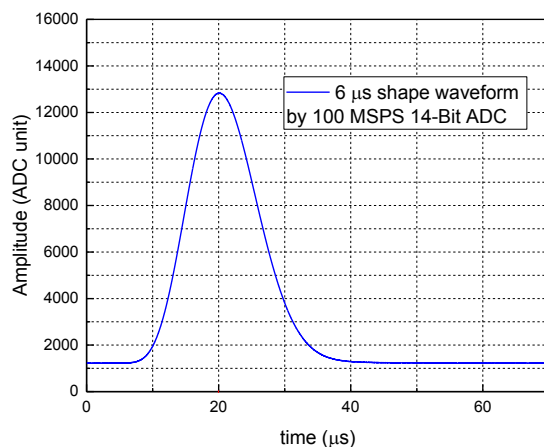


Figure 4. The ENOB of the AD9253 and Gigabit Ethernet readout. ADC12D1000 in this design with the SMA100A and BPFs.

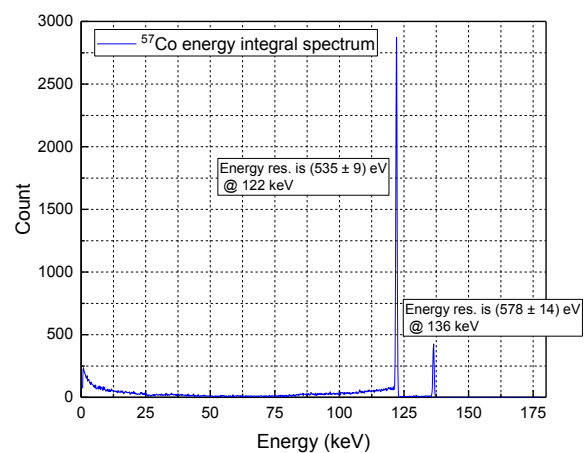


Figure 5. The data throughput performance of the Gigabit Ethernet readout.

3. Conclusions and future work

This preliminary design of the pulse digitalization and readout board, including FPGA, readout module and the combined 14-Bit 100 MSPS ADC with 12-Bit 1 GSPS ADC, is adequate for digitalization and readout of pulse signals from the Germanium detectors and the Anti-Compton detectors. The performance of analogy part and Gigabit Ethernet data throughput is fulfilling the requirement of experiment.

In the future, this system will be deployed with the CDEX-10 and more physical results will be presented. The shape amplifiers and timing amplifiers will be designed and integrated in the future data acquisition system.

References

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