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TOPICAL WORKSHOP ON ELECTRONICS FOR PARTICLE PHYSICS 2014,
22–26 SEPTEMBER 2014,
AIX EN PROVENCE, FRANCE

The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments

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ABSTRACT: The future upgrades of the LHC experiments will increase the beam luminosity leading to a corresponding growth of the amounts of data to be treated by the data acquisition systems. To address these needs, the GBT (Giga-Bit Transceiver optical link [1, 2]) architecture was developed to provide the simultaneous transfer of readout data, timing and trigger signals as well as slow control and monitoring data. The GBT-SCA ASIC, part of the GBT chip-set, has the purpose to distribute control and monitoring signals to the on-detector front-end electronics and perform monitoring operations of detector environmental parameters. In order to meet the requirements of different front-end ASICs used in the experiments, it provides various user-configurable interfaces capable to perform simultaneous operations. It is designed employing radiation tolerant design techniques to ensure robustness against SEUs and TID radiation effects and is implemented in a commercial 130 nm CMOS technology. This work presents the GBT-SCA architecture, the ASIC interfaces, the data transfer protocol, and its integration with the GBT optical link.

KEYWORDS: Radiation-hard electronics; Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); VLSI circuits

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Contents

1	Introduction	1
2	GBT-SCA architecture	2
3	The GBT-SCA communication architecture	5
3.1	The E-link transport protocol layer	5
3.2	The SCA channel command protocol layer	6
4	ASIC implementation	7
5	Summary and outlook	8

1 Introduction

The GBT (Giga-Bit Transceiver) system [1] was developed with the purpose to provide on a unique optical link the simultaneous transfer of the three types of information required by the High Energy Physics experiments: readout data (DAQ), timing and trigger information (reference clock and trigger decisions) and detector control and monitoring information. Figure 1 depicts the generic topology of the GBT system while figure 2 shows a typical implementation of on-detector electronics making use of the GBT-chipset.

The GBT-SCA ASIC (Giga-Bit Transceiver - Slow Control Adapter) is an integrated circuit built in a commercial 130 nm CMOS technology and is the part of the GBT chipset which purpose is to distribute control and monitoring signals to the front-end electronics embedded in the detectors. It connects to a dedicated electrical port on the GBTX ASICs through an 80 Mbps dual redundant bidirectional data-link; namely the e-links [3]. In order to meet the requirements of different front-end ASIC in various experiments, the SCA provides a number of user-configurable electrical interface ports, able to perform concurrent data transfer operations. The user interface ports are: 1 SPI master, 16 independent I²C masters, 1 JTAG master and 32 general-purpose IO signals with individual programmable direction and interrupt generation functionality. It also includes 31 analog inputs multiplexed to a 12 bit ADC featuring offset calibration and gain correction as well as four analog output ports controlled by four independent 8-bits DACs.

This paper describes the architecture, operation and implementation of the SCA ASIC. Section 2 presents the overall architecture and internal circuitry organization while section 3 presents the communication architecture and its layered structure. Finally section 4 presents the ASIC implementation and the design techniques employed to mitigate the effects of single event upsets.

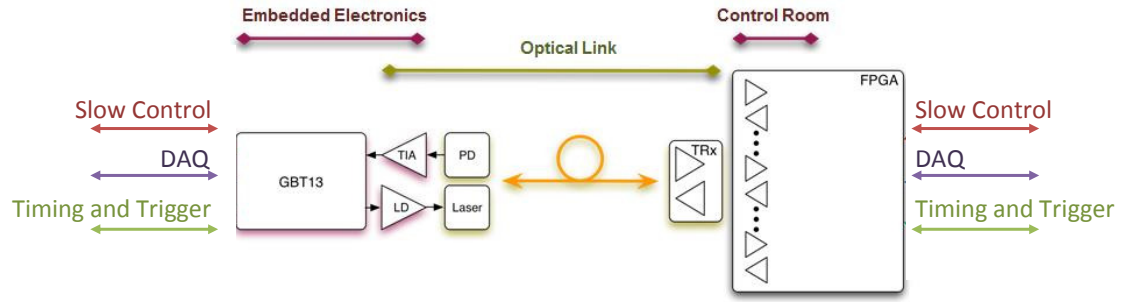


Figure 1. GBT system architecture.

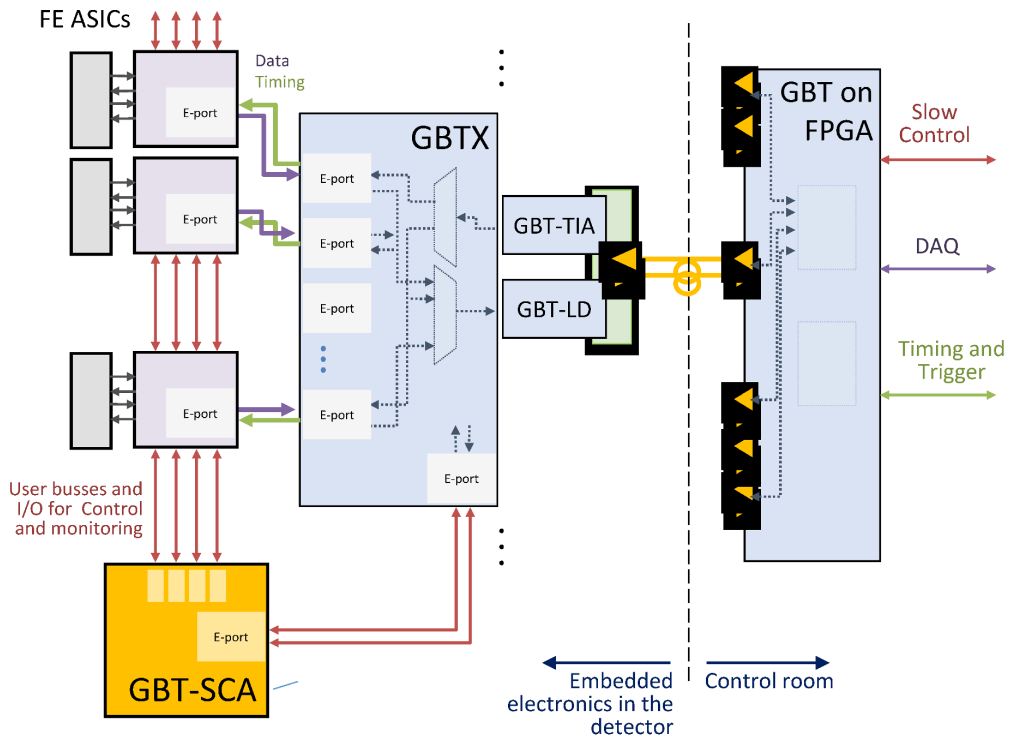


Figure 2. GBT chipset front-end system architecture.

2 GBT-SCA architecture

The architecture of the SCA ASIC is shown in figure 4. The SCA is broadly composed of two e-link ports that connect to the GBTX ASICs, a set of user interface ports to connect with the on-detector electronics and a network controller that routes the information between the e-links and the user interfaces.

Typically, the SCA ASIC connects via an e-link to the special purpose slow control e-port of the GBTX ASIC. This dedicated e-port runs at 40MHz double data rate (DDR) mode giving an effective data rate of 80 Mbps. It is also possible to connect the SCA ASIC to any of the other GBTX

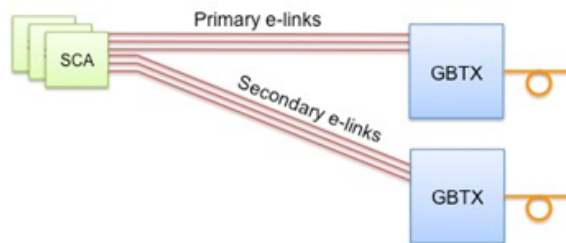


Figure 3. Dual redundant e-link ports connection.

e-ports as long as its data transfer mode is properly configured for 40MHz DDR operation. This feature permits the scalability of the slow control system and effectively allows the implementation of front-end topologies where a GBT link could be used for slow control only operations.

The disposal of two, functionally identical, e-link ports on the SCA facilitates the implementation of redundancy schemes anticipating failures on the optical links. A possible redundancy scheme is depicted in figure 3 where two GBTX ASICs connect to the same SCA ASIC. In this scheme only one of the e-ports is active at any moment. The active port is also the source of the 40MHz system clock that synchronizes the SCA internal state machines. The inactive port is properly muted and any activity on the clock or data lines is discarded. Switching over between e-ports is performed on user's demand by issuing a "CONNECT" command which is specially foreseen in the high-level communication protocol as described in section 3. One of the e-ports is considered as primary and the other as secondary. On power-up the primary e-port is automatically selected for operation.

Both e-ports communicate with the Network Controller block via an Atlantic interface parallel bus [4]. The Network Controller connects further with all the interface channels via a common Wishbone bus [5]. The interface channels are circuit blocks that implement the functionalities of the user interface ports. The interface channels can operate independently and concurrently. As described in section 3, the SCA uses a packet oriented communication protocol. The Network Controller block implements the functionalities of routing the data packets to and from the interface channels as well as supervising the operation of the interface channels. The channels can demand attention to transmit data at any time asserting an interrupt line on the internal Wishbone interconnect fabric. A Wishbone bus arbiter using the round robin technique handles the interrupts. An auxiliary I²C port is attached on the internal Atlantic interface bus, bypassing the e-link ports, and can be used for debugging purposes.

The SCA ASIC integrates the following interface channels:

- 16 independent I²C master serial bus channels. The I²C channels feature individually programmable data transfer rates from 100KHz to 1MHz and can generate both 7-bit and 10-bit address as well as single-byte and multi-byte I²C bus transactions. They can also perform Read, Write and Read/Modify/Write transactions on the I²C bus. The transactions are initiated by the reception of a user command and executed locally by the channel's state machines. Upon completion a return packet is generated containing user data and status flags. These channels can be individually disabled to reduce power consumption in periods of inactivity.

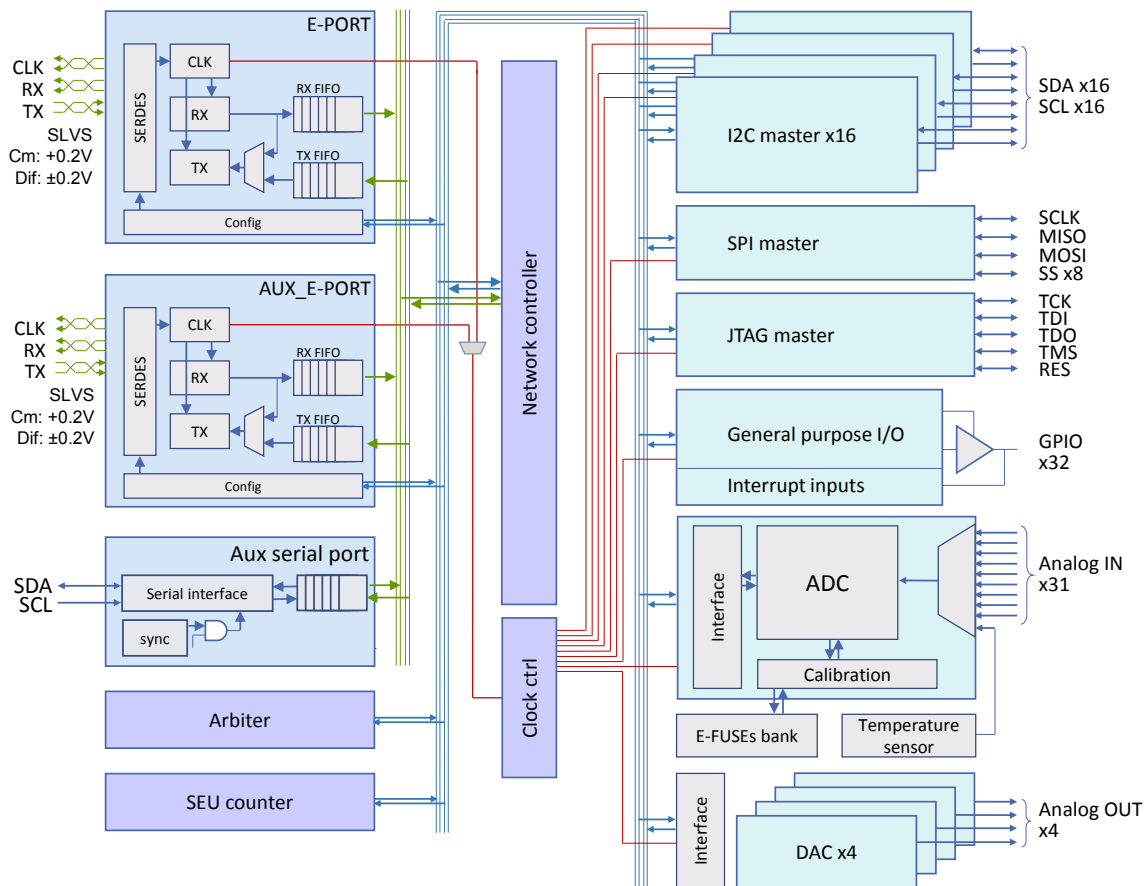


Figure 4. GBT-SCA block diagram.

- 1 SPI serial bus master channel with 8 individual slave select lines. The Serial Peripheral Interface (SPI) channel implements a full duplex synchronous serial bus master with a single transaction length of up to 128 bits and a programmable transfer rate up to 20 MHz. It supports all the standard SPI bus operating modes: 00, 01, 10 and 11. It also integrates 8 independent slave-select lines. The bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps. The SPI channel is implemented around a 128-bit shift register that serializes and de-serializes the bit-streams between the MISO and MOSI SPI lines and the internal parallel bus. The SPI channel is protocol agnostic. The user specific protocol is implemented in FPGA circuitry residing at the control room electronics. The SPI channel can be powered down to conserve power.
- 1 JTAG serial bus master channel. The JTAG channel can perform bus transactions of up to 128-bit length. Longer transactions are also possible by segmenting them and having them executed on consecutive channel commands. The interface implements an asynchronous reset line of configurable pulse width. The bus frequency spans from 156KHz up to 20MHz in 128 user programmable steps. The JTAG channel is implemented around two 128-bit shift register that serializes and deserializes the bit-streams between the TMS, TDO and TDI lines and the internal parallel bus. The JTAG channel in the SCA does not implement a JTAG

master state machine. The JTAG bus cycles will be generated by the FPGA circuitry residing at the control room electronics. The SPI channel can be powered down to conserve power.

- 1 Parallel Interface Adapter (PIA) channel featuring 32 General Purpose digital IO lines. Each line can be individually programmed as input or output or in a tri-state mode. Input signals are sampled and registered at the raising or falling edges of the system clock or of an external strobe signal from the user's application connected on a dedicated input line. Any line configured as input can be programmed to generate an interrupt request to the control room electronics. The electrical levels on all digital IO lines are 0 - 1.5 V.
- 1 ADC channel with 31 multiplexed analog inputs. The ADC channel block consists of a 32 input analog multiplexer connected to a 12-bit analog to digital converter (ADC). One analog input is internally connected to the embedded temperature sensor while the remaining 31 inputs are available to the user. All inputs feature a switchable 10 μ A current source to facilitate the use of externally connected resistance temperature sensors (RTD). The ADC adopts a single-slope Wilkinson architecture. This architecture features circuit simplicity and low power consumption. The long conversion time associated with this architecture is perfectly compatible with the conversion requirements of slow varying parameters like detector leakage current and temperature, power supply voltages etc. The analog input range is 0.0 V to 1.0 V, the maximum conversion rate is 3.5 KHz and the maximum quantization error is 1 LSB. The ADC block features automatic offset cancellation and gain correction circuitry. The comparator offset is removed by performing an offset evaluation cycle before any conversion. The gain error is corrected by multiplying the converted value with a gain calibration coefficient. The gain calibration coefficient is evaluated during production phase for every chip and stored on the on-chip e-fuse bank. The stored coefficient can be overridden by the user to compensate for any possible drifts caused by the radiation environment in the field application.
- 4 DAC channels. There are four independent digital to analog converter (DAC) channels featuring 8-bit resolution and capable to generate voltage signals in the range of 0.0 V to 1.0 V.

3 The GBT-SCA communication architecture

The slow control system is organized in a point-to-point network topology where a fixed bandwidth of 80 Mbps is allocated by the GBT system for slow control functions. The communication architecture used by the SCA is based on two protocol layers as shown in figure 5:

- The e-link transport protocol
- The SCA channel command protocol

3.1 The E-link transport protocol layer

The e-link port on the SCA ASIC implements a packet oriented full duplex transmission protocol based on the HDLC standard (ISO/IEC 13239:2002) [6]. The structure of the HDLC data packet

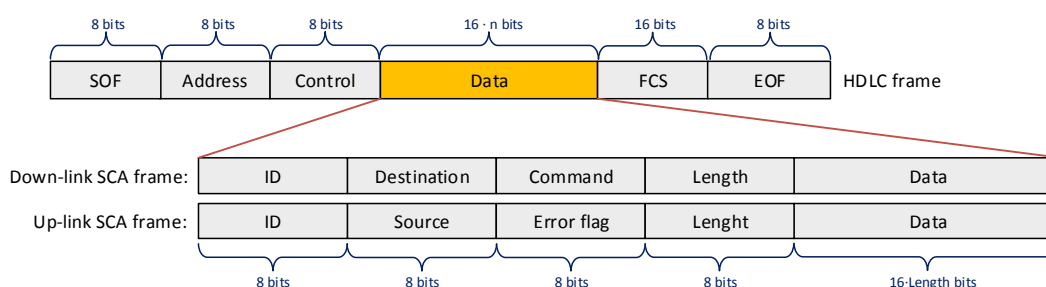
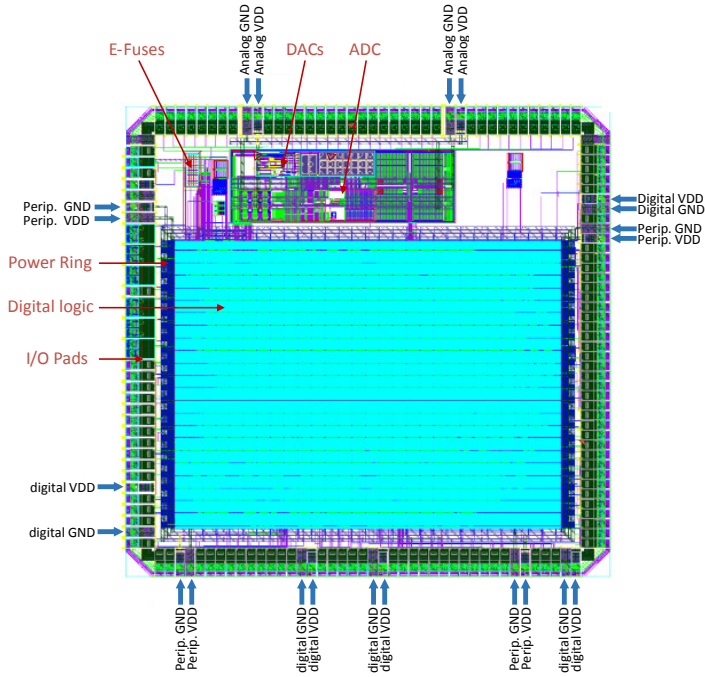


Figure 5. Communication architecture of the GBT-SCA.

is shown on figure 5 and consists of a frame delimiter character (SOF), an 8-bit address field, an 8-bit control field, a variable length data payload field and a 16-bit frame checksum field (FCS). The HDLC protocol is employing the “bit-stuffing” technique to implement a frame delimiter character. The frame delimiter is composed of six consecutive ‘1s’. The protocol assures that this combination is not found anywhere else in the data bit-stream by any inserting a ‘0’ in any sequence of five consecutive ‘1’ at the transmitter side and by stripping off this trailing ‘0’ at the receiver side. Bits within the frame are transmitted from the least significant bit first. A Frame Check Sequence (FCS) field is calculated over the address, control and information field using the CCITT standard 16-bit CRC. The control field contains frame sequence numbers of the currently transmitted frame and the last correctly received frame implementing a acknowledgement handshake mechanism between the SCA and the control room electronics. All transmitted HDLC frames require the reception of HDLC response frames with positive acknowledgment. The control field is also used to convey three supervisory level commands. The CONNECT command that instructs the SCA e-port to activate and receive data, deactivating at the same time the alternate redundant e-port. The RESET command that resets the SCA e-port, its internal FIFOs and state machines. Finally, the TEST command that sets the SCA e-port in loopback mode to facilitate the link verification and debugging operations in the field application.

3.2 The SCA channel command protocol layer

The SCA uses a command-oriented protocol to address the on-chip interface channels and instruct the execution of specific operations. The SCA command frames are encapsulated in the HDLC e-link transport frames as shown in figure 5. The SCA command frames consist of an 8-bit transaction identification field (ID field), an 8-bit Destination/Source address field, an 8-bit Command/ErrorFlag field, an 8-bit Length qualifier, and a Data field of variable length. The transaction ID field associates the transmitted commands with the corresponding data replies, allowing the concurrent use of all the SCA channels. ID values 0x00 and 0xff are reserved for interrupt packets generated by one or more of the 32 programmable edge sensitive general purpose digital input lines. The Destination/Source address field refers to the target channel. The Command field is present in the frames received by the SCA and indicates the operation to be performed. The Error Flag field is present in the channel reply frames to indicate error conditions encountered in the execution of a



Die size	2.6 x 2.6 mm
Digital supply voltage	1.5V
Analog supply voltage	1.5V
Periphery supply voltage	1.5V
Digital input voltage range	0V to 1.5V
Digital output voltage range	0V to 1.5V
Analog input voltage range	0V to 1V
Analog output voltage range	0V to 1V

Figure 6. GBT-SCA layout and general characteristics.

command (reception of an invalid command, invalid channel address, no response from the target device etc.). If no errors are found, its value is 0x00. The Data field is command dependent and the length qualifier field indicates its length.

4 ASIC implementation

Due to the increase of the LHC beam luminosity, the on detector electronics will be exposed to radiation levels expected to reach 200 MRad in some of the inner detectors. To address the TID requirements the SCA ASIC is implemented in a commercial 130 nm CMOS technology largely characterized for radiation tolerance and adopted for the implementation of the entire GBT-chipset. The increased luminosity of the LHC beam will also lead to an increase of the SEU (Single Event Upset) rate. To mitigate the effects of SEUs we have employed the Triple Modular Redundancy (TMR) technique at the state machine level in the entire digital circuitry of the SCA ASIC. A set of Python scripts was developed to automatize the state machine triplication and the generation of synthesizable HDL code. The clock tree was also triplicated to mitigate the effects of SET (Single Event Transients) on the clock tree buffer elements. To verify the triplication process and ensure that no errors are unintentionally slipped in the generated HDL code we have developed Tool Command Language (TCL) scripts for random error injection in all digital circuitry nodes for both behavioral Register Transfer Level (RTL) simulations as well as gate-level, post-place-and-route simulations. To help reduce the power consumption in the digital circuitry we have employed a clock gating technique on all interface channel blocks. All the analog blocks of the SCA (ADC, DAC, bandgap voltage reference and biasing circuits) were laid out in one single analog block.

For the top-level chip assembly and final physical verification we have used a digital-on-top fully scripted backend implementation. The analog/mixed-signal modules were therefore imported in the top-level netlist of the digital-centric design. Figure 6 shows the layout of the chip.

For a digital-centric design where the analog/mixed-signal IP is imported, a netlist-driven flow with a Digital-on-Top methodology is used.

5 Summary and outlook

The GBT-SCA ASIC is part of the GBT-chipset and is designed to address the needs of the slow-control functionalities of the on-detector electronics of future LHC experiments. The GBT-SCA dispatches and collects control and monitoring information to and from the front-end ASICs and the control room electronics. It implements several transmission protocols on the local electrical links and analog ports, using a command-oriented communication protocol. The ASIC is implemented in a 130nm commercially available CMOS technology and has been submitted for prototyping on a common Multi Project Wafer run along with all other ASICs comprising the GBT chipset. The SCA ASIC will be packaged in a 196-pin 12 x 12 low-profile ball-grid array (LFBGA) plastic package with a ball pitch of 0.8mm and ball diameter of 0.5mm. Test benches are in preparation to validate the functionality of the ASIC and characterize the performance of the ADC and DAC circuitry. Further tests for TID performance qualification and SEU irradiation characterization are also foreseen. Subject to successful test results, sample packaged chips will be made available to the front-end system developers.

Acknowledgments

The authors would like to thank the members of the MEDIPIX collaboration for their contribution of IP blocks for the implementation of the DAC circuitry and specially X. Llopart Cudie for his assistance in the reuse of these IP blocks in the SCA ASIC.

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