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Front End Readout Electronics for the CMS Hadron Calorimeter

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***Abstract--* The front-end electronics for the CMS Hadron Calorimeter provides digitized data at the beam interaction rate of 40 MHz. Analog signals provided by hybrid photodiodes (HPDs) or photomultiplier tubes (PMTs) are digitized and the data is sent off board through serialized fiber optic links running at 1600 Mbps. In order to maximize the input signal, the front-end electronics are housed on the detector in close proximity to the scintillating fibers or phototubes. To fit the electronics into available space, custom crates, backplanes and cooling methods have had to be developed. During the expected ten-year lifetime, the front-end readout electronics will exist in an environment where radiation levels approach 330 rads and the neutron fluence will be 1.3E11 n/cm^2. For this reason, the design approach relies heavily upon custom radiation tolerant ASICs. This paper will present the system architecture of the front-end readout crates and describe our results with early prototypes.**

I. Introduction

The CMS experiment is designed to run with a beam crossing time of 25ns or at 40 MHz. The front-end electronics must digitize analog signals from HPDs[1] or PMTs at the rate of 40 MHz. The data from each detector subsystem will be synchronized with all other channels to take out any transmission timing effects due to differing lengths of scintillating fibers and time of flight. Data is transmitted off board at 1600 Mbps to the Trigger/DAQ readout, see Figure 1. No data compression is performed by the front-end electronics.

II. The Front End Readout Cards

The front-end readout cards must condition the analog signal, digitize it and send the result off board at 40 MHz. The cards, pictured in Figure 2, make extensive use of ASICs. The analog to digital converter is a QIE ASIC (QIE8)[2] which was developed for CMS by engineers at Fermi National Accelerator Laboratory (FNAL). The board also utilizes a Channel Control ASIC (CCA)[3] developed at FNAL, as well a Gigabit Optical Link (GOL)[4] developed at CERN, the European Organization for Nuclear Research.

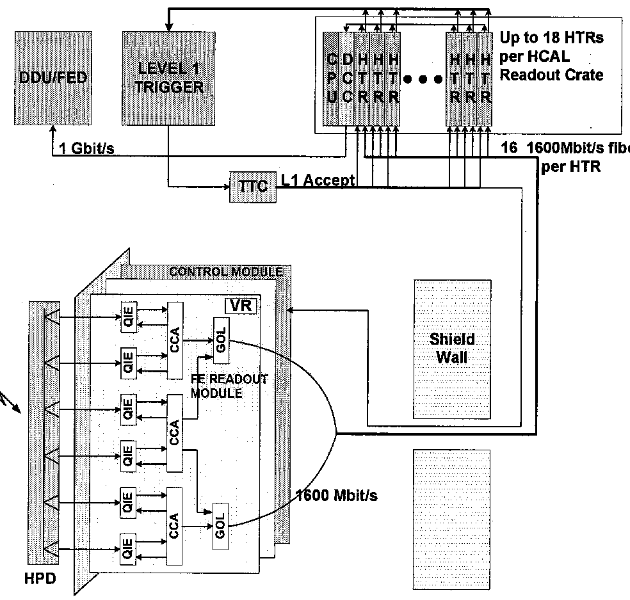

Figure 1. CMS HCAL System Architecture Overview

A. The QIE

QIE is an acronym for the functions of the ASIC - Q (charge) I (integration) and E (encode). A large dynamic range is accomplished through a non-linear multi-range technique. The input current is simultaneously integrated on all ranges, and comparators are used to select the lowest range that is not at full scale. The selected voltage representing the integrated charge is then put through an on-chip Flash ADC. The outputs of the Flash ADC are a 5-bit mantissa representing the voltage and a two-bit code indicating the range. A two-bit Capacitor ID is also provided. The QIE utilizes four integrating capacitors. Operations are time multiplexed and pipelined to allow signals to settle, be integrated and cleared. Latency is 100 ns as the pipeline is four clock cycles deep.

The CMS QIE has two independent input amplifiers. This was necessary so that the QIE could accept the negative HPD

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pulses of the barrel electronics, as well as the positive pulses from the PMTs used in the forward calorimeter.

The inverting amplifier was designed for the positive current pulses from HPD's. A current gain of –2.6 is applied by the inverting input amplifier. Low-end sensitivity is approximately 1 fC/bit. The maximum input charge per bucket accepted by the inverting input is approximately 10 pC.

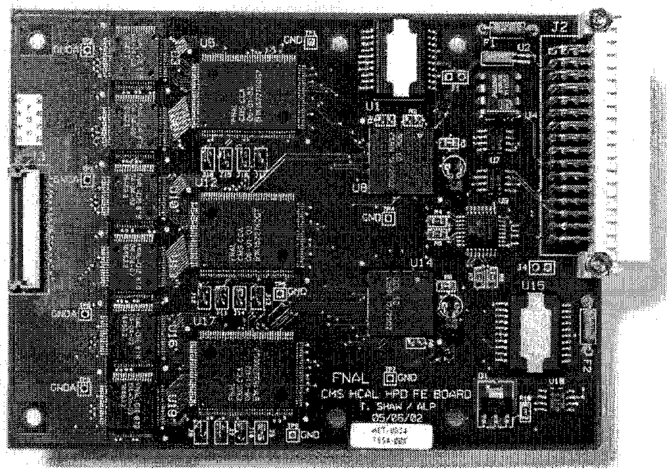

Figure 2. Photograph of CMS HCAL Front End Module

The non-inverting input is designed to work with fast negative current PMT signals. The amplifier gain is approximately one, resulting in a low-end sensitivity of 2.6 fC/bit. The maximum charge accepted per bucket by the non-inverting input is approximately 26 pC.

The Flash ADC provides a dynamic range of 10,000:1, or about 13 bits. It does this by utilizing a piecewise linear conversion. As shown in Table 1, there are 15 bins weighted one, seven bins weighted two, four bins weighted three, three bins weighted four, and three bins weighted 5. Each successive range applies a times 5 weighting factor. Please note that the exact charge conversion is dependent upon fabrication process, and therefore must be calibrated on a chip-by-chip basis. This is why the column labeled "Approximate Input Charge" is a charge range, rather than an exact charge. In all cases, the approximate input charge should be within 20% of nominal.

TABLE 1
INVERTING INPUT SCALE (HPD INPUTS)

Range (2 bits)	Approximate Input Charge	FADC Codes (5 bits)	Gain (q/Lsb)
0	-1 fC --- 14 fC	0---14	1 fC/bin
0	14 fC --- 28 fC	15---21	2 fC/bin
0	28 fC --- 40 fC	22---25	3 fC/bin
0	40 fC --- 52 fC	26---28	4 fC/bin
0	52 fC --- 67 fC	29---31	5 fC/bin
1	57 fC --- 132 fC	0---14	5 fC/bin
1	132 fC --- 202 fC	15---21	10 fC/bin
1	202 fC --- 262 fC	22---25	15 fC/bin
1	262 fC --- 322 fC	26---28	20 fC/bin
1	322 fC --- 397 fC	29---31	25 fC/bin
2	347 fC --- 722 fC	0---14	25 fC/bin
2	722 fC --- 1072 fC	15---21	50 fC/bin
2	1072 fC --- 1372 fC	22---25	75 fC/bin
2	1372 fC --- 1672 fC	26---28	100 fC/bin
2	1672 fC --- 2047 fC	29---31	125 fC/bin
3	1797 fC --- 3672 fC	0---14	125 fC/bin
3	3672 fC --- 5422 fC	15---21	250 fC/bin
3	5422 fC --- 6922 fC	22---25	375 fC/bin
3	6922 fC --- 8422 fC	26---28	500 fC/bin
3	8422 fC --- 10297 fC	29---31	625 fC/bin

Figure 3 represents test bench data gathered by measuring the response of the non-inverting input. The figure shows the response of the QIE as increasing charge is applied. The four distinct ranges can be seen, as well as the piecewise linearity of the ranges.

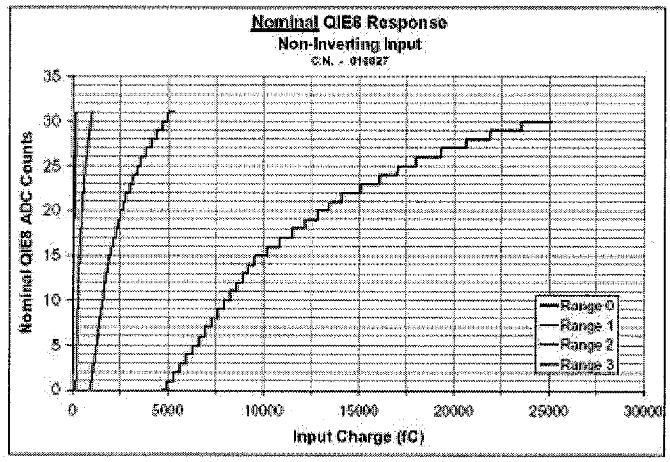

Figure 3. Measured Response of Non-Inverting Input

B. The Channel Control ASIC

The modules also use a custom Channel Control ASIC (CCA) developed at FNAL. The CCA was designed specifically to service the QIE and to provide initial processing of QIE data. Each CCA services and receives the digital data from two QIEs.

Figure 4 is a block diagram representation of the connectivity of the QIEs, CCAs and GOL. As can be seen, all QIE control signals are delivered via the CCA. Additionally, all QIE data is passed through the CCA before being sent to the optical link driver. Most importantly, the CCA allows for the phasing of the 40 MHz clock driving the QIE. This allows customization of the integration clock timing on a channel-by-channel basis, so that the correct charge integration window is accomplished. The CCA also allows for a programmable alignment of the QIE data, which can take out any channel-to-channel skew effects of up to 50ns.

The CCA also provides the following functions:

- A check of the accuracy of the Capacitor IDs (the Cap IDs from different QIEs should be in synchronization),
- The ability to force the QIE to use one of four internal ranges,
- The ability to set QIE Pedestal DAC values,
- The ability to issue two test pulse triggers of programmable polarity,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optical link,
- The ability to reset the QIE,
- And, the ability to send and report on any detected errors at a known and determined time.

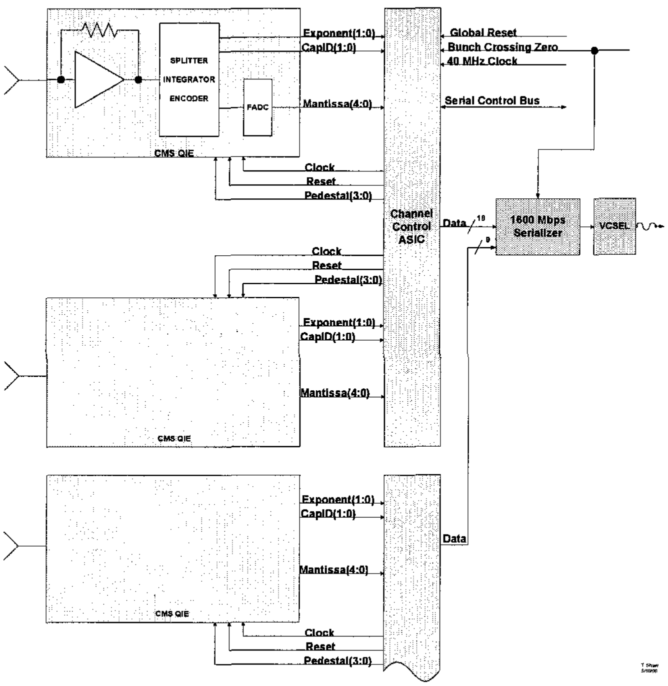

Figure 4. QIE, CCA and GOL connection overview.

C. *The Gigabit Optical Link and VCSEL*

The data is sent off board through the use of a rad hard serializer ASIC, the Gigabit Optical Link (GOL). The GOL has been developed by the microelectronics group at CERN. Data is transmitted at 1600 Mbps in 8B/10B format through this link.

The GOL provides a laser driver output. The laser driver output is used to drive a commercial VCSEL, Honeywell's HFE4191-541. Data is sent off board to data concentrator crates through optical cables plugged into the VCSELs.

III. The Readout Box Mechanics And Backplane

Custom crates, backplanes and cooling had to be developed to house the front-end electronics. The crates, or Readout Boxes (RBXs)[5], make use of aluminum cooling plates and circulating water to cool the electronics. RBX design was driven by available detector space. Four distinct mechanical designs have had to be developed for each of the inner barrel, outer barrel, endcap and forward regions of the detector. Figure 5 shows an inner barrel RBX prototype.

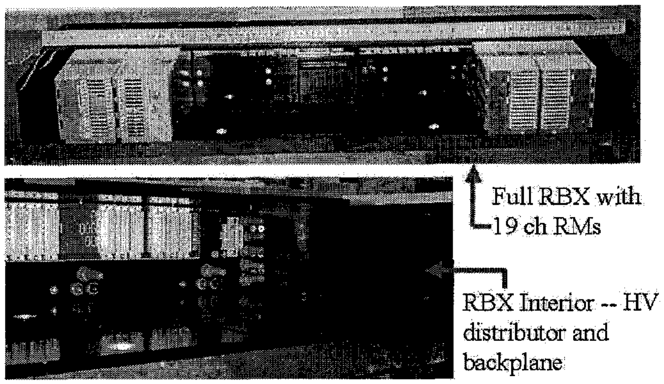

Figure 5. Picture of RBX.

A. *The Readout Modules*

A Readout Module (RM) is a three card unit which also contains an Optical Decoder Unit (ODU)[6], the HPD, and a HPD interface card. The ODU provides for grouping of input fibers into one of eighteen HPD pixels. The HPD produces approximately 2000 electrons for each photoelectron it sees. The charge from these electrons is supplied to the QIEs on the FE modules, through cables which run between the HPD interface cards and the FE modules. The RM also provides a High Voltage (HV) connection for the HPD via a connector which plugs into the HV distributor located within the RBX.

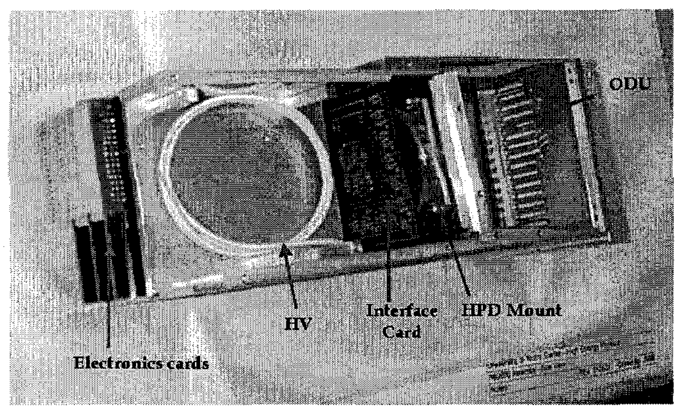

Figure 6. Picture of a Readout Module.

B. *The Electrical Backplane and High Voltage Distributor*

The main functions of the electrical backplane[7] in the RBX is to provide low voltage power in addition to clock and control signals. A separate high voltage distributor is used to provide high voltage to the HPDs.

Unregulated low voltage levels of 6.5 Volts and 5.0 Volts are distributed by the backplane. Onboard regulators, ST Microelectronic LHC4913s[8], are used to provide regulated voltage levels of 5.0, 3.3 and 2.5 Volts.

Clock and control signals are distributed via low voltage PECL signaling levels. Low voltage PECL was chosen because radiation tolerance testing found commercial chips utilizing this technology to be much less prone to single event latch-up than LVDS chips. In order to keep clock jitter low, the 40MHz system clock is distributed to no more than three electrical loads. Therefore, each RM gets its own private copy of the clock.

Other control signals include general resets to initialize the ASICs and resets to re-synchronize the DLL of the CCA and the PLL of the GOL.

A two-wire communication bus is also provided on the backplane. This serial communication path is used to download programmable registers in the CCA and GOL.

C. *The Clock and Control Module*

The Clock and Control Module (CCM) is actually a set of three boards which provide for general control of the RBX.

The Clock Board is used to receive timing information optically from TTC[9] system via the TTCrx[10]. It then distributes the recovered clock to the Front End modules using low voltage differential PECL signaling levels.

The Control Board provides an RS485 interface to the detector slow control system[11]. It distributes control signals through backplane signals and messages through a two-wire communication path.

The Monitor Board monitors the supply voltages and reads out temperature transducers located in each RM.

D. *Cooling*

Cooling of the electronics is accomplished through the use of thermal foam which carries the heat away from the components and into aluminum cooling plates which are in contact with the water cooled top and bottom plates of an RBX. Each RBX is expected to generate no more than 100 Watts of power. Tests show that this method will hold chip temperatures to no more than about 45 degrees centigrade.

IV. CONCLUSIONS

A test beam run took place over the summer of 2002. Two completely instrumented RBXs were used in the test beam, for a total of 144 channels of electronics. The system performed quite well and showed that noise levels of approximately 4500 electrons RMS were achievable. Figure 7 shows a 300GeV pion pulse measured by the electronics. The horizontal axis represents 33ns time slices, and the vertical axis, the charge in femtocoulombs.

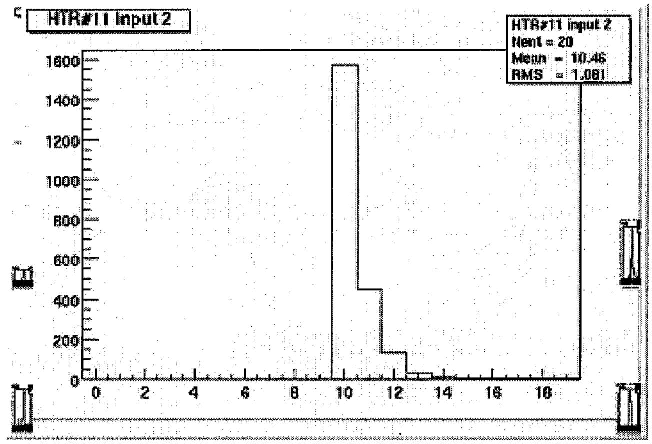

Figure 7. 300 GeV Pions from 2002 Test beam

Further reliability testing is scheduled early in 2003. A 360 channel test beam run will begin in May 2003. Production electronics is scheduled to begin late next summer.

V. ACKNOWLEDGMENT

We would like to thank Charlie Nelson of Fermi National Accelerator Lab for his contributions in testing the prototype QIE chips.

VI. REFERENCES

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